Application Report
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DRV8711 Quick Spin and Tuning Guide

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ABSTRACT

The DRV8711 quick spin and tuning guide is provided as a guide for the tuning steps of the DRV8711. These steps can be used with any DRV8711 system. The report is a high level introduction allowing a new user of the DRV8711 to quickly tune the motor for basic operation. For more details using the decay settings, please refer to SLVA637.

Contents

1 DRV8711 Configuration Items

The items in Table 1 are helpful when configuring the DRV8711. None of the items are required, but many need to be known or selected before configuration is complete. Example values given in Table 1 are from the DRV8711EVM.

Table 1. DRV8711 Configuration

Item		Reference	Example
1	Supply voltage	VM	24 V
2	MOSFET gate charge	Q_g	18 nC
3	MOSFET drain to source resistance	$R_{DS(ON)}$	3.5 mΩ
4	Motor winding resistance	R_L	1.0 Ω/phase
5	Motor winding inductance	L_L	3.5 mH/phase
6	Motor winding parasitic capacitance	C_L	10 nF
7	Motor full step angle	θ_{step}	1.8°/step
8	Motor current	I_L	3.0 A/phase
9	Sense resistor	R_{SENSE}	0.033 Ω
10	Target microstepping level	n_m	16 steps
12	Target motor speed	v	120 rpm
13	Target full-scale current	I_{FS}	1:00 AM
14	Target MOSFET rise time	RT	600 ns
15	Target pulse-width modulation (PWM) chopping frequency	f_{PWM}	40 kHz
16	Target stall detect stepping speed	f_{stall}	60 rpm
17	Target overcurrent protection level	I_{OCP}	2 A

NOTE: The equations on the following pages are to be used as initial values and may not be the optimal settings. For best results, the DRV8711 should be tuned in-system.

NOTE: The default register settings shown in Table 2 are examples. Refer to the DRV8711 data sheet (SLVSC40C) for the default settings.

2 Initial Recommended Settings

The settings in Table 2 are recommended to begin the process for tuning the DRV8711. If additional tuning is required, the information in the remaining sections provides a more detailed process of tuning the DRV8711. With the settings in Table 2, a typical stepper motor with less than 3 A per winding should operate. The stall indicator has been set to a minimal value and must be adjusted if stall indication is desired.

Table 2. Recommended Settings

	Register	Hex Value	Settings
0x01	Torque	0x01TQ	100-µs sample, See torque (TQ) calculation in Equation 1
0x02	Off	0x0032	Internal indexer, 25 µs off time
0x03	Blank	0x0100	Adaptive blanking, 1-µs current blanking
0x04	Decay	0x0510	Use auto mixed decay, mixed decay time has no effect.
0x05	Stall	0x0A02	BEMF/8, Stall after 2, approximately 20 mV (requires experimentation)
0x06	Drive	0x0000	Minimal drive, minimum OCP deglitch and threshold
0x00	Control	0x0C11	850 ns dead time, gain of 5, internal stall detect, 1/4 step, enable motor

$$\text{TORQUE(TQ)} = \text{Hex}\left(\frac{256 \times \text{ISGAIN} \times R_{SENSE}\,(\Omega) \times I_{FS}\,(A)}{2.75\text{V}}\right) \tag{1}$$

3 Microstepping

A stepper motor is driven by regulating the two motor winding currents in a sinusoid fashion. At each step, current is regulated using an adjustable fixed-off-time PWM chopping scheme. A well-tuned system will keep the motor current relatively constant around a current chopping threshold. This threshold is set by an internal sine DAC controlled by an indexer. Whenever a step input is received, the indexer increments its position, and the current chopping threshold is changed (illustrated in Figure 1).

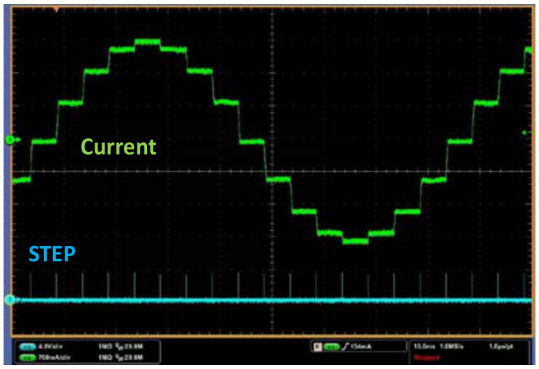

Figure 1. Fixed-Off-Time PWM Chopping Illustration

4 Stepper Motor Speed

The first step in configuring the DRV8711 requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency f_{step} must be applied to the STEP/AIN1 pin, or a '1' must be written to the RSTEP bit every 1 / f_{step} seconds.

If the target motor speed is too high, the motor will not spin. Make sure that the motor can support the target speed.

For a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step}),

$$f_{step}(\text{steps / sec}) = \frac{v(\text{rpm}) \times n_m(\text{steps}) \times 6}{\theta_{step}(° / \text{step})} \tag{2}$$

The value θ_{step} can be found in the stepper motor datasheet, or written on the motor itself.

For the DRV8711, the microstepping level is set by the MODE bits and can be any of the settings in the following **CTRL Register** table. Higher microstepping will mean a smother motor motion and less audible noise, but will increase switching losses and require a higher f_{step} to achieve the same motor speed.

NOTE: All register defaults shown in the following **CTRL Register** table are examples and subject to change. Refer to the datasheet to ensure the correct default settings are used.

CTRL Register Address = 0x00h

Bit	Name	Size	R/W	Default	Description
6-3	MODE	4	R/W	0110	0000: Full-step, 71% current (n_m = 1) 0001: Half step (n_m = 2) *0010: 1/4 step (n_m = 4)* 0011: 1/8 step (n_m = 8) 0100: 1/16 step (n_m = 16) 0101: 1/32 step (n_m = 32) 0110: 1/64 step (n_m = 64) 0111: 1/128 step (n_m = 128) 1000: 1/256 step (n_m = 256)

5 Supported External FETs

It is critical to ensure that any external FETs used can support the PWM current chopping frequency desired. Equation 3 is used to calculate the maximum FET driving capability of the DRV8711:

$$Q_g(\text{nC}) < \frac{20\text{mA} \times (2 \times \text{DTIME} + \text{TBLANK} + \text{TOFF})}{4} \approx \frac{20\text{mA}}{4 \times f_{PWM}(\text{Hz})} \tag{3}$$

In Equation 3, 2 × DTIME + TBLANK + TOFF is the worst-case scenario (smallest time period) for PWM current chopping (1/f_{PWM}). Since the PWM current chopping frequency is not fixed, the desired f_{PWM} only gives an estimate on the worst-case FET driving capacity.

DTIME is the dead-time inserted between turning off a low-side FET and turning on a high-side FET, or vice versa. During this time, both FETs are in High-Z, and current is conducted through the body diodes in asynchronous decay. It is recommended to leave DTIME as its default value unless the stepping speed is very high.

CTRL Register Address = 0x00h

Bit	Name	Size	R/W	Default	Description
11-10	DTIME	2	R/W	11	Dead time set 00: 400 ns dead time 01: 450 ns dead time 10: 650 ns dead time *11: 850 ns dead time*

TBLANK is the blanking time during PWM current chopping. This sets the minimum drive time (current is increasing) during the PWM cycle. At the beginning of the PWM cycle, the current trip value is ignored for TBLANK. In auto mixed decay mode, TBLANK is also the fast decay time if the current is higher than the current chopping level after the drive time. This value is explained more in the Decay Modes section.

BLANK Register Address = 0x03h

Bit	Name	Size	R/W	Default	Description
7-0	TBLANK	8	R/W	0x80h	Sets current trip blanking time, in increments of 20 ns 0x00h: 1.00 µs … 0x32h: 1.00 µs 0x33h: 1.02 µs … 0xFEh: 5.10 µs 0xFFh: 5.12 µs Also sets minimum on-time of PWM

TOFF sets the time that the driver is in a decay mode after the drive phase of PWM current chopping. This value is explained more in the Decay Modes section.

OFF Register Address = 0x02h

Bit	Name	Size	R/W	Default	Description
7-0	TOFF	8	R/W	0x30H	Sets fixed off time, in increments of 500 ns 0x00h: 500 ns 0xFFh: 128 µs

The registers IDRIVEP, IDRIVEN, TDRIVEP, and TDRIVEN are set based on the gate charge of the external FETs used (Q_g), and the desired rise time (RT). RT is the time it will take to charge the FET gate and turn on.

$$\text{IDRIVE} > \text{Q} / \text{RT} \tag{4}$$

$$\text{TDRIVE} > 2 \times \text{RT} \tag{5}$$

IDRIVEN / IDRIVEP and TDRIVEN / TDRIVEP should be selected to be the smallest settings that meet the requirements in Equation 4 and Equation 5.

DRIVE Register Address = 0x06h

Bit	Name	Size	R/W	Default	Description
5-4	TDRIVEN	2	R/W	01	Gate drive sink time 00: 250 ns *01: 500 ns* 10: 1 µs 11: 2 µs
7-6	TDRIVEP	2	R/W	01	Gate drive source time 00: 250 ns *01: 500 ns* 10: 1 µs 11: 2 µs
9-8	IDRIVEN	2	R/W	00	Gate drive peak sink current *00: 100 mA peak (sink)* 01: 200 mA peak (sink) 10: 300 mA peak (sink) 11: 400 mA peak (sink)
11-10	IDRIVEP	2	R/W	00	Gate drive peak source current *00: 50 mA peak (source)* 01: 100 mA peak (source) 10: 150 mA peak (source) 11: 200 mA peak (source)

6 Current Regulation

In a stepper motor, the full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity depends on the TORQUE bits, the ISGAIN setting, and the sense resistor value (R_{SENSE}). During stepping, I_{FS} defines the current chopping threshold (I_{TRIP}) for the maximum current step. Typically, the value of I_{FS} can be found on the motor manufacturer's data sheet.

$$I_{FS}(A) = \frac{2.75V \times TORQUE}{256 \times ISGAIN \times R_{SENSE}(\Omega)} \tag{6}$$

I_{FS} is set by a comparator which compares the voltage across R_{SENSE} to a reference voltage. There is a current sense amplifier built in with programmable gain through ISGAIN. Note that I_{FS} must also follow Equation 5 in order to avoid saturating the motor. VM is the motor supply voltage, and R_L is the motor winding resistance.

$$I_{FS}(A) < \frac{VM(V)}{R_L(\Omega) + 2 \times R_{DS(ON)}(\Omega) + R_{SENSE}(\Omega)} \tag{7}$$

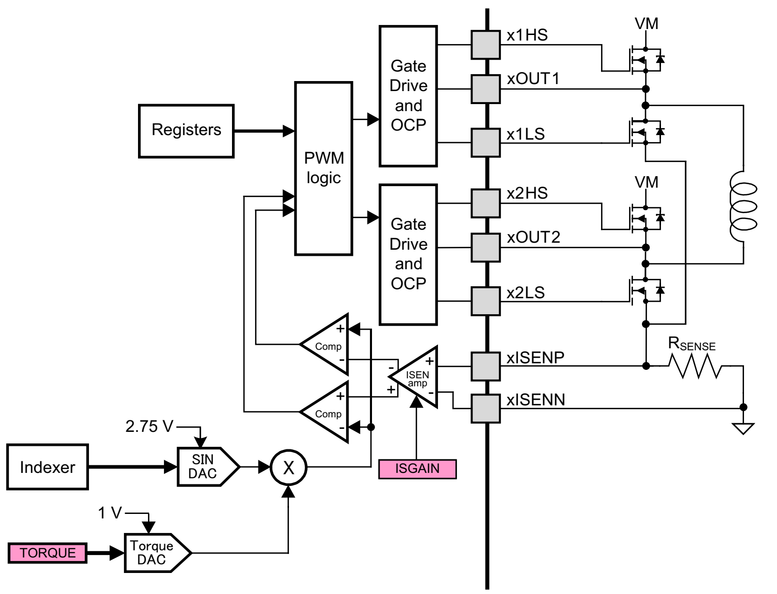

Figure 2.

TORQUE is a register used to scale the output. If TORQUE = 0xFF, then the SIN DAC is scaled by 1. As TORQUE is decreased, the reference is decreased as well.

As an example, the torque register can be reduced when the motor has been stopped. Reducing torque at this point could reduce the current required to hold the motor.

TORQUE Register Address = 0x01h

Bit	Name	Size	R/W	Default	Description
7-0	TORQUE	8	R/W	0xFFh	Sets full-scale output current for both H-bridges

ISGAIN controls the gain of the current sense amplifier. Note that from the Equation 7, increasing this gain will decrease I_{FS} since it is used in the feedback path.

CTRL Register Address = 0x00h

Bit	Name	Size	R/W	Default	Description
9-8	ISGAIN	2	R/W	00	ISENSE amplifier gain set *00: Gain of 5* 01: Gain of 10 10: Gain of 20 11: Gain of 40

7 Decay Modes

The DRV8711 supports four different decay modes: slow, fast, mixed, and auto mixed. The current through the motor windings is regulated using an adjustable fixed-time-off scheme. This means that after any drive phase, when a motor winding current has hit the current chopping threshold (I_{TRIP}), the DRV8711 will place the winding in one of the four decay modes for TOFF. After TOFF, a new drive phase starts.

If there is a desired PWM chopping frequency, f_{PWM}, use Equation 8. Note that this will only ensure that the minimum PWM frequency is f_{PWM}, since the drive time may be longer than TBLANK.

$$\text{TBLANK} + \text{TOFF} + (2 \times \text{DTIME}) \approx 1/f_{PWM} \text{ (Hz)} \quad (8)$$

If there is no target f_{PWM}, the best way to choose TBLANK and TOFF is to tune the DRV8711 in-system based on the chosen decay mode.

In most applications, it is recommended to use auto mixed decay. This decay mode eliminates some of the disadvantages of the other decay modes when the motor is stopped.

TOFF defines the time that the device is in the defined decay mode.

OFF Register Address = 0x02h

Bit	Name	Size	R/W	Default	Description
7-0	TOFF	8	R/W	0x30h	Sets fixed off time, in increments of 500 ns 0x00h: 500 ns 0xFFh: 128 µs

TBLANK defines the minimum drive time for the PWM current chopping. I_{TRIP} is ignored during TBLANK, so the winding current may overshoot the trip level. In auto mixed decay, TBLANK also sets the fast decay time.

BLANK Register Address = 0x00h

Bit	Name	Size	R/W	Default	Description
7-0	TBLANK	8	R/W	0x80h	Sets current trip blanking time, in increments of 20ns 0x00h: 1.00 µs … 0x32h: 1.00 µs 0x33h: 1.02 µs … 0xFEh: 5.10 µs 0xFFh: 5.12 µs

If the application requires a high degree of microstepping (n_m = 64, 128, or 256), it is recommended to set the ABT bit. This enables adaptive blanking time, which will cut the blanking time in half for small current steps. Adaptive blanking time allows for more accurate current control at these lower current steps.

BLANK Register Address = 0x03h

Bit	Name	Size	R/W	Default	Description
8	ABT	1	R/W	0	*0: Disable adaptive blanking time* 1: Enable adaptive blanking time

Figure 3 describes each of the three decay modes.

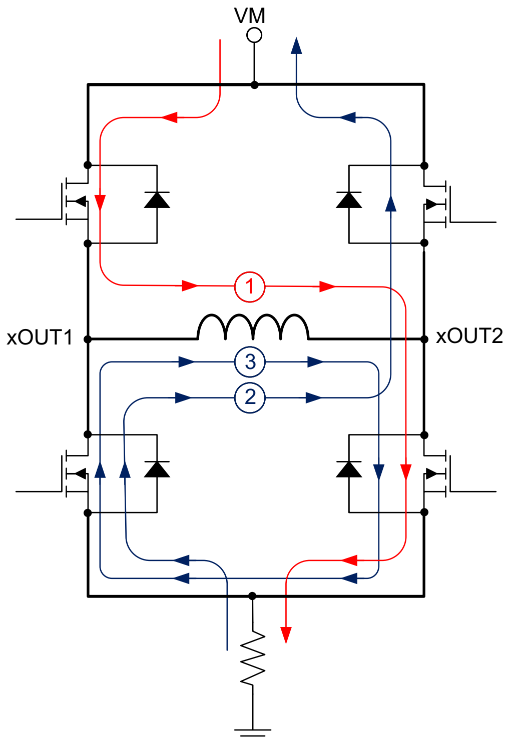

Figure 3. Decay Modes

For the diagrams shown in Figure 4 through Figure 7, the red (solid) lines indicate drive phase current and the blue (dashed) lines indicate decay mode current. When tuning the DRV8711 operation, it is best to try out the settings for DECMOD to see which works best for the application. It also may be beneficial to use one decay mode for operation and a second decay mode when holding.

In slow decay, the winding current is recirculated in both of the low side FETs. This results in the current decreasing very slowly. However, in slow decay the back EMF is shorted, which can cause the motor speed to decrease very rapidly during TOFF.

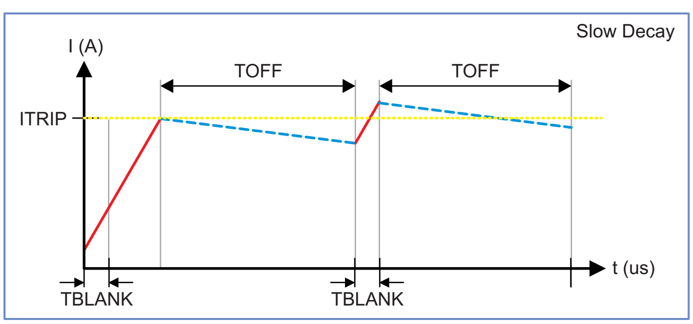

Figure 4. Slow Decay

In fast decay, H-bridge is reversed to rapidly decrease the motor winding current. The motor speed does not decrease rapidly as compared to slow decay. If the current approaches zero, then the H-bridge is turned off so that the current will never begin flowing in the reverse direction. Note that in Figure 5, the current is shown to decrease to zero, and the H-bridge is deactivated. This will not happen in the system if TOFF is not very long.

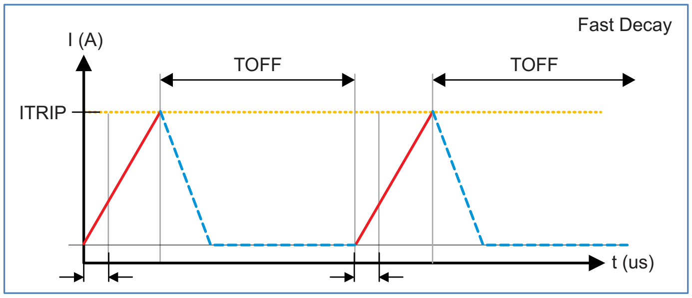

Figure 5. Fast Decay

Mixed decay begins as fast decay, but switches to slow decay after a period of TDECAY for the remainder of TOFF.

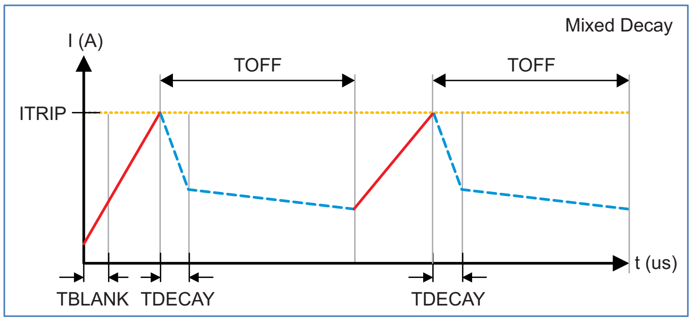

Figure 6. Mixed Decay

In auto mixed decay, current is sampled at the end of the blanking time. If the current is less than I_{TRIP}, the current is allowed to increase to I_{TRIP}. Afterwards, slow decay is used. If the current is greater than I_{TRIP} after the blanking time, fast decay is used for a period of TBLANK, followed by slow decay for the remainder of TOFF.

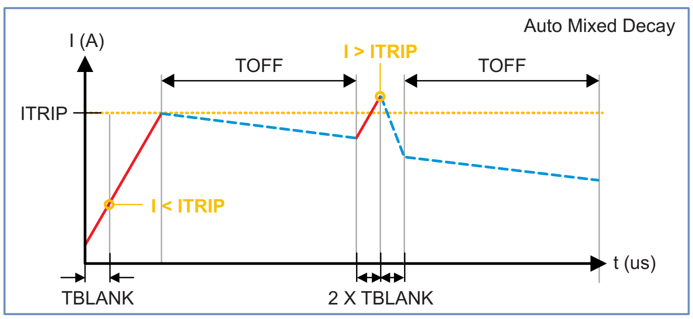

Figure 7. Auto Mixed Decay

During microstepping, current can be either increasing or decreasing from one step to the next. Fast decay can be very useful when I_{TRIP} is decreasing, because it allows the winding current to decay very rapidly and settle at the next step. Slow decay is used often because the current decays slowly and results in a lower current ripple versus fast decay. Mixed decay and auto mixed decay allow flexibility to have the advantages of both fast decay and slow decay in the same mode.

DECAY Register Address = 0x04h

Bit	Name	Size	R/W	Default	Description
10-8	DECMOD	3	R/W	001	000: Force slow decay at all times *001: Slow decay for increasing current, mixed decay for decreasing current (indexer mode only)* 010: Force fast decay at all times 011: Use mixed decay at all times 100: Slow decay for increasing current, auto mixed decay for decreasing current (indexer mode only) 101: Use auto mixed decay at all times

8 Overcurrent Protection

In the DRV8711, current is sensed by measuring the voltage (V_{DS}) across the external FETs during the drive phase. If the voltage across any FET is measured greater than OCPTH for longer than the time specified by OCPDEG, the driver is disabled and the nFAULT pin is pulled low. In order to calculate the current needed to trip OCP, use the OCPTH value and the FET $R_{DS(ON)}$:

$$I_{OCP} = \frac{OCPTH}{R_{DS(ON)}(\Omega)} \tag{9}$$

If the motor winding parasitic capacitance, C_L, is very large (on the order of 1 µF), then it may be required to increase OCPDEG to account for the large inrush current. For C_L less than 10 nF, the default value for this register should be sufficient.

DRIVE Register Address = 0x06h

Bit	Name	Size	R/W	Default	Description
1-0	OCPTH	2	R/W	00	OCP threshold *00: 250 mV* 01: 500 mV 10: 750 mV 11: 1000 mV
3-2	OCPDEG	2	R/W	10	OCP deglitch time 00: 1 µs *01: 2 µs* 10: 4 µs 11: 8 µs

9 Stall Detect

The DRV8711 implements an internal stall detect scheme that monitors the back-EMF when in microstep mode. During each zero current step of either H-bridge, the BEMF voltage is sampled and held on the BEMF pin. The sampling occurs after SMPLTH during this zero current step. An internal divider VDIV can be configured to scale the BEMF.

The stall detection logic in the DRV8711 indicates that a stall has been detected and can be ignored, if desired. The stall detection does not change the operation of the DRV8711 in any way. It is up to the host to determine the appropriate action.

Stall detection works properly if the stepper motor is spinning fast enough to generate a detectable BEMF. In addition, the time given by SMPLTH is required to take the sample. As a result, BEMF detection may not work with high stepping speeds (generally at high microstepping levels) or very low motor velocities.

If desired, the STALLn/BEMFn pin can be configured to notify the host processor when the BEMF sample is ready on the BEMF pin. This allows the host to measure the back-EMF and perform external stall-detect or other algorithms if necessary.

If internal stall detect is selected, the STALLn/BEMFn pin is pulled low whenever a stall event is detected.

After the BEMF is sampled, it is compared to an adjustable threshold SDTHR. If the sampled BEMF falls below SDTHR for a given number of steps (SDCNT), a stall event is detected.

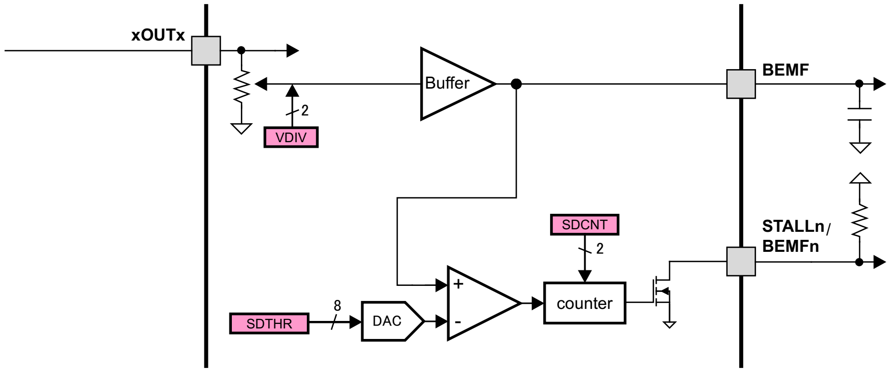

Figure 8. Stall Detect Block Diagram

The best way to configure internal stall detect is by selecting a desired stall speed (in rpm). Set both SDTHR and VDIV to their minimum values. Next, decrease the motor speed to the desired stall detect speed. Use Equation 10 to determine the necessary stepping frequency:

$$f_{step}(steps / sec) = \frac{v(rpm) \times n_m(steps) \times 6}{\theta_{step}(° / step)} \quad (10)$$

Now that the motor is spinning more slowly, increase SDTHR, or VDIV, or both SDTHR and VDIV until STALLn/BEMFn are asserted. Increasing either SDTHR or VDIV will make the stall detect trip at higher speeds. Set SDCNT so that the stall detect will trip after the desired number of steps.

CTRL Register **Address = 0x00h**

Bit	Name	Size	R/W	Default	Description
7	EXSTALL	1	R/W	0	*0: Internal stall detect* 1: External stall detect

TORQUE Register **Address = 0x01h**

Bit	Name	Size	R/W	Default	Description
10-8	SMPLTH	3	R/W	001	Back EMF sample threshold 000: 50 µs *001: 100 µs* 010: 200 µs 011: 300 µs 100: 400 µs 101: 600 µs 110: 800 µs 111: 1000 µs

STALL Register **Address = 0x05h**

Bit	Name	Size	R/W	Default	Description
7-0	SDTHR	8	R/W	0x40h	Sets stall detect threshold The correct setting needs to be determined experimentally
9-8	SDCNT	2	R/W	00	*00: STALLn asserted on first step with back EMF below SDTHR* 01: STALLn asserted after 2 steps 10: STALLn asserted after 4 steps 11: STALLn asserted after 8 steps
11-10	VDIV	2	R/W	00	*00: Back EMF is divided by 32* 01: Back EMF is divided by 16 10: Back EMF is divided by 8 11: Back EMF is divided by 4

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