

## Lab 5a

- State transition table is basically a truth table showing the functionality of a circuit based on a given present state.
- Present state are like a truth table's inputs and Next state are similar to a truth table's outputs
- A state transition diagram is a web-like diagram that shows how states proceed from one to the next



- A state machine needs two elements to function. A memory element to hold current state and some way to determine the next state. With Flip-Flops we have two such elements.
- Registers are constructed using one or more Flip-Flops that share common signal (such as clock)
- Reg is used for updated always outputs

current state  
& set of static  
logic gates



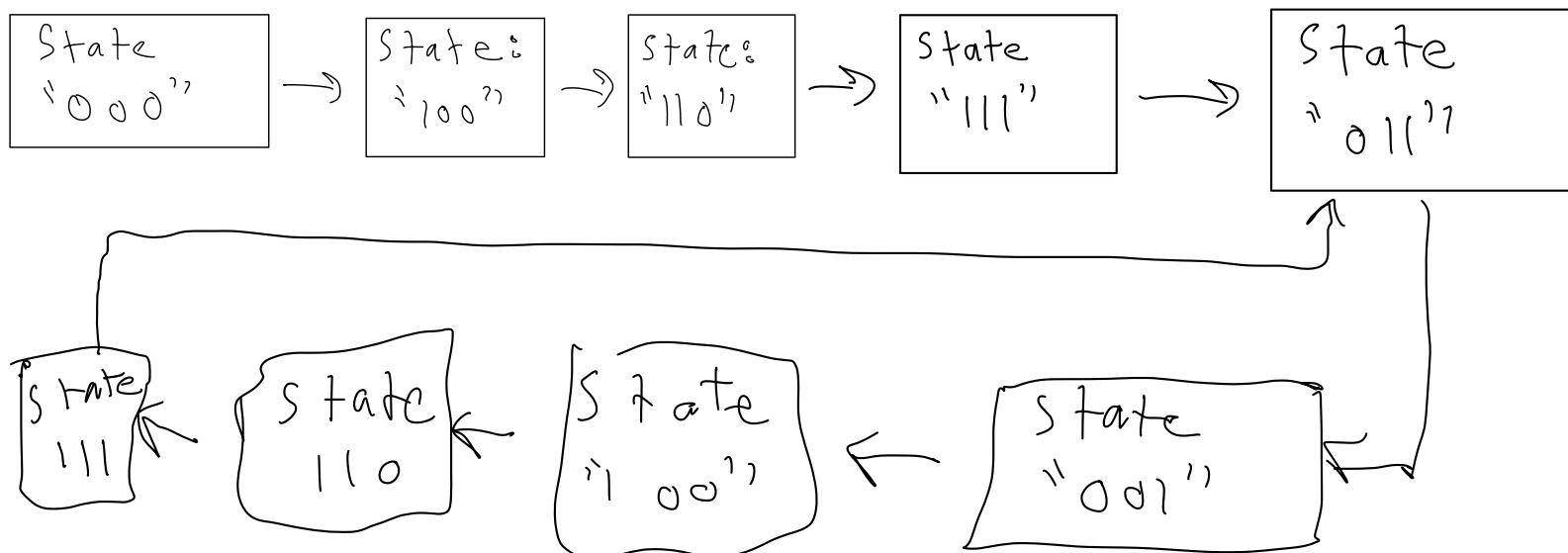
# PRE LAB

I  
Table 1: Pre-Lab Transition Table

PRESENT STATE (Inputs)			NEXT STATE (Outputs)		
A	B	C	NextA	NextB	NextC
0	0	0	1	0	0
0	0	1	1	0	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	1	1

$$Q = J Q' + K' Q$$

Transition Diagram



Next A k-map  $\Sigma m(0,1,2,4,5,6)$

BC \ A		0	1
0	0	1	1
0	1	1	1
1	1	0	0
1	0	1	1

$\overline{B}$  (points to the top two rows)  
 $\overline{C}$  (points to the left two columns)

$$F_{NA} = \overline{B} + \overline{C}$$

Next B k-map  $\Sigma m(4,5,6,7)$

BC \ A		0	1
0	0	0	1
0	1	0	1
1	1	0	1
1	0	0	1

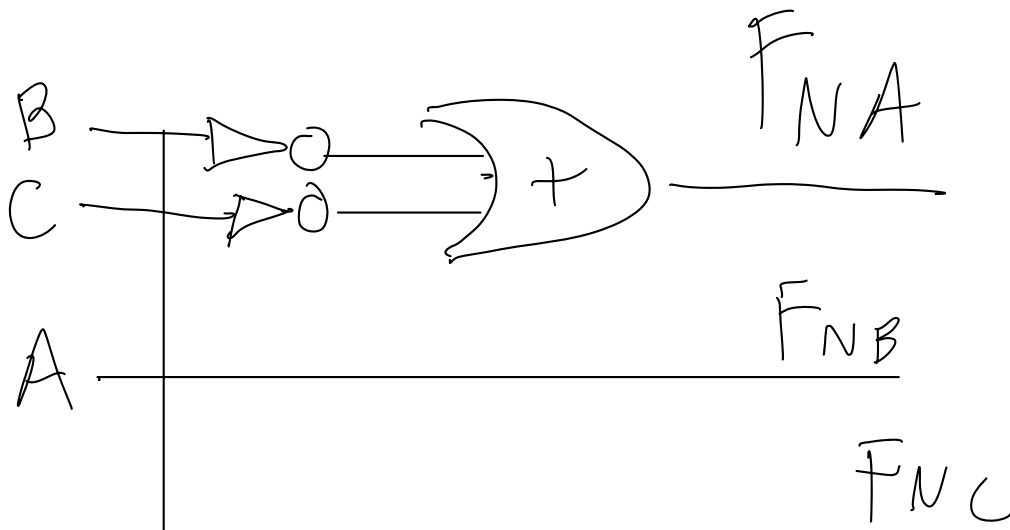
$A$  (points to the right column)  
 $F_{NB} = A$

Next C k-map  $\Sigma m(2,3,6,7)$

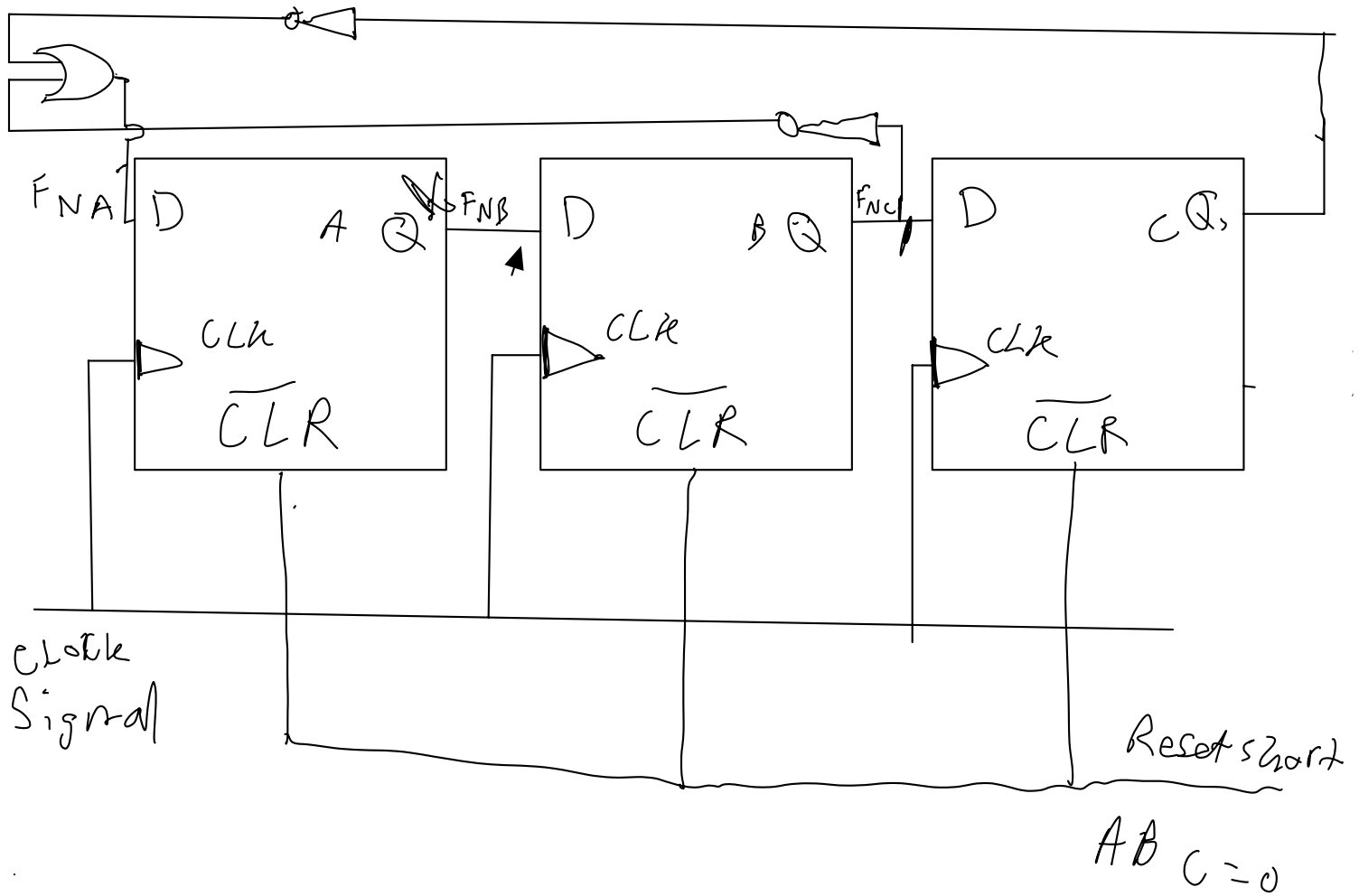
$\overline{B}C \backslash A$	0	1
00	0	0
01	0	0
11	1	1
10	1	1

$$F_{NC} = B$$

## Combination Logic Design



# Schematic



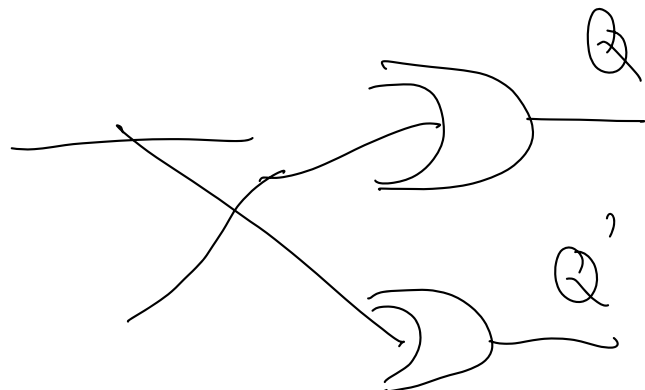
DAF



in D  
in CLK  
in QST  
out Q

assign

$\bar{D} \cdot CL$



$$\bar{D} \cdot (CLK) + Q$$

D

clk

NRST

Explain what happening

clk

RESET

↑ whenever  
1 all is zero  
ABC

A

B

C

whenever CLK rises  
that is when if sends  
a signal to A, then B,  
then C