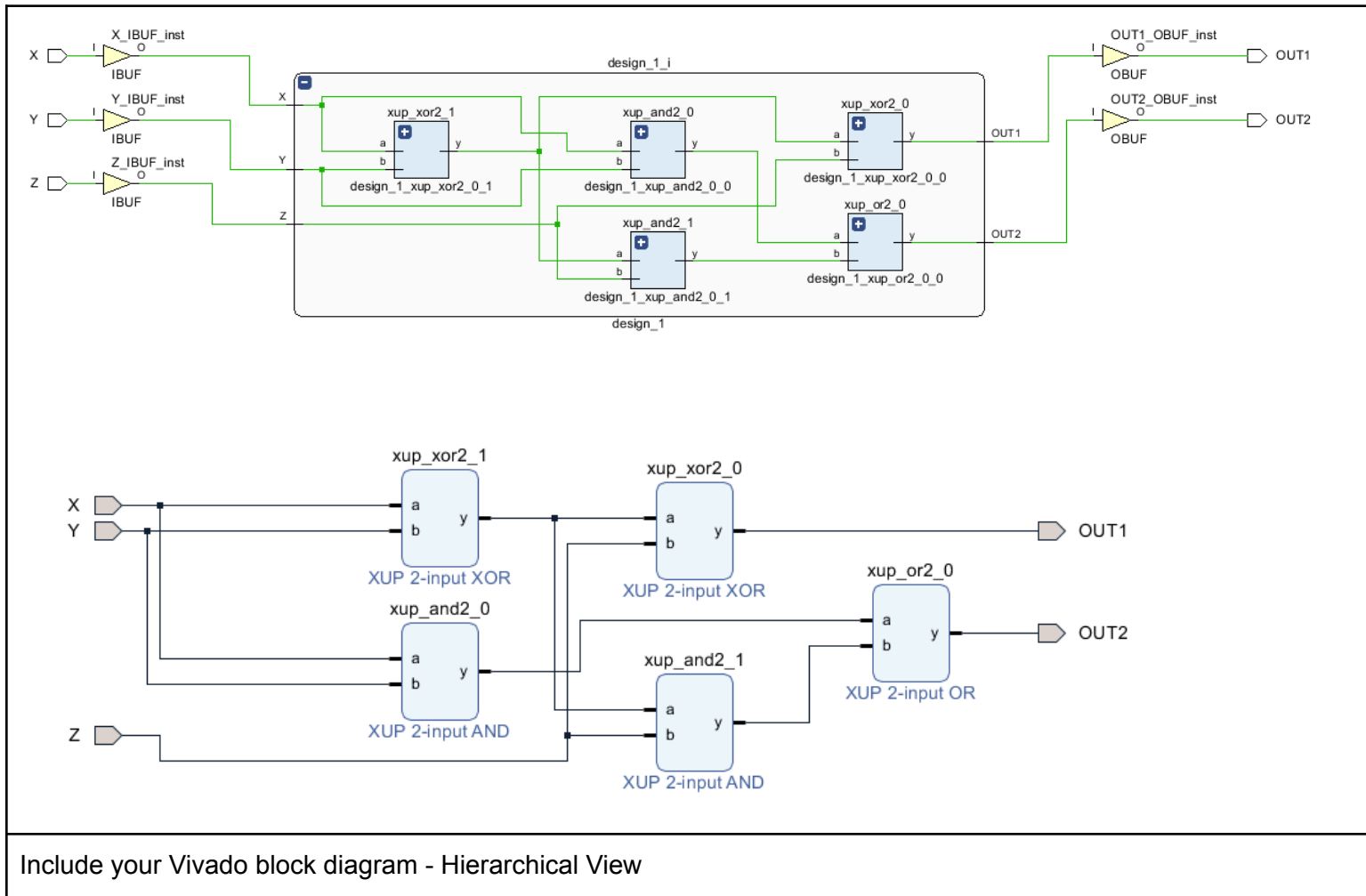


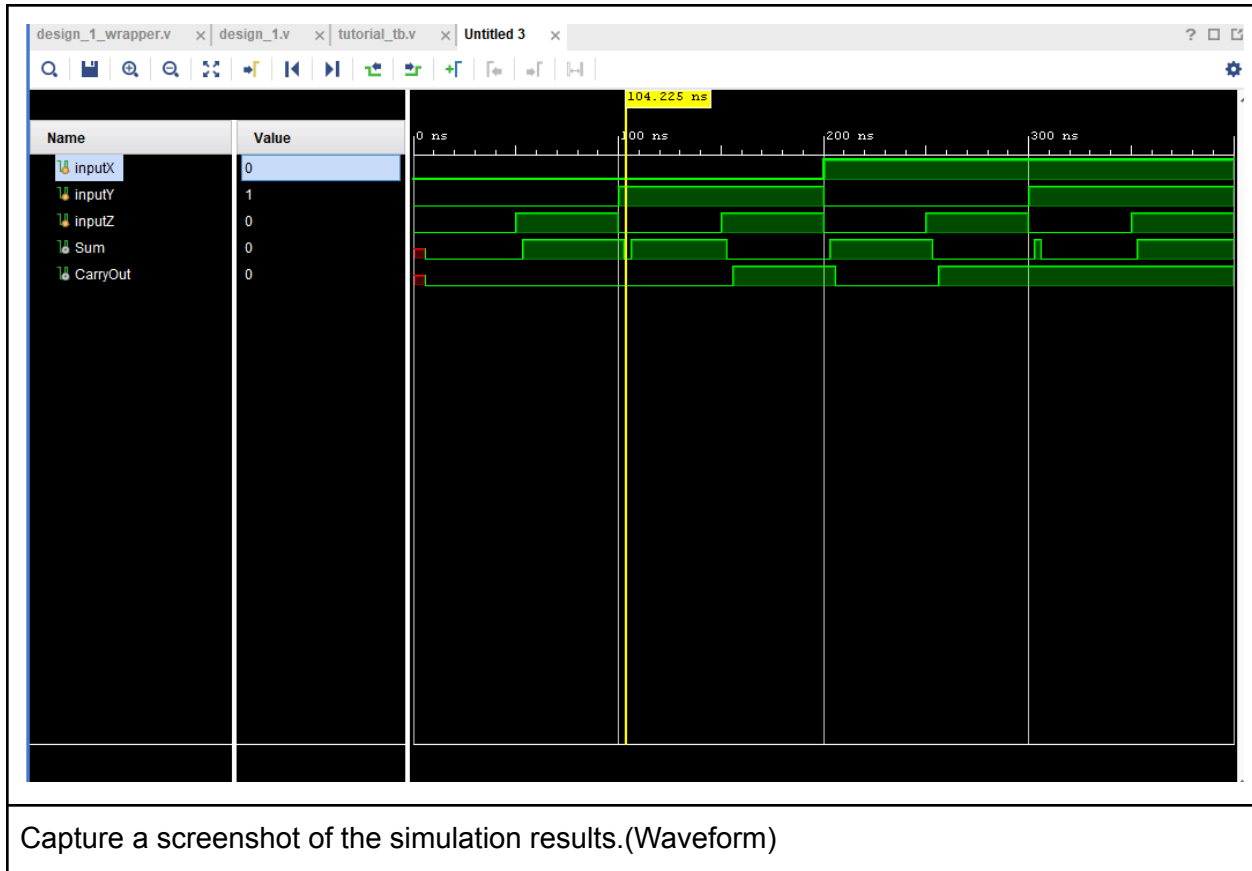
Name: Danyal Falsafi

Section: 02

X500: falsa003

## Lab 1a:





```
`timescale 1ns / 1ps
////////////////////////////////////////////////////////////////
// Module Name: tutorial_tb
////////////////////////////////////////////////////////////////

module tutorial_tb(
);
reg inputX, inputY, inputZ;
wire Sum;
wire CarryOut;
design_1_wrapper Instance_1_of_Adder(
    .X(inputX),
    .Y(inputY),
    .Z(inputZ),
    .OUT1(Sum),
    .OUT2(CarryOut));
initial
begin
    inputX = 0; inputY = 0; inputZ = 0;
    #50
    inputX = 0; inputY = 0; inputZ = 1;
    #50
    inputX = 0; inputY = 1; inputZ = 0;
    #50
    inputX = 0; inputY = 1; inputZ = 1;
    #50
    inputX = 1; inputY = 0; inputZ = 0;
    #50
    inputX = 1; inputY = 0; inputZ = 1;
    #50
    inputX = 1; inputY = 1; inputZ = 0;
    #50
    inputX = 1; inputY = 1; inputZ = 1;
end
endmodule
```

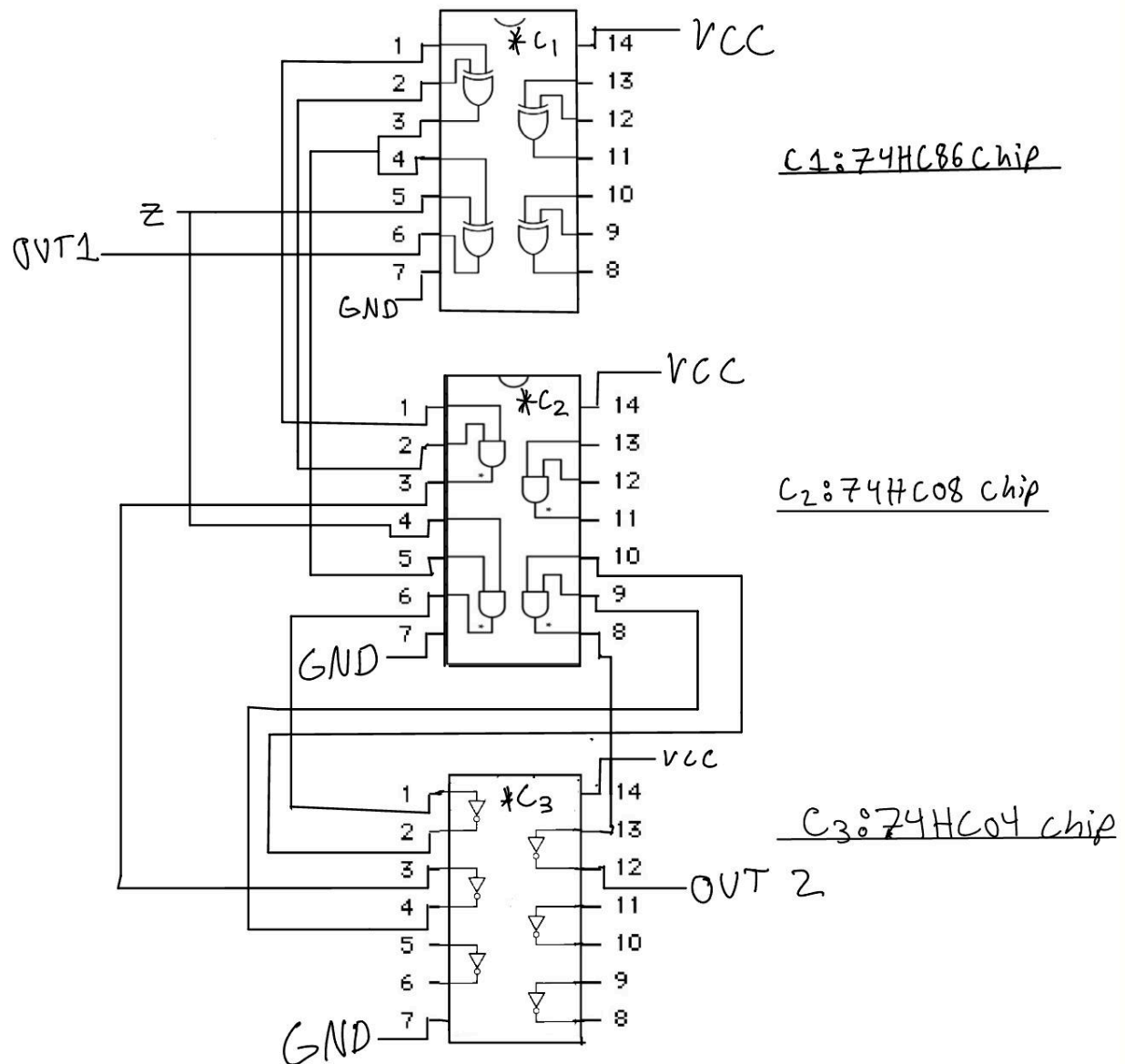
Include a copy of your testbench file text. (Delete all unnecessary lines)

X	Y	Z	SUM	CARRYOUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

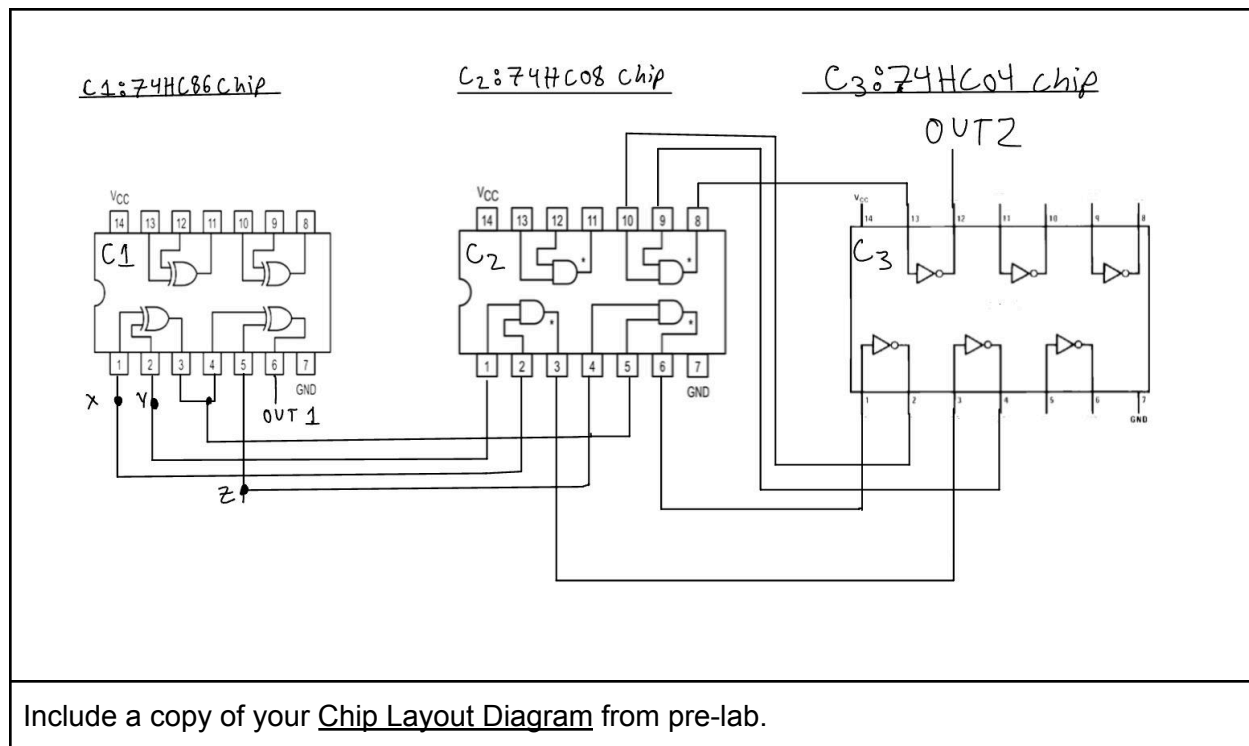
Include a typed copy of the truth table that you filled out above.

---

## **Lab 1b:**



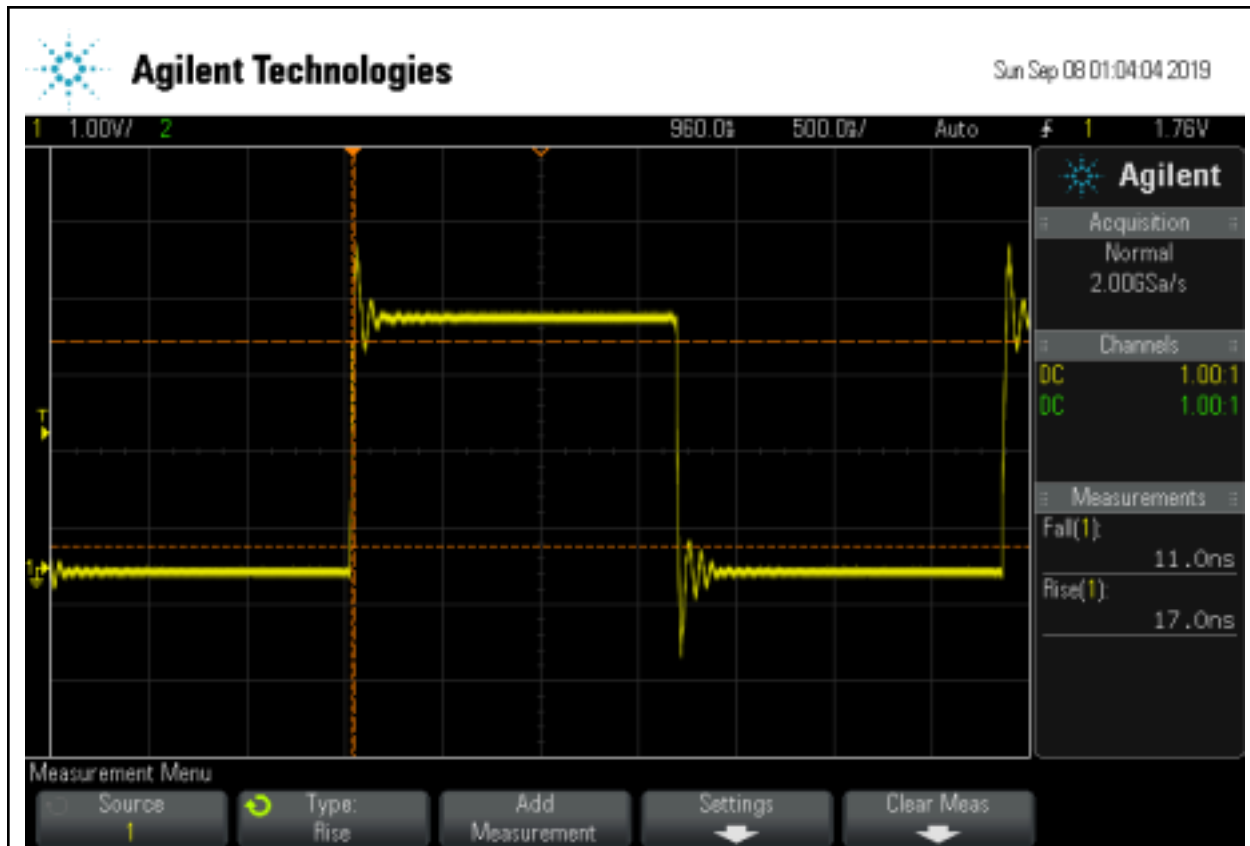
Include a copy of your Logic Diagram from pre-lab.



X	Y	Z	SUM	CARRYOUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Include a typed copy of the truth table that you filled out above.

## Lab 1c:

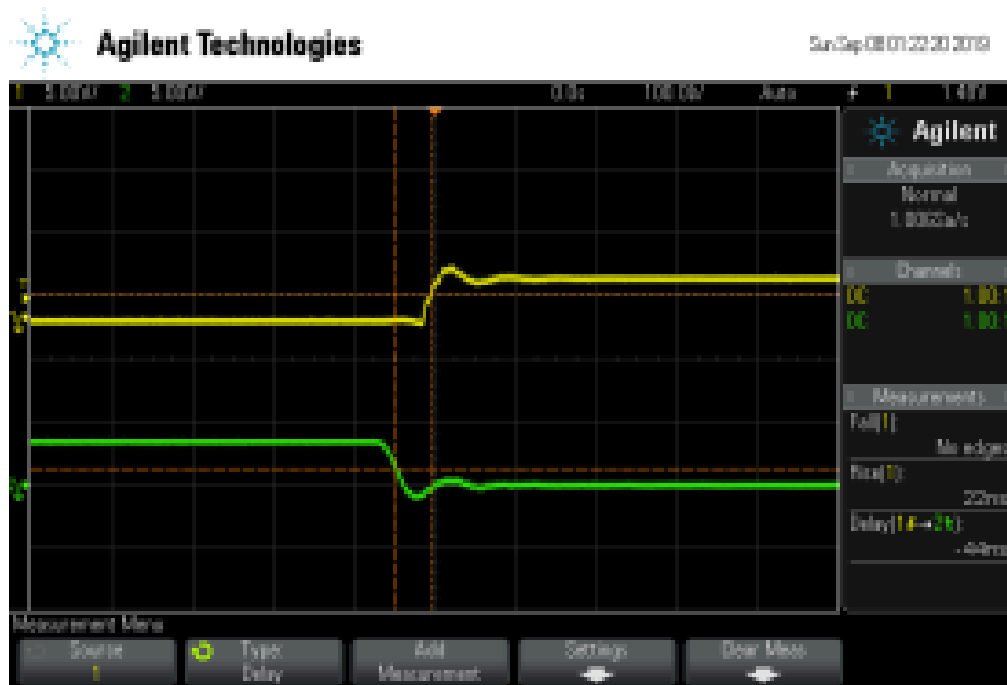


Include a copy the Waveform showing Rise Time and Fall Time Measurements captured.

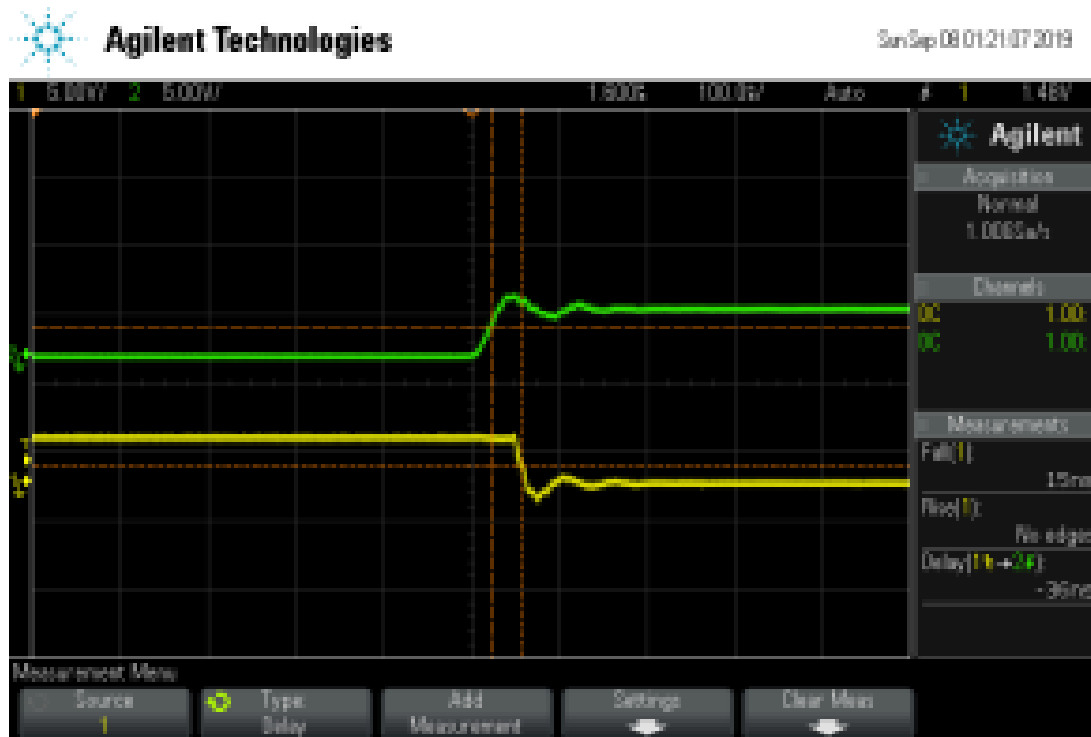


Note: Green line = input signal, Yellow line = output signal.  
The below images show the propagation delay of the input as it travels through 3 NAND gates which are arranged to behave as an inverter.

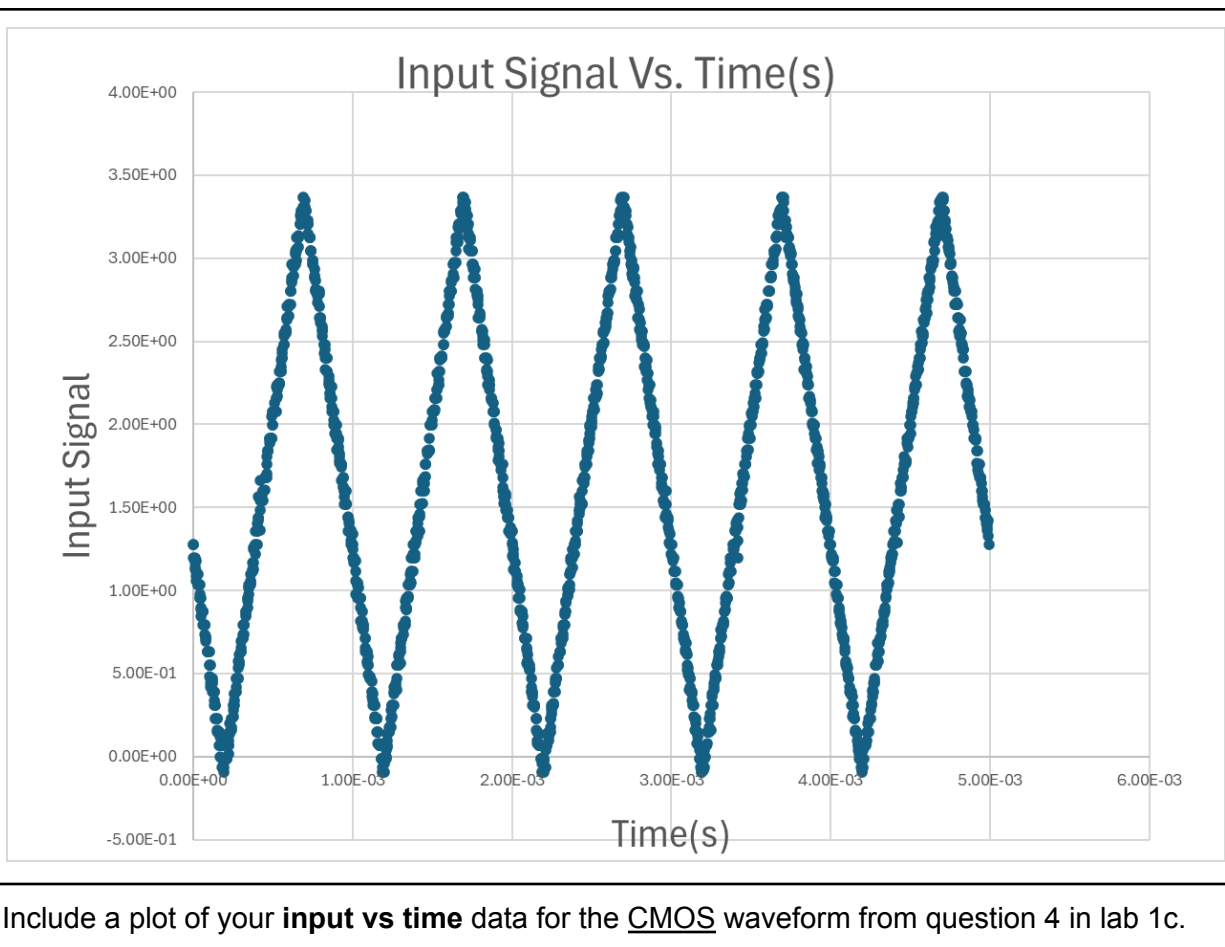
Falling input and rising output delay:

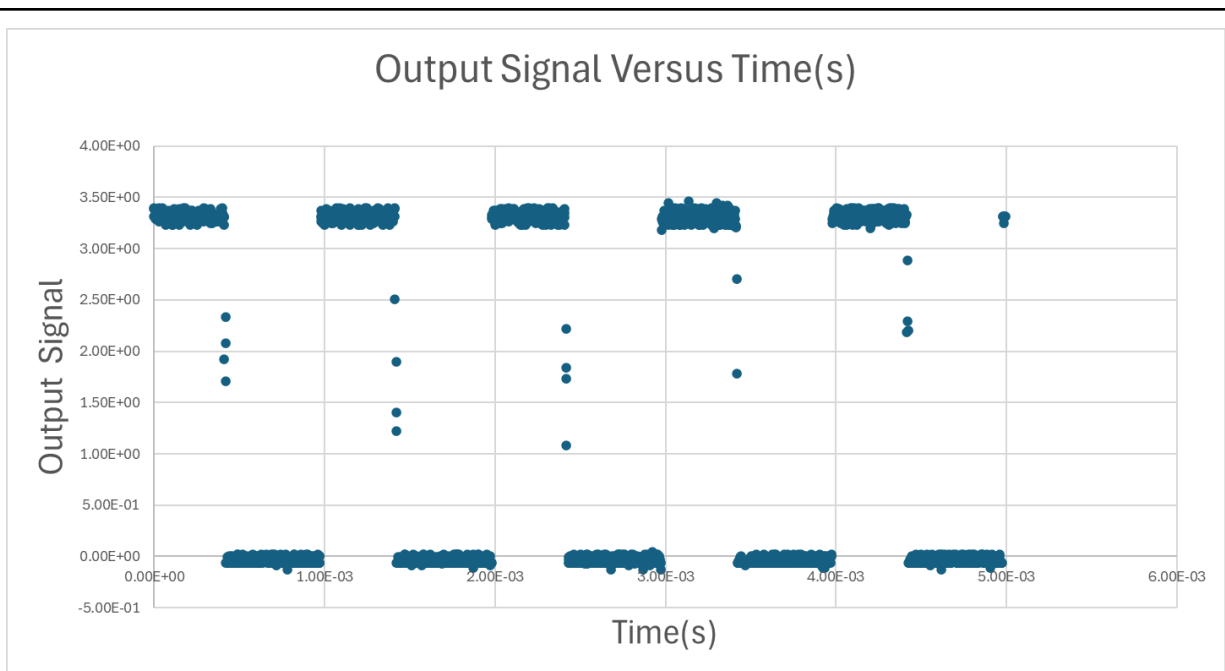


Rising input and falling output delay:

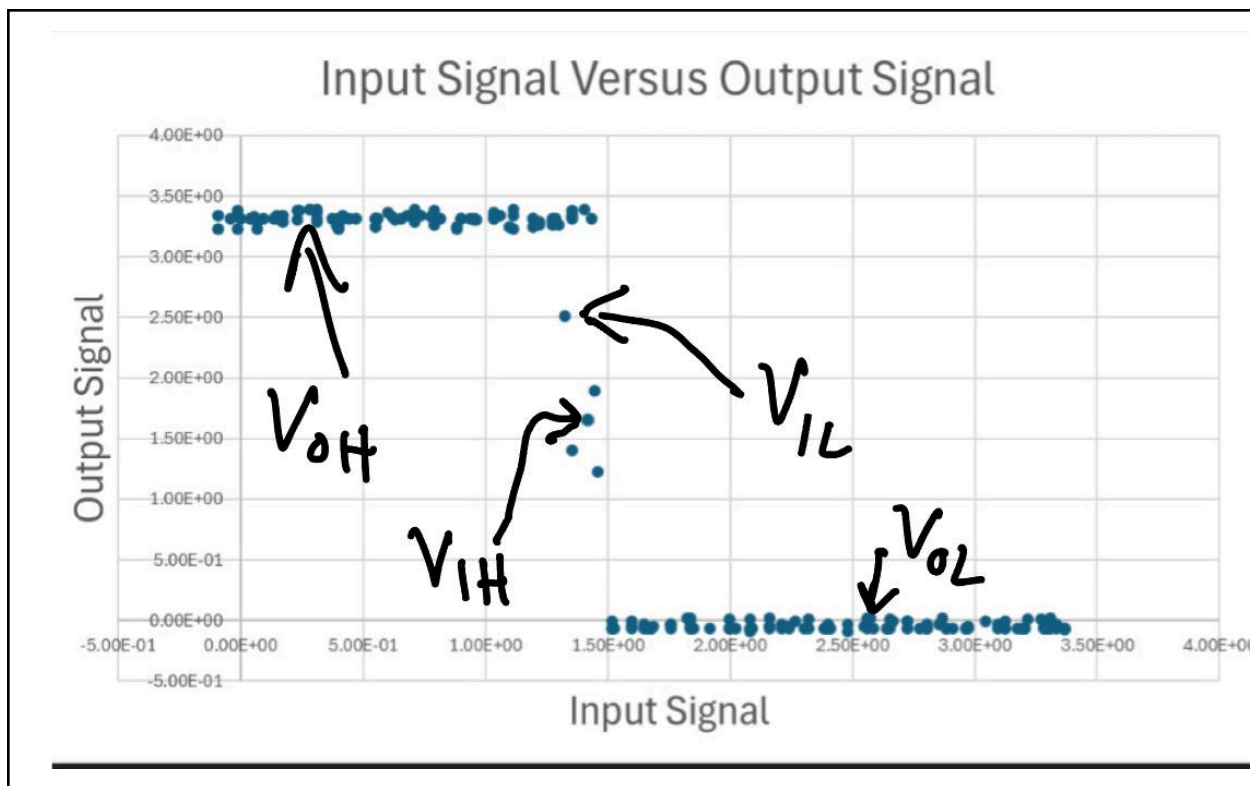


Include a copy of your waveform showing the Propagation Delay Measurements captured. Zoom in to show the associated (rising/falling) edges and cursors.





Include a plot of your **output vs time** data for the CMOS waveform from question 4 in lab 1c.



Include a plot of your **output vs input** data for the CMOS waveform from question 4 in lab 1c.

Make sure you Locate the  $V_{IH}$ ,  $V_{IL}$ ,  $V_{OH}$  and  $V_{OL}$  on this graph. [Located above]

\* Note that the Output vs. Input graph above is that of an inverter:

- When the input signal is read as HIGH, the output will be read to be LOW.
- When the input signal is read as LOW, the output will be read to be HIGH.

**Measurements of above graph:**

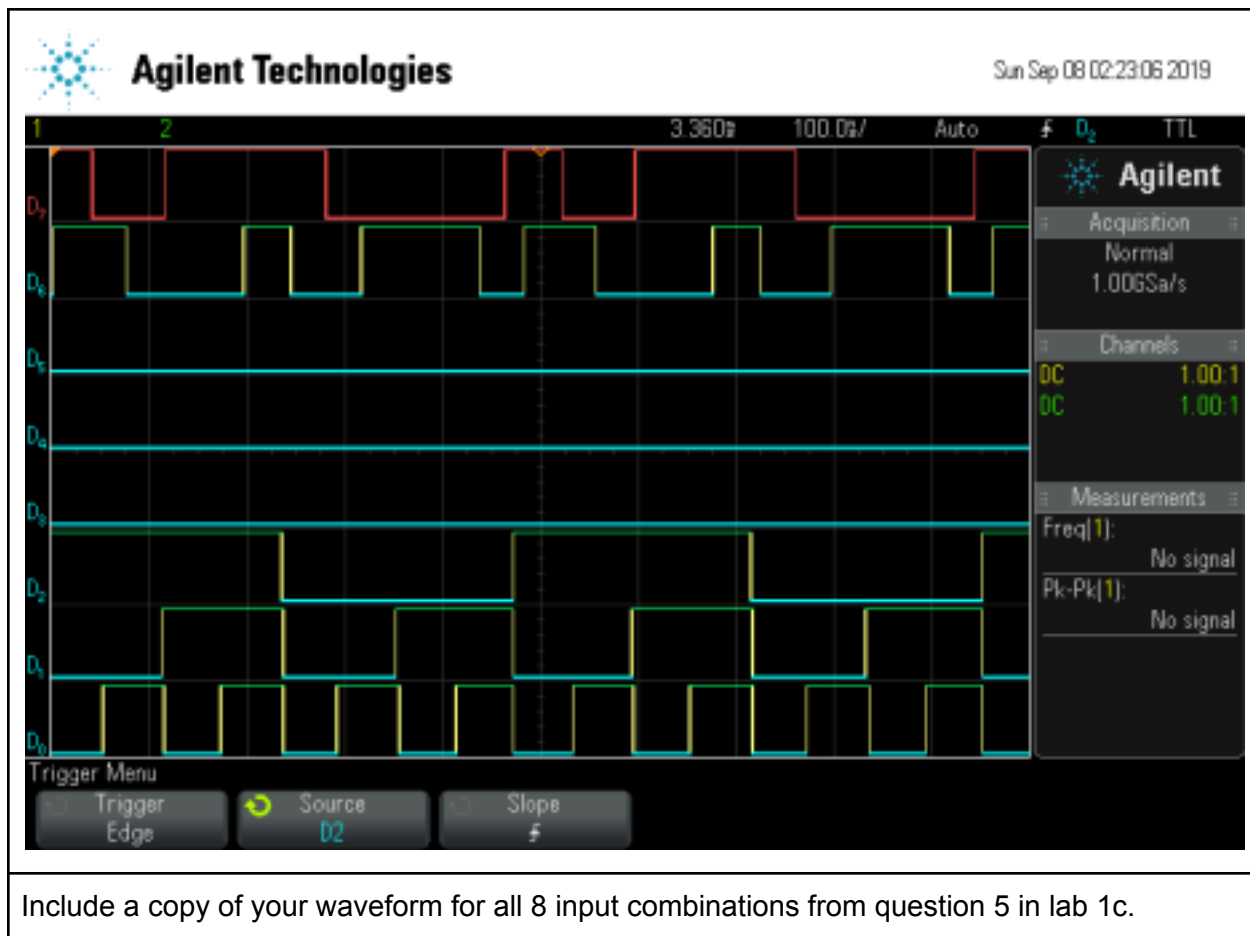
- $V_{IH} = 1.517 \text{ V}$  [Minimum voltage input that will be recognized as a HIGH input for the output signal to be considered LOW, which is anything downwards of approximately 0.4V.]
- $V_{OH} = 3.303 \text{ V}$  [Minimum voltage that could occur on the output of a gate to achieve a HIGH voltage output signal]
- $V_{IL} = 1.326 \text{ V}$  [Maximum input voltage that will be interpreted as a LOW input—i.e. the output is still considered HIGH, which is anything upwards of approximately 2.4V.]
- $V_{OL} = 0.007 \text{ V}$  [Maximum voltage that could occur on the output of a gate for achieving a LOW output signal]

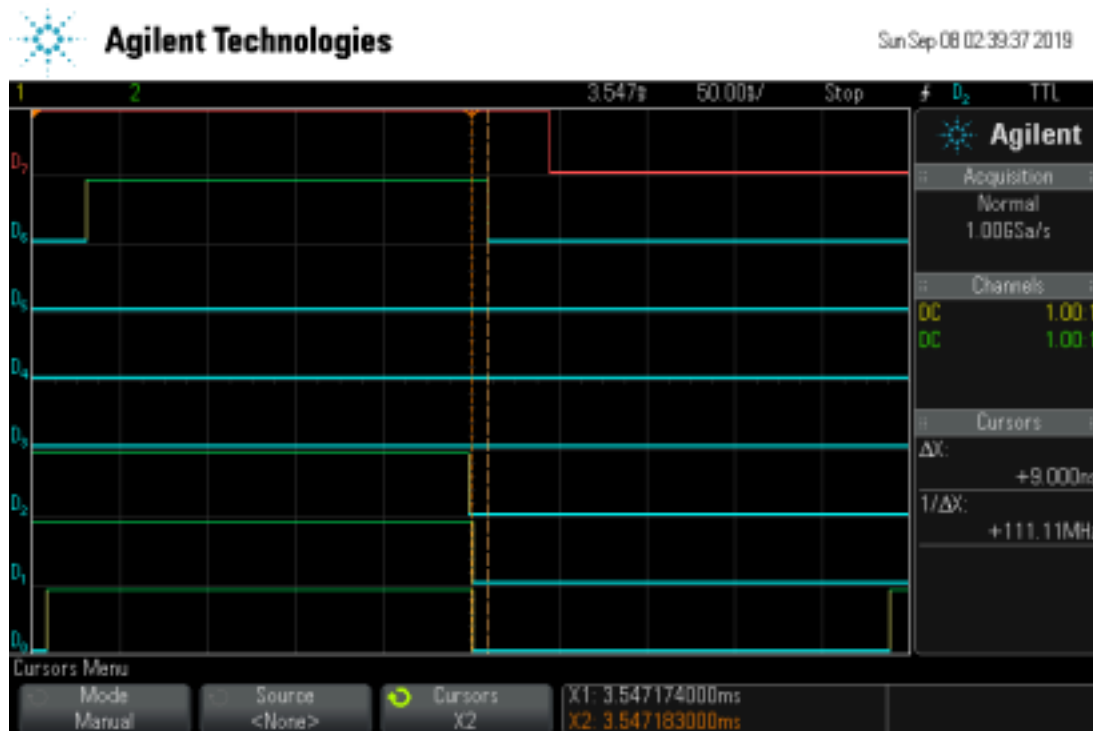
**Calculate the  $NM_H$  and  $NM_L$  using these values.**

$$NM_H = V_{OH} - V_{IH} = (3.303 \text{ V}) - (1.517 \text{ V}) = 1.786 \text{ V}$$

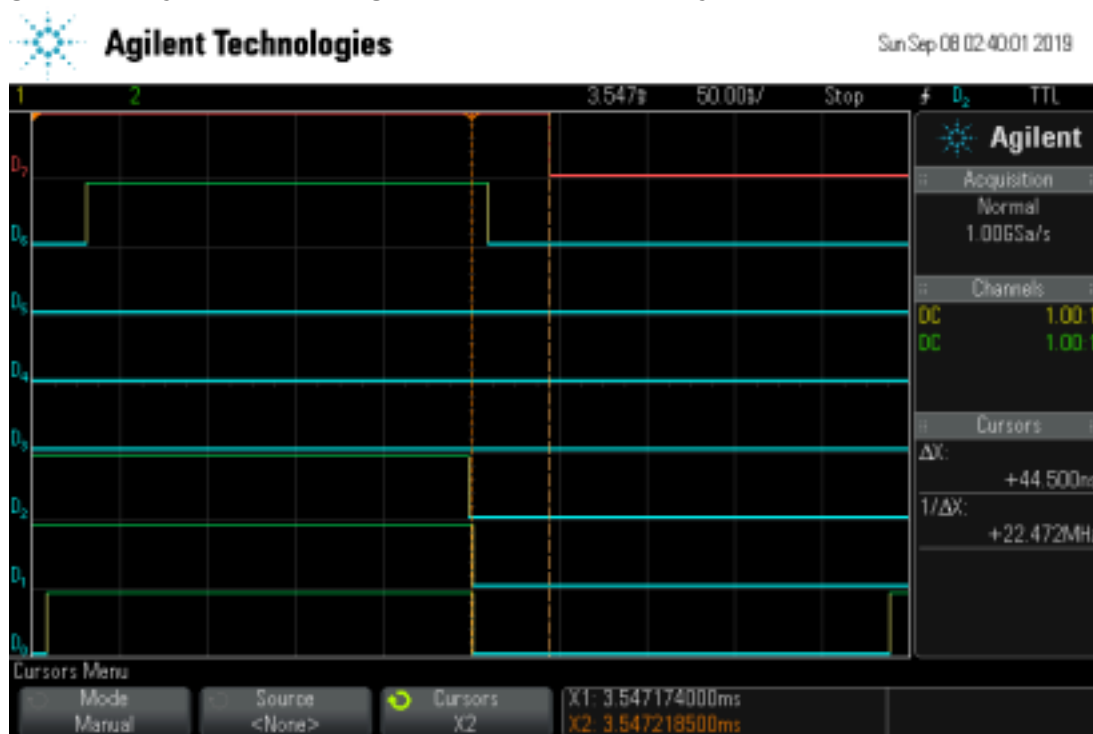
$$NM_L = V_{IL} - V_{OL} = (1.326 \text{ V}) - (0.007 \text{ V}) = 1.319 \text{ V}$$

$$\text{Noise margin} = \min(NM_L, NM_H) = 1.319 \text{ V}$$





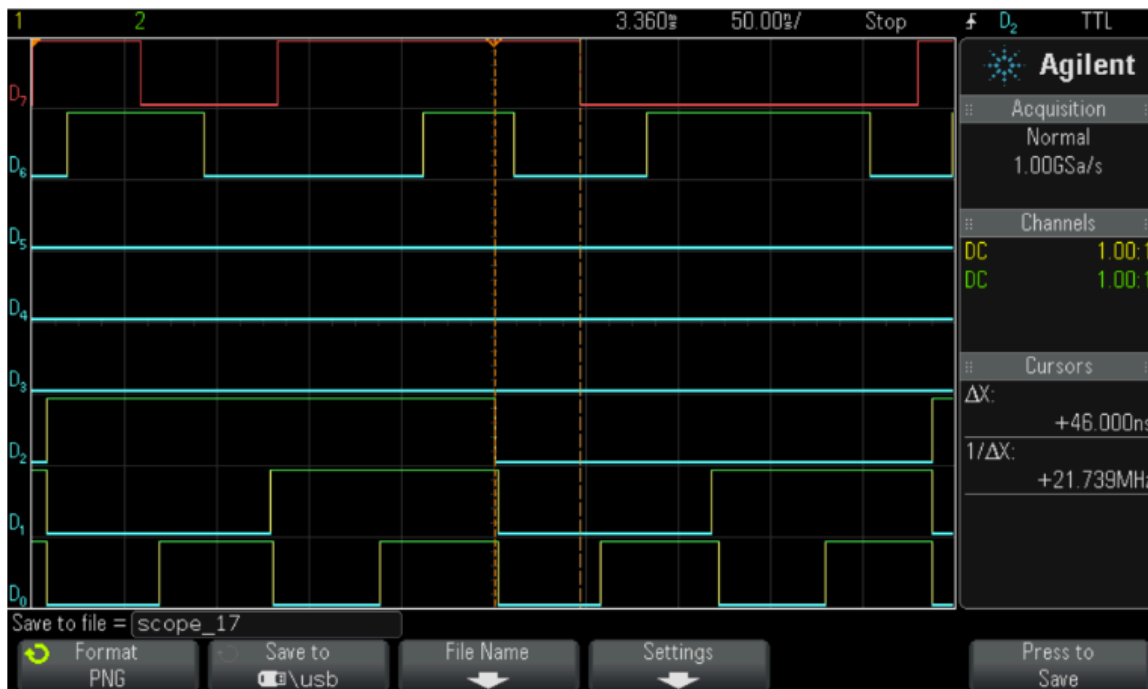
Propagation delay of OUTPUT2 given an input frequency of  $2^{22}$  Hz:



Propagation delay of OUTPUT1 given an input frequency of  $2^{24}$  Hz:



Propagation delay of OUTPUT2 given an input frequency of  $2^{24}$  Hz:





Include a copy of your propagation delay measurement from question 5 in lab 1c.

“You have to place cursors manually for the digital signals and see the  $\Delta(x)$  for the Propagation Delay”