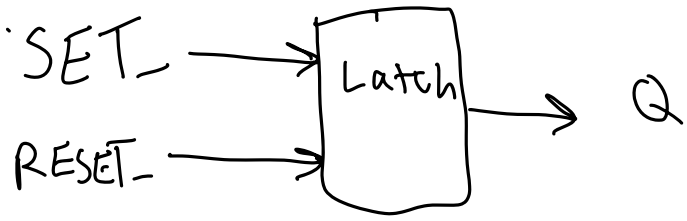
Lab 4 Pre Lab

1)



$\overline{SET}$ — SET_ = 0, out(Q) hight

SET_	RESET_	Q	$Q^+ = Q(n+1)$
Low (Q forced high)	Low (Q forced low)	Unkown	
High (Q forced low)	High (Q forced high)	Q (unchanged)	

- gated S-R Latch reduces sensitivity of outputs to changin inputs
  Clock signal must be high for S-R latch to respond to input signals
- Latch should change only once for each (each) application of the clock
- Main secondary flip flops are a variation of the two phase clock approach for outputs from latches controlly by one phase of clock or another by the other phase of the clock.

- S-R latches improve our rejection of glitches on the inputs, but suffer from draw backs
  - S-R is sensitive to glitches
- D-type latch is either transparent (output follows input) or latched (output is held at the last value input)
- D-type latch makes sure with an inverter that the inputs S & R they gaurantee to not be asserted at the same time, eliminating any invalid inputs

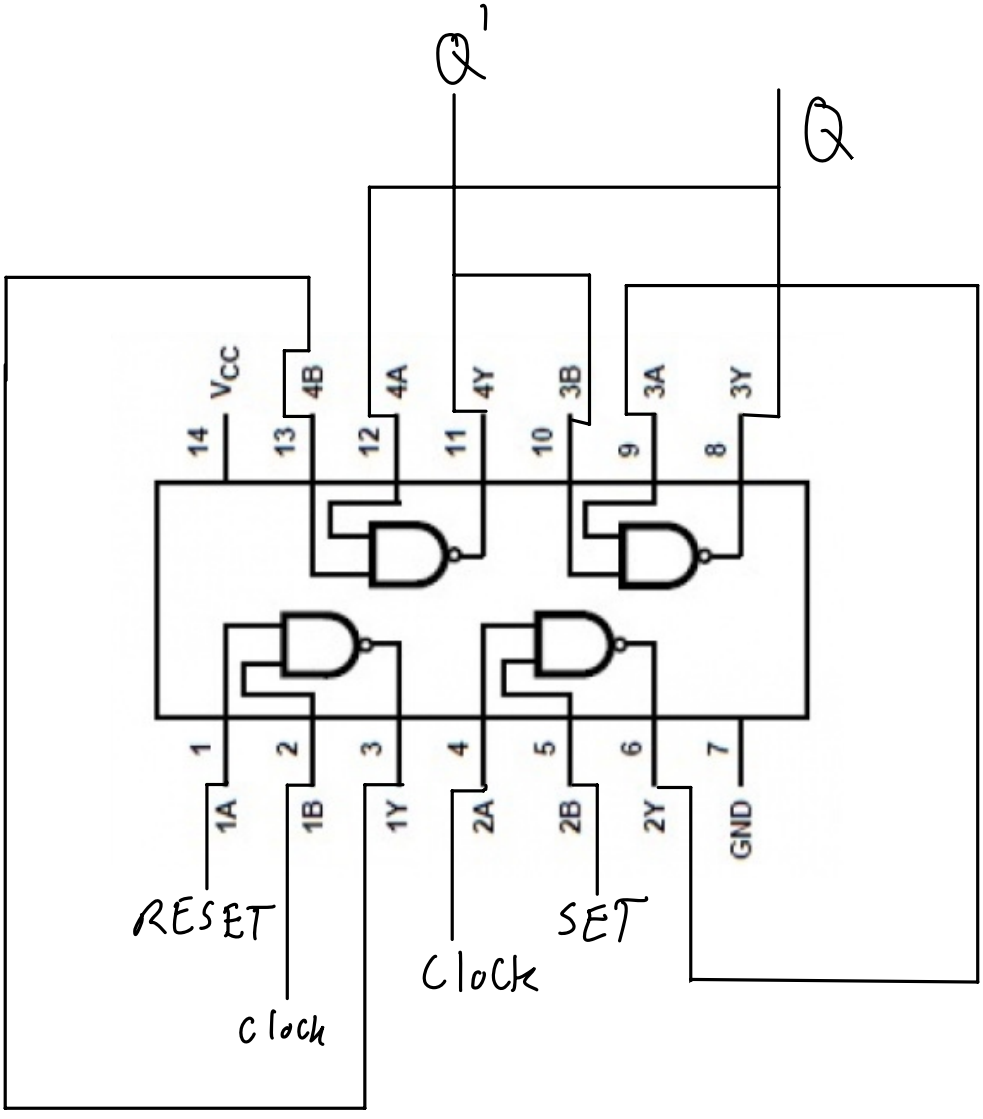
(half clock cycle) gate high

- Flip-Flops [D-type]

(2) a) Should S & R signals be allowed to change while clock (G) is high?

Since this is a gated S-R Latch tends to be less sensitive with the effect changing inputs has on the output. Since clock signal is high the changing S & R signals are allowed to change which the S-R latch responds to those input signals.

b) For a gated S-R latch



Input:

SET $\xrightarrow{PIN1}$ GREEN

RESET $\xrightarrow{PIN2}$ RED

clock $\xrightarrow{PIN3}$ Yellow

output:

Q $\xrightarrow{PIN1}$ purple

Q' $\xrightarrow{PIN2}$ orange

Read lab 1b

bin.

bit files