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University of Minnesota
EE 2301 Introduction to Logic Design Summer 2023

Homework 4

1. Design a synchronous counter to count like 2, 3, 5, 7, 2…… with J-K flip flops.
   Show your results of
   a) Next state table
   b) Karnaugh maps
   c) The resultant flip-flop circuit.

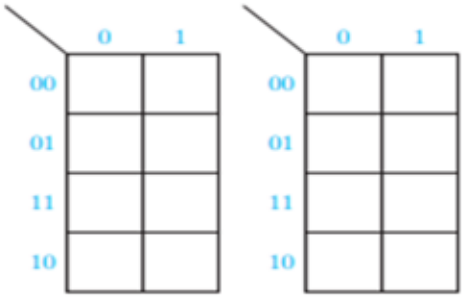
Step 1: State Diagram:

Step 2: Next State Table:

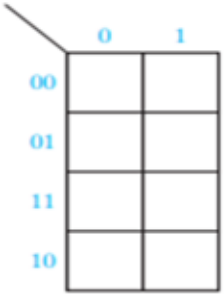
Present state Q_2 Q_1 Q_0	Next state Q_2 Q_1 Q_0	J_2 K_2	J_1 K_1	J_0 K_0

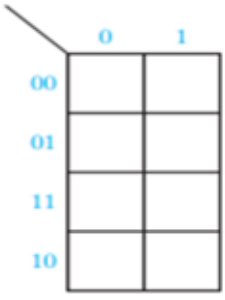
Step 3: Transition Table for the Flip Flop:

Output transition $Q_N \rightarrow Q_{N+1}$	FF inputs J	K
0 → 0	0	X
0 → 1	1	X
1 → 0	X	1
1 → 1	X	0



Step 4: Prepare Karnaugh maps and write the functio





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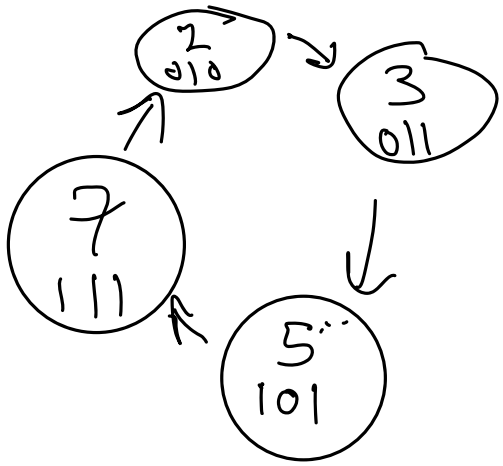
Step 1:

State Diagram:

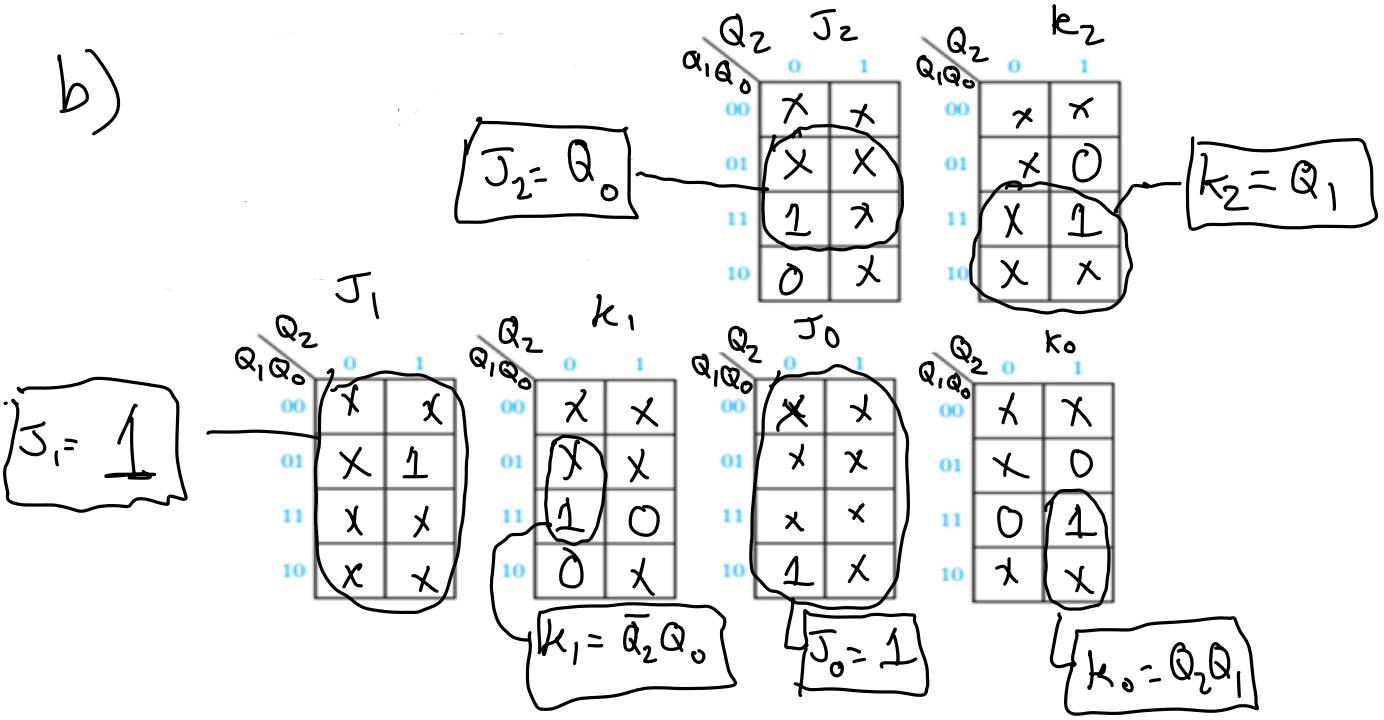


Step 2:

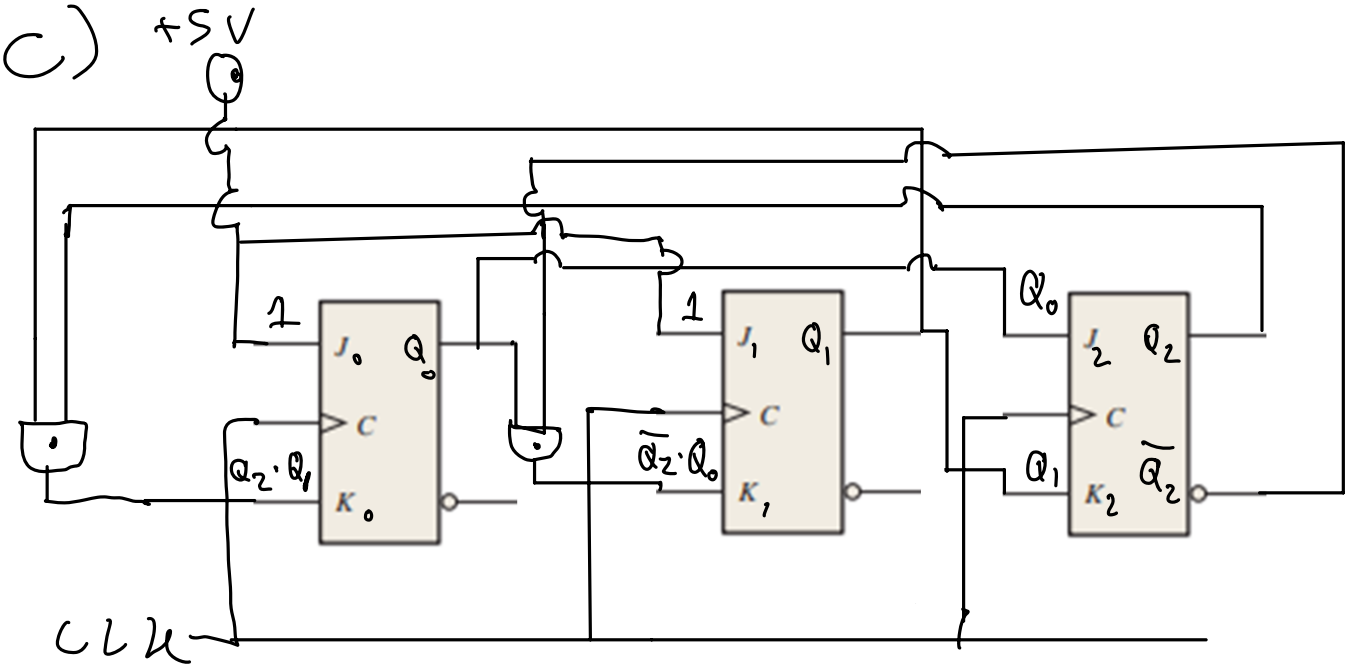
a)

Present state Q_2 Q_1 Q_0	Next state Q_2 Q_1 Q_0	J_2	K_2	J_1	K_1	J_0	K_0
0 1 0	0 1 1	0	X	X	0	1	X
0 1 1	1 0 1	1	X	X	1	X	0
1 0 1	1 1 1	X	0	1	X	X	0
1 1 1	0 1 0	X	1	X	0	X	1

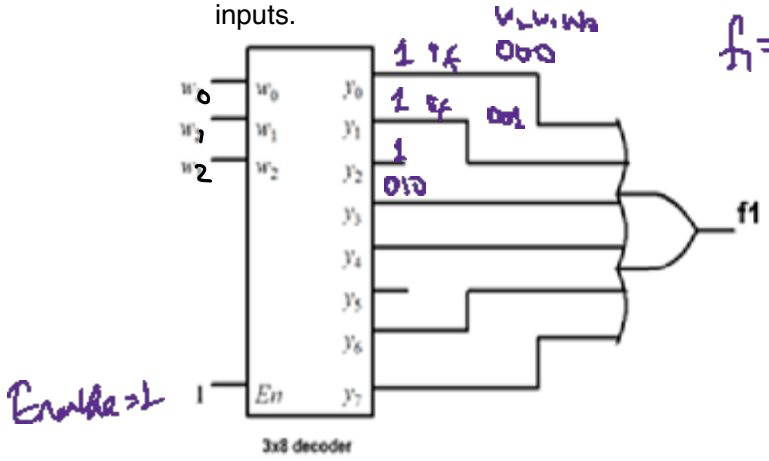
b)



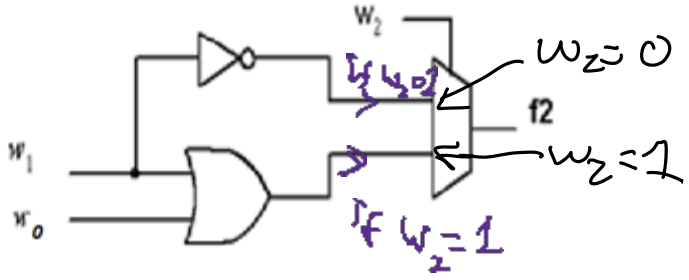
c) +5V



2. Calculate the output values for the functions implemented in the following circuits for the given inputs.



$f_1 = \Sigma(0,1,3,4,6,7)$



Inputs			Outputs	
w2	w1	w0	f1	f2
0	0	0	1	1
0	1	0	0	0
1	0	0	1	0
1	0	1	0	1

$f_2 = \bar{w}_1$

$f_2 = w_1 + w_2$ 3.

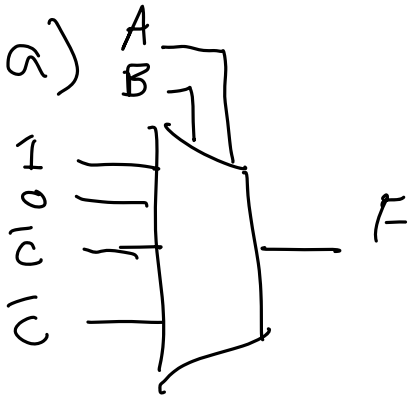
f_1 doesn't work for $\langle w_2 w_1 w_0 \rangle$ = 010 or 101 due to no connections to OR gate for f_1

a) Implement the following function using an 4x1 multiplexer. Sketch the circuit completely, label everything properly.

$$F(A,B,C) = \Sigma\,(0,1,4,6)$$

b) Implement the following function using an 8x1 multiplexer. Sketch the circuit completely, label everything properly.

a)

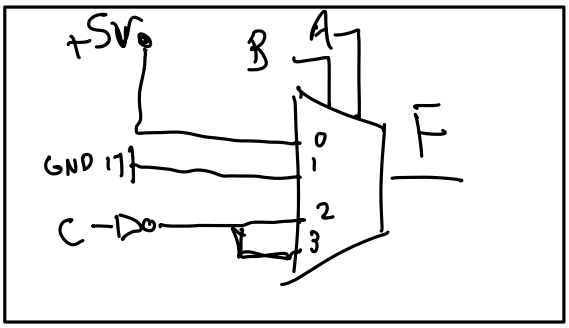


A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

$\bar{C} = F$

$\bar{C} = F$

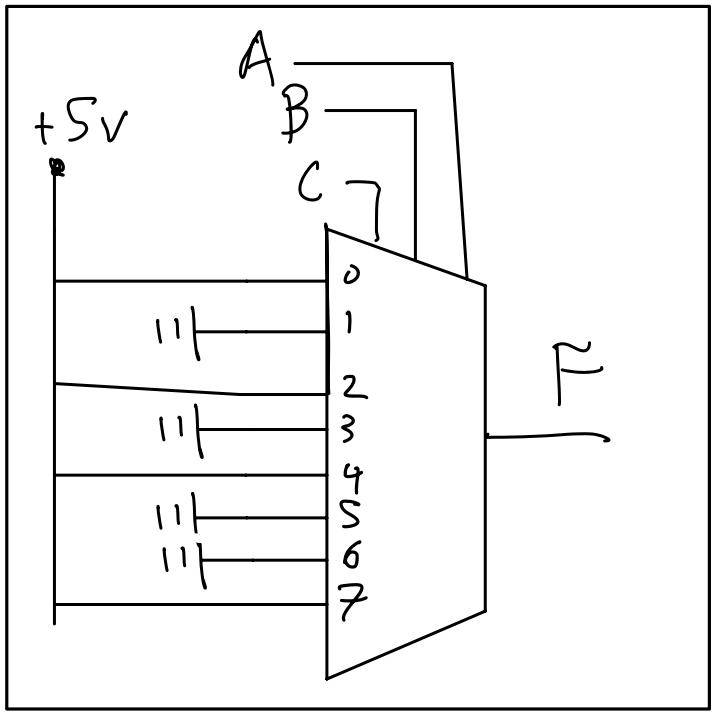
Circuit



b)

A	B	C	D	F	
0	0	0	0	1	F = 1
0	0	0	1	1	
0	0	1	0	0	F = 0
0	0	1	1	0	
0	1	0	0	1	F = 1
0	1	0	1	1	
0	1	1	0	0	F = 0
0	1	1	1	0	
1	0	0	0	1	F = 1
1	0	0	1	1	
1	0	1	0	0	F = 0
1	0	1	1	0	
1	1	0	0	0	F = 0
1	1	0	1	0	
1	1	1	0	1	F = 1
1	1	1	1	1	

Circuit



$$F(A,B,C,D) = \Sigma\,(0,1,4,5,8,9,14,15)$$

4. Derive the state diagram for an FSM that has an input w and an output z. The machine has to generate z = 1 when the previous four values of w were 1001 or 1111; otherwise, z = 0. Overlapping input patterns are allowed. An example of the desired behavior is below:

$$w: 0101111001100111111$$
$$z: 0000000100100011001$$

5. An FSM is defined by the following state-assigned table. Derive a circuit that realizes this FSM using D flip-flops.

Present state y_2y_1	Next state $w=0$ Y_2Y_1	Next state $w=1$ Y_2Y_1	Output z
0 0	1 0	1 1	0
0 1	0 1	0 0	0
1 0	1 1	0 0	0
1 1	1 0	0 1	1

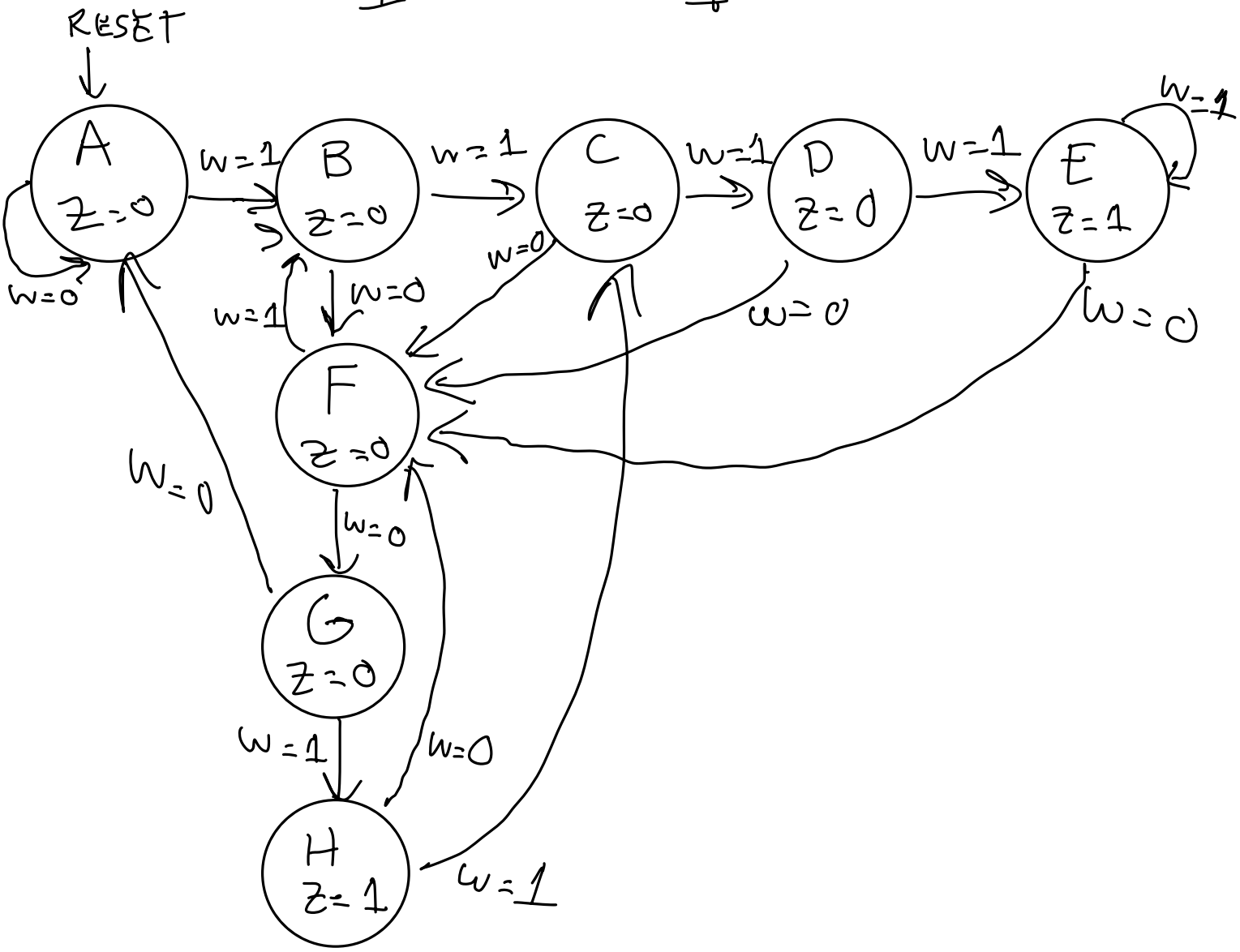
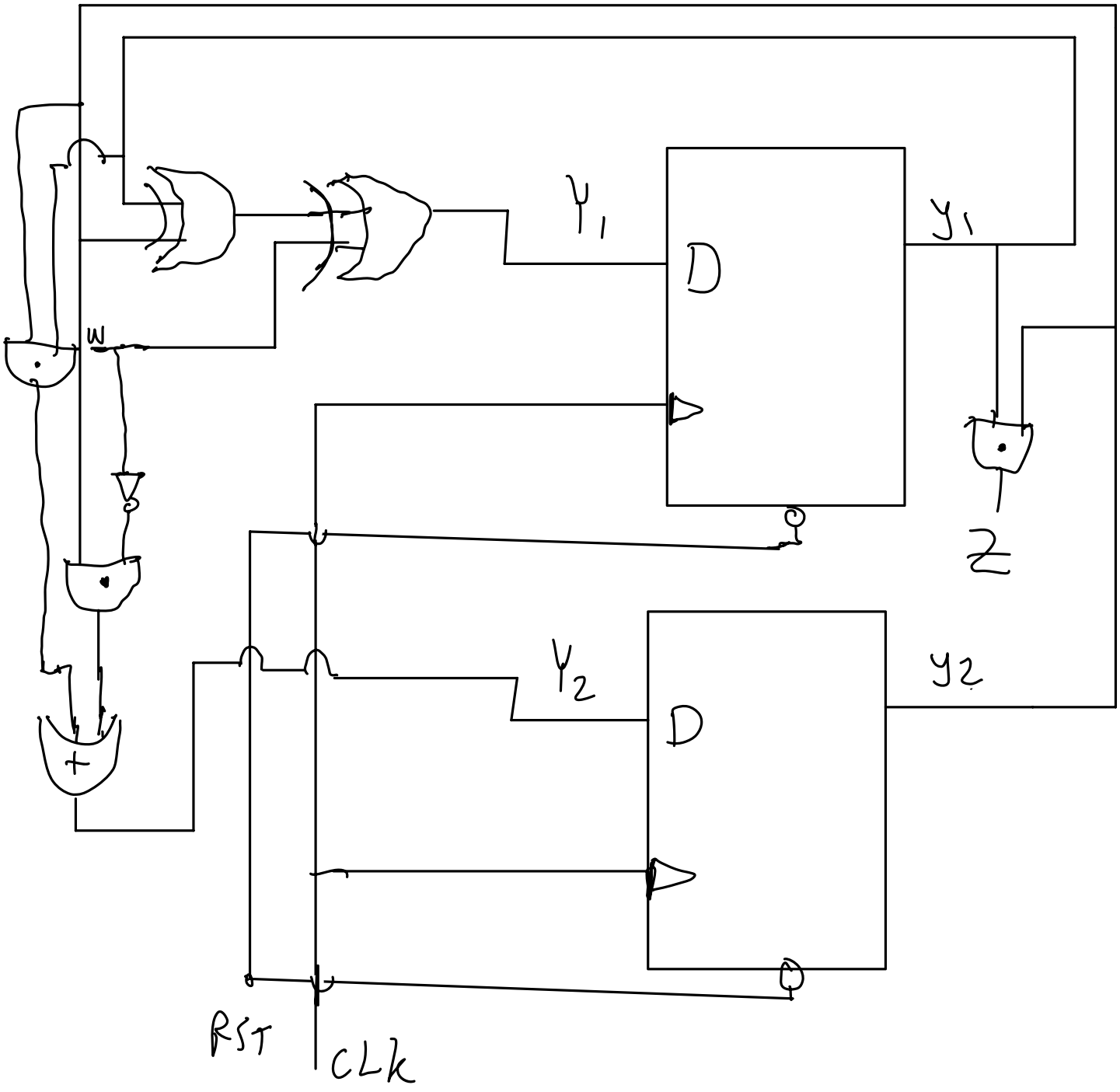
$\rightarrow Y_2 = \bar{w}y_2 + y_1y_2$

$\rightarrow Y_1 = y_2 \oplus y_1 \oplus w$

$\rightarrow z = y_1 \cdot y_2$

Question 5

4) 1 0 0 1 or 1 1 1 1 → Next = 1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