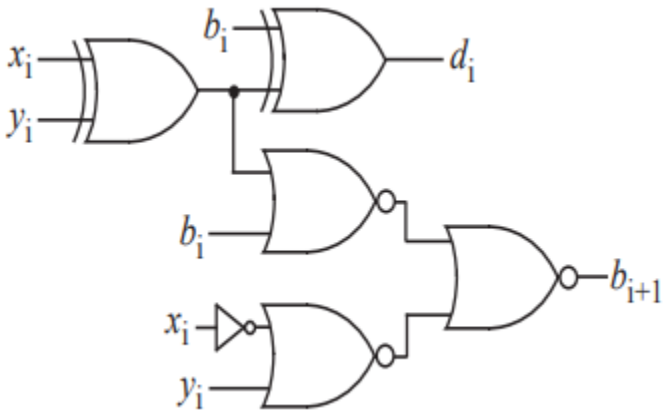
University of Minnesota
EE 2301 Introduction to Logic Design Summer 2023

Homework 3

1. Truth table for a full subtractor is given below.

x_i	y_i	b_i	b_{i+1} d_i
0	0	0	0 0
0	0	1	1 1
0	1	0	1 1
0	1	1	1 0
1	0	0	0 1
1	0	1	0 0
1	1	0	0 0
1	1	1	1 1

   a) Can we use the EXOR gate circuit we use for full adder for the difference function (d_i)?
   b) Obtain a minimal sum of products (SOP) expression for next step borrower, b_{i+1}?
   c) Write the functions of the following circuit.
   d) Does the circuit provide the output values in the truth table? You can check if the function is equivalent to your function or you can obtain the truth table of the circuit with the truth table above.



(1)

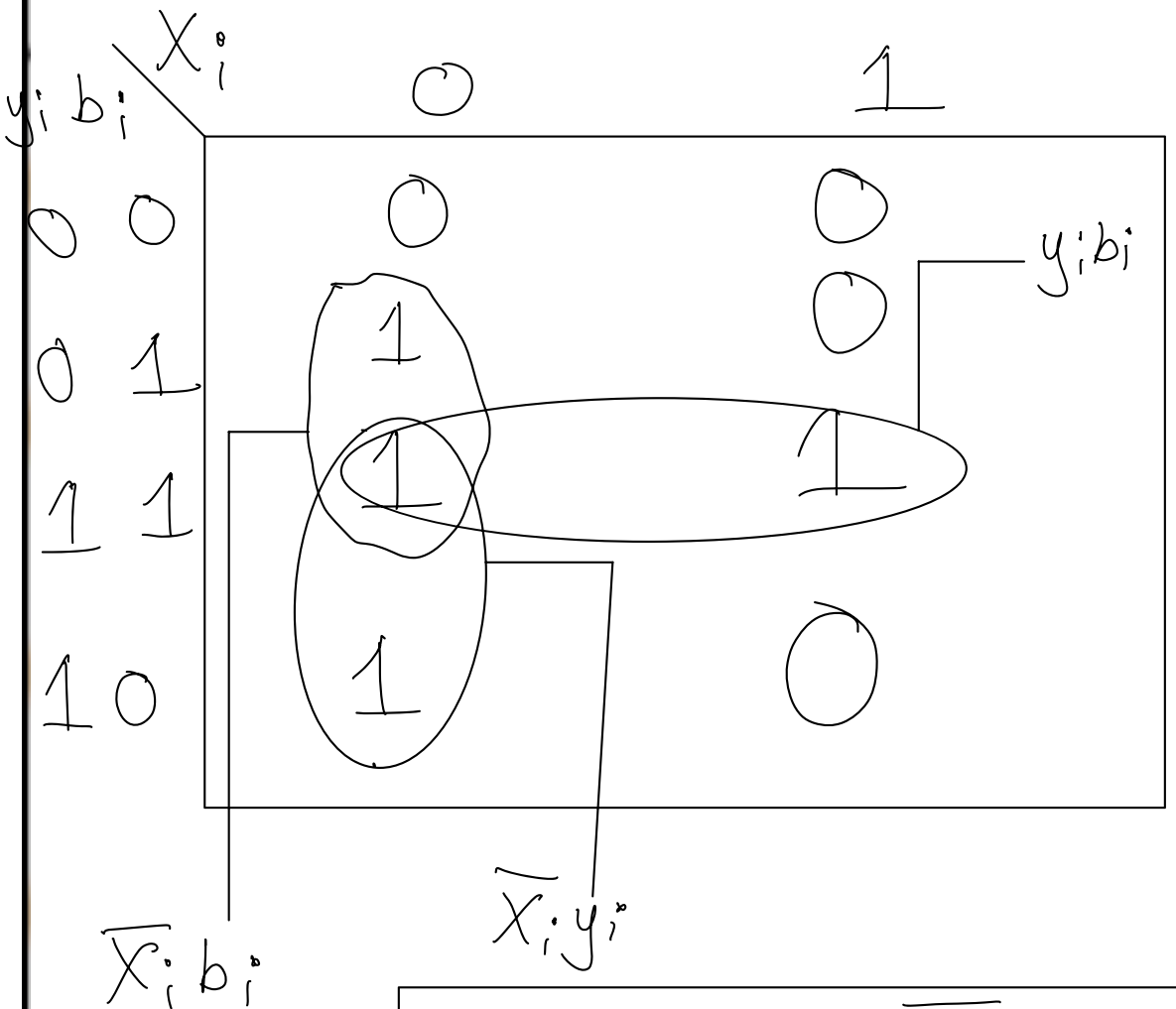
a) $f = x_i \oplus y_i \oplus b_i$

Decimal Number	x_i	y_i	b_i	d_i	
0	0	0	0	0	$0 \oplus 0 \oplus 0 = 0 \oplus 0 = 0$ (good)
1	0	0	1	1	$0 \oplus 0 \oplus 1 = 0 \oplus 1 = 1$ (good)
2	0	1	0	1	$0 \oplus 1 \oplus 0 = 1 \oplus 0 = 1$ (good)
3	0	1	1	0	$0 \oplus 1 \oplus 1 = 1 \oplus 1 = 0$ (good)
4	1	0	0	1	$1 \oplus 0 \oplus 0 = 1 \oplus 0 = 1$ (good)
5	1	0	1	0	$1 \oplus 0 \oplus 1 = 1 \oplus 1 = 0$ (good)
6	1	1	0	0	$1 \oplus 1 \oplus 0 = 0 \oplus 0 = 0$ (good)
7	1	1	1	1	$1 \oplus 1 \oplus 1 = 0 \oplus 1 = 1$ (good)

Yes the truth table proves we can use the X-OR gate for full adder for the difference function(d_i).

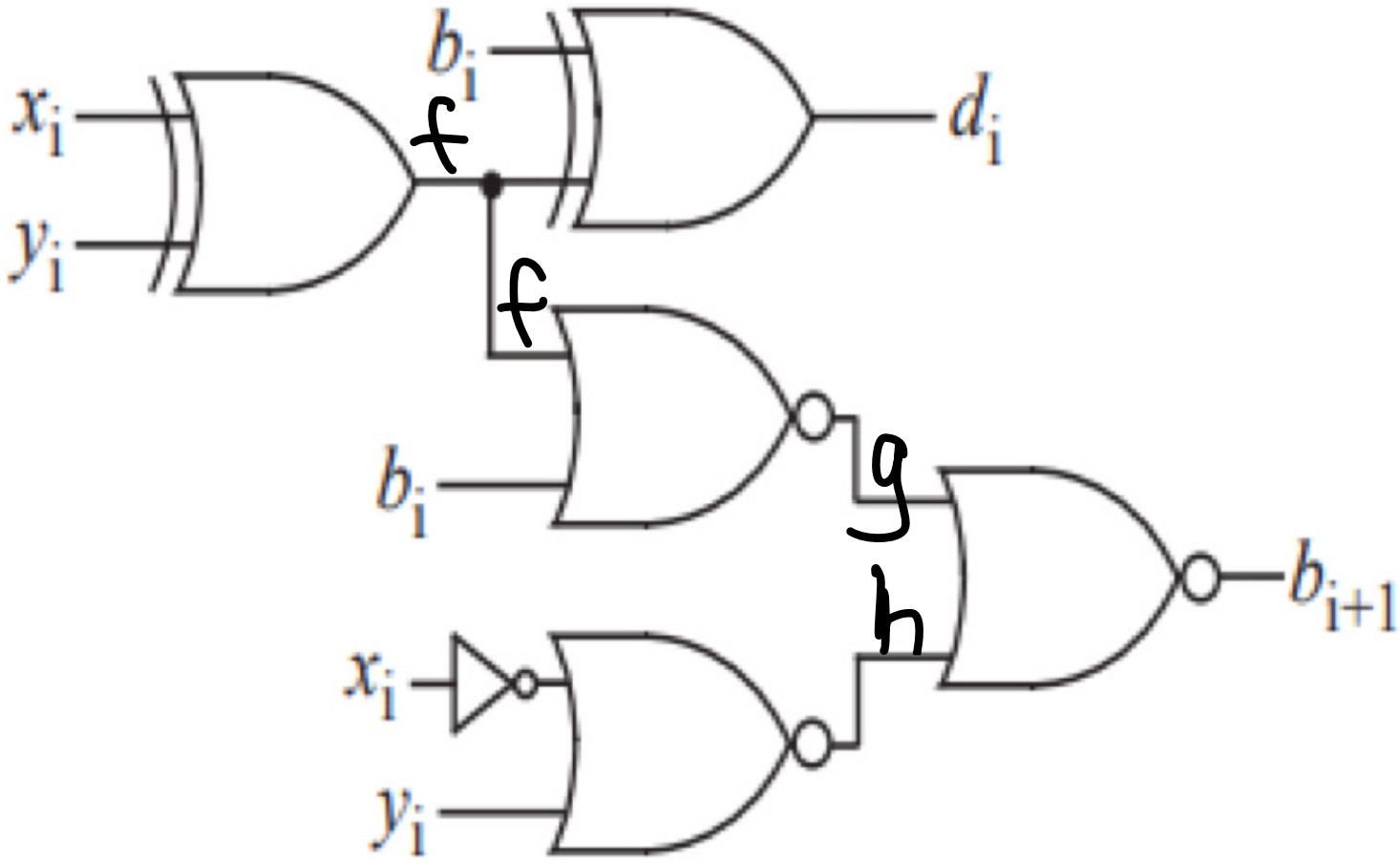
b) minterms: 1, 2, 3, 7 for b_{i+1}

$$\Sigma m(1,2,3,7)$$



$$f = \overline{x}_i b_i + \overline{x}_i y_i + y_i b_i$$

c)



$f = x_i \oplus y_i \rightarrow$ $\boxed{d_i = b_i \oplus x_i \oplus y_i}$

$g = \overline{f + b_i} = \overline{(x_i \oplus y_i) + b_i}$

$h = \overline{\overline{x_i} + y_i}$

$b_{i+1} = \overline{h + g} = \overline{\overline{\overline{x_i} + y_i} + \overline{(x_i \oplus y_i) + b_i}}$

$\boxed{b_{i+1} = (\overline{x_i} + y_i) \cdot (x_i \oplus y_i + b_i)}$

d)

Decimal Number	x_i	y_i	b_i	d_i	
0	0	0	0	0	$0 \oplus 0 \oplus 0 = 0 \oplus 0 = 0$ (good)
1	0	0	1	1	$0 \oplus 0 \oplus 1 = 0 \oplus 1 = 1$ (good)
2	0	1	0	1	$0 \oplus 1 \oplus 0 = 1 \oplus 0 = 1$ (good)
3	0	1	1	0	$0 \oplus 1 \oplus 1 = 1 \oplus 1 = 0$ (good)
4	1	0	0	1	$1 \oplus 0 \oplus 0 = 1 \oplus 0 = 1$ (good)
5	1	0	1	0	$1 \oplus 0 \oplus 1 = 1 \oplus 1 = 0$ (good)
6	1	1	0	0	$1 \oplus 1 \oplus 0 = 0 \oplus 0 = 0$ (good)
7	1	1	1	1	$1 \oplus 1 \oplus 1 = 0 \oplus 1 = 1$ (good)

Decimal Numbers	x_i y_i b_i	b_{i+1}	$b_{i+1} = (\overline{x}_i + y_i) \cdot (x_i \oplus y_i + b_i)$
0	0 0 0	0	$(1+0) \cdot (0 \oplus 0 + 0) = 1 \cdot 0 = 0$
1	0 0 1	1	$(1+0) \cdot (0 \oplus 0 + 1) = 1 \cdot 1 = 1$
2	0 1 0	1	$(1+1) \cdot (0 \oplus 1 + 0) = 1 \cdot 1 = 1$
3	0 1 1	1	$(1+1) \cdot (0 \oplus 1 + 1) = 1 \cdot 1 = 1$
4	1 0 0	0	$(0+0) \cdot (1 \oplus 0 + 0) = 0 \cdot 1 = 0$
5	1 0 1	0	$(0+0) \cdot (1 \oplus 0 + 1) = 0 \cdot 1 = 0$
6	1 1 0	0	$(0+1) \cdot (1 \oplus 1 + 0) = 1 \cdot 0 = 0$
7	1 1 1	1	$(0+1) \cdot (1 \oplus 1 + 1) = 1 \cdot 1 = 1$

Yes, for both b_{i+1} and d_i had the exactly correct outputs of the equation provided by the circuit proven by the truth tables above for both outputs

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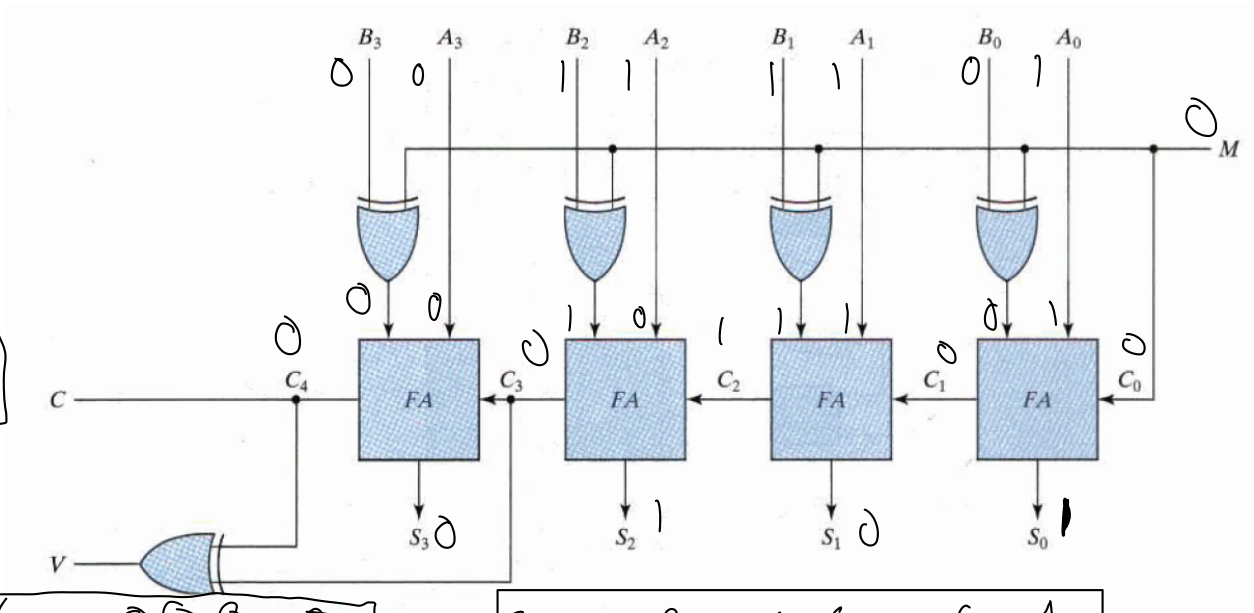
2. The adder-subtractor circuit below has the following values for the mode input M (0: adder, 1: subtractor) and data inputs A and B. For each case, determine the values of four Sum outputs, the carry C, and overflow V.

	M	A	B
(a)	0	0111	0110
(b)	0	1000	1001
(c)	1	1100	1000
(d)	1	0101	1010
(e)	1	0000	0001

a)

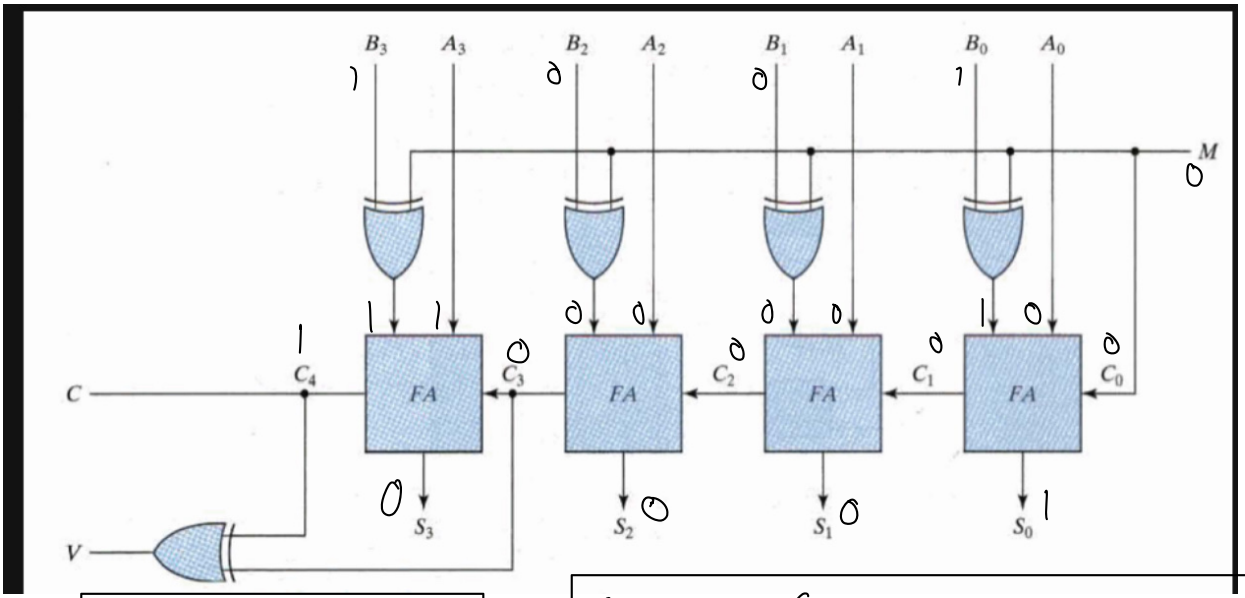


C = 0

V = $C_4 \oplus C_3 = 0 \oplus 0 = 0$

$S_3 = 0, S_2 = 1, S_1 = 0, S_0 = 1$

b)

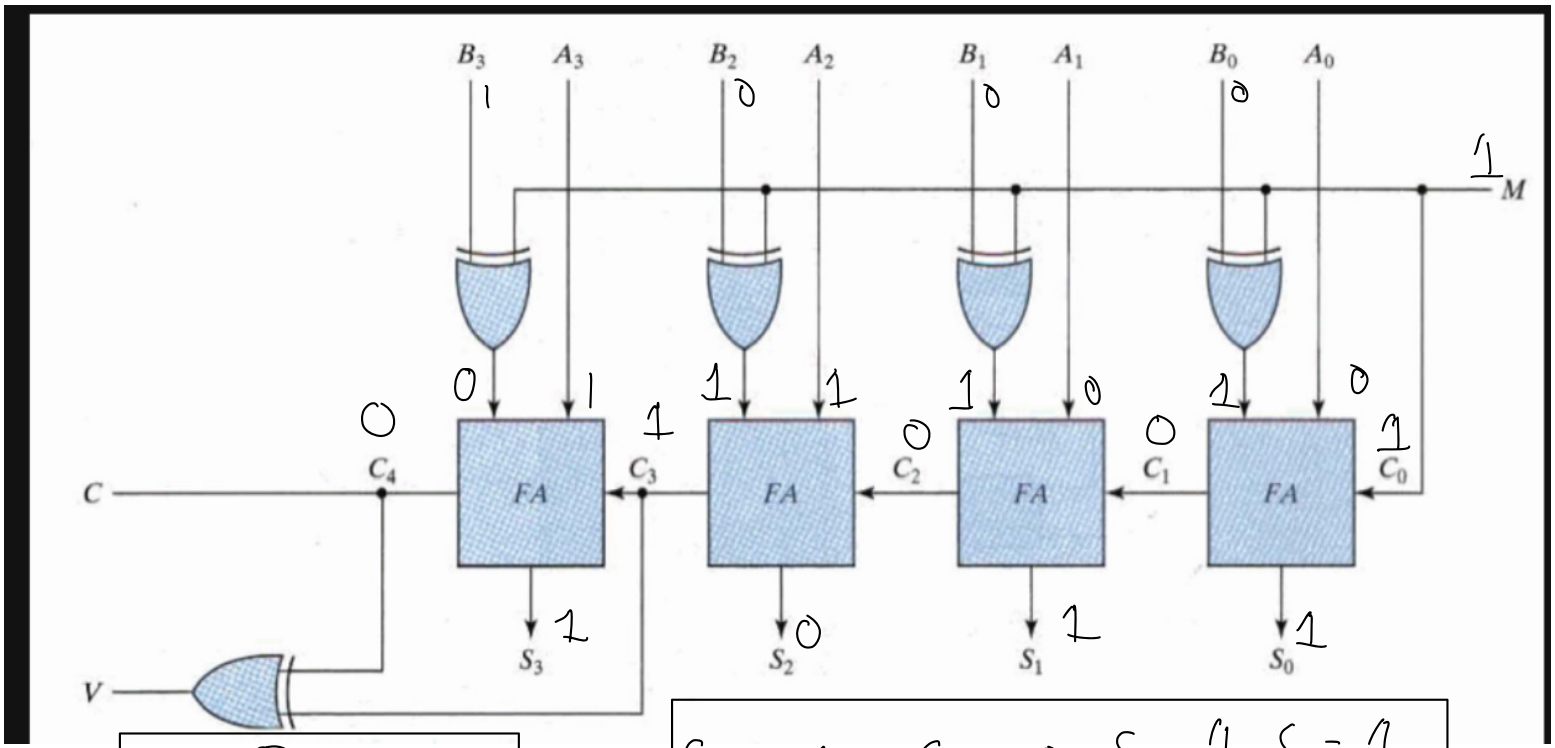


C = 1

V = 1 ⊕ 0 = 1

$S_3 = 0, S_2 = 0, S_1 = 0, S_0 = 1$

c)

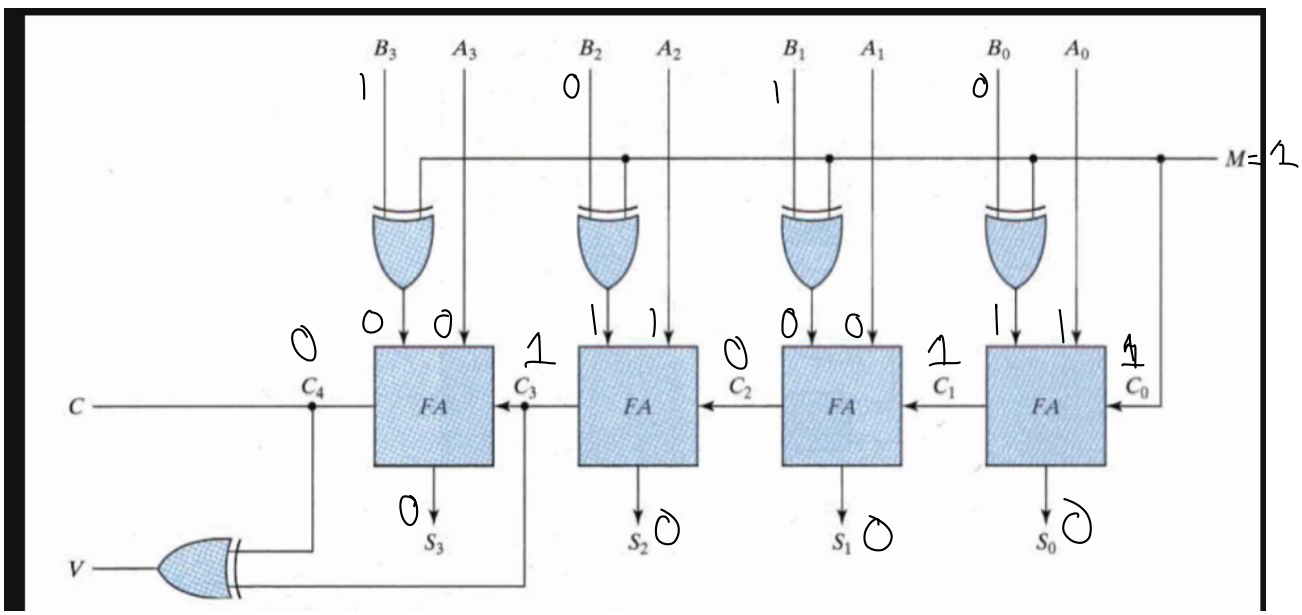


$C = 0$

$V = 1 \oplus 0 = 1$

$S_3 = 1, S_2 = 0, S_1 = 1, S_0 = 1$

d)

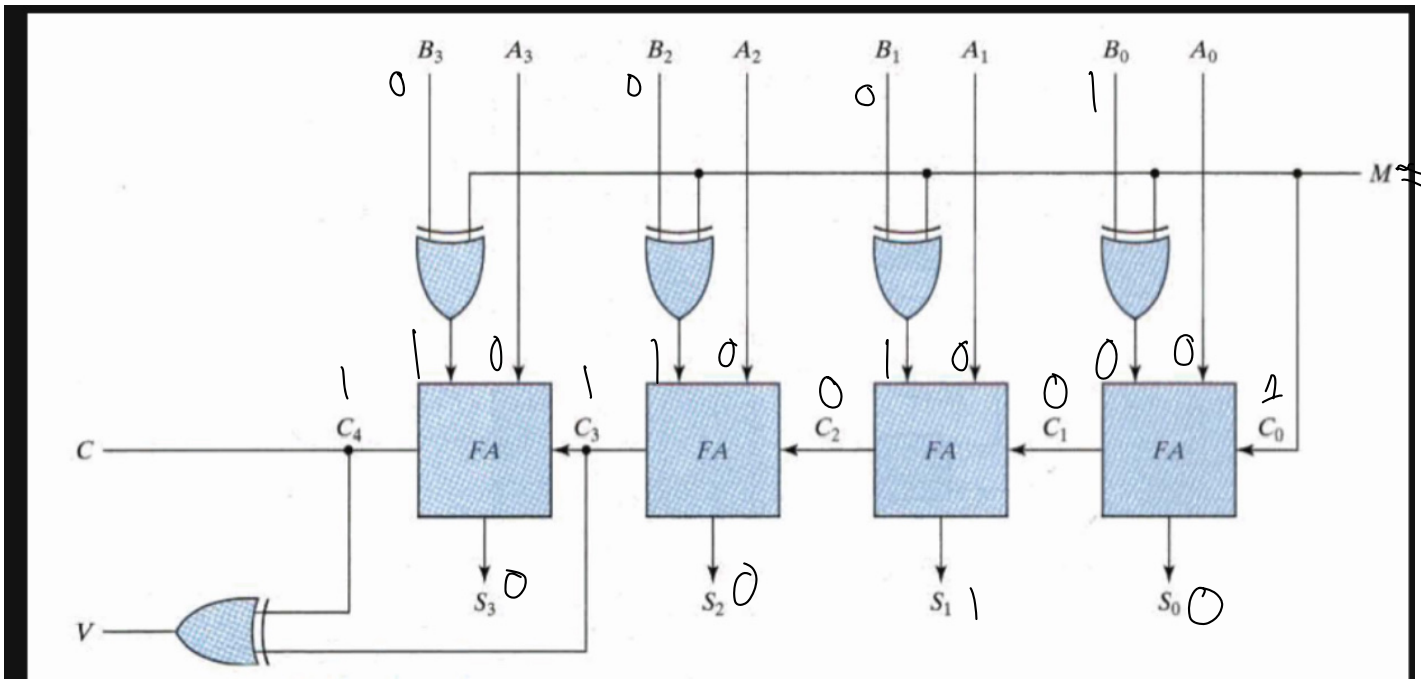


$C = 0$

$V = 1 \oplus 0 = 1$

$S_3 = 0, S_2 = 0, S_1 = 0, S_0 = 0$

e)

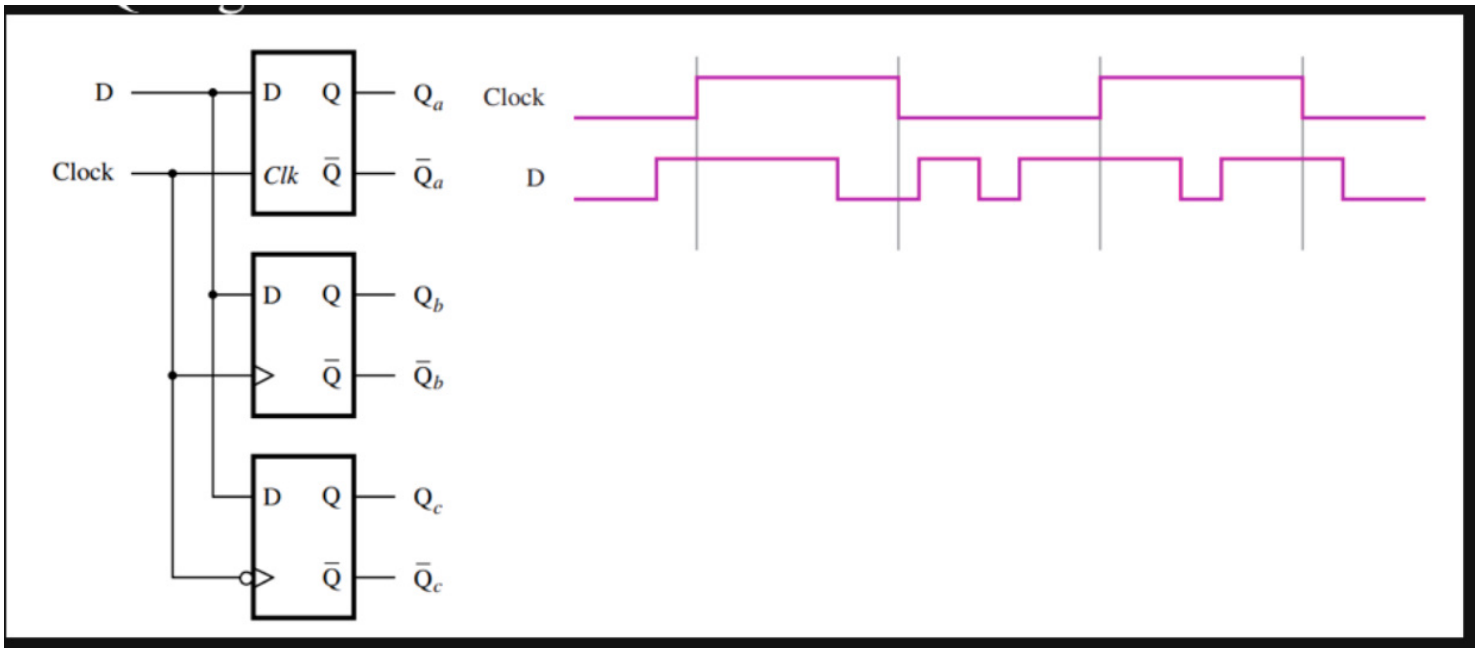

B_3 A_3 B_2 A_2 B_1 A_1 B_0 A_0
0 0 0 1
M = 1
1 0 1 0 1 0 0 0
1 0 0 1
C
C_4 FA C_3 FA C_2 FA C_1 FA C_0
S_3 0 S_2 0 S_1 1 S_0 0
V

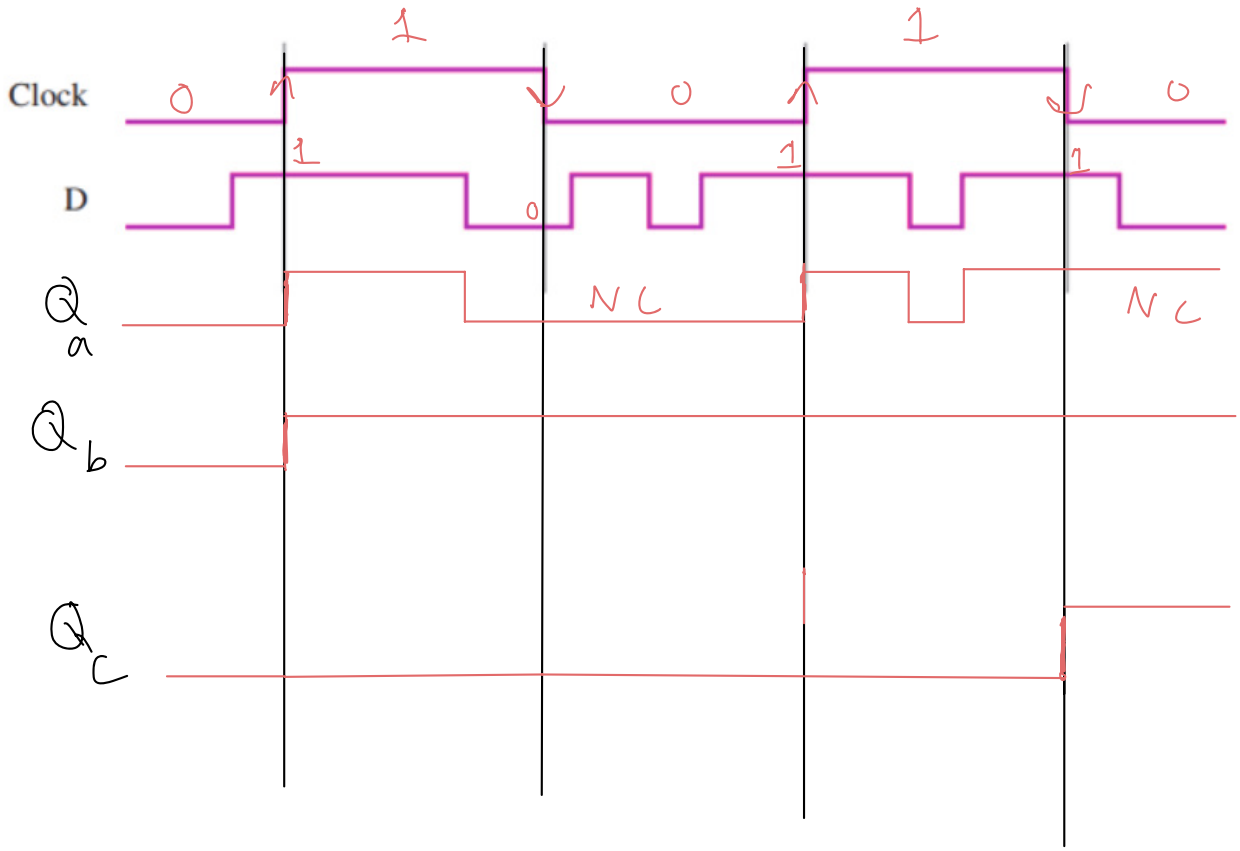
C = 1

V = 101 = 0

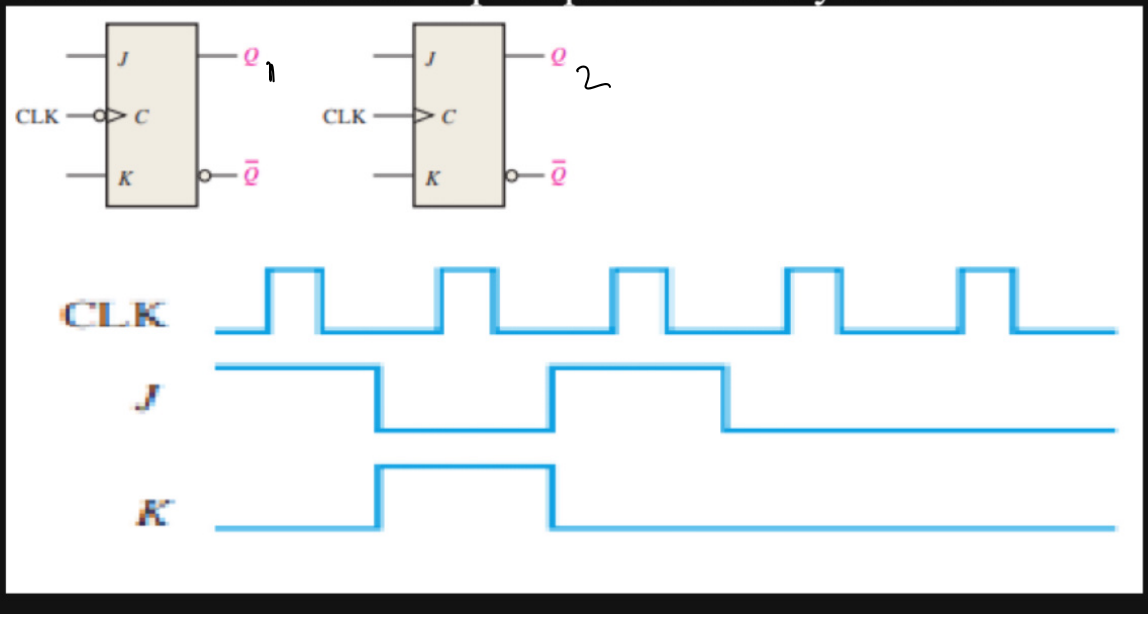
1

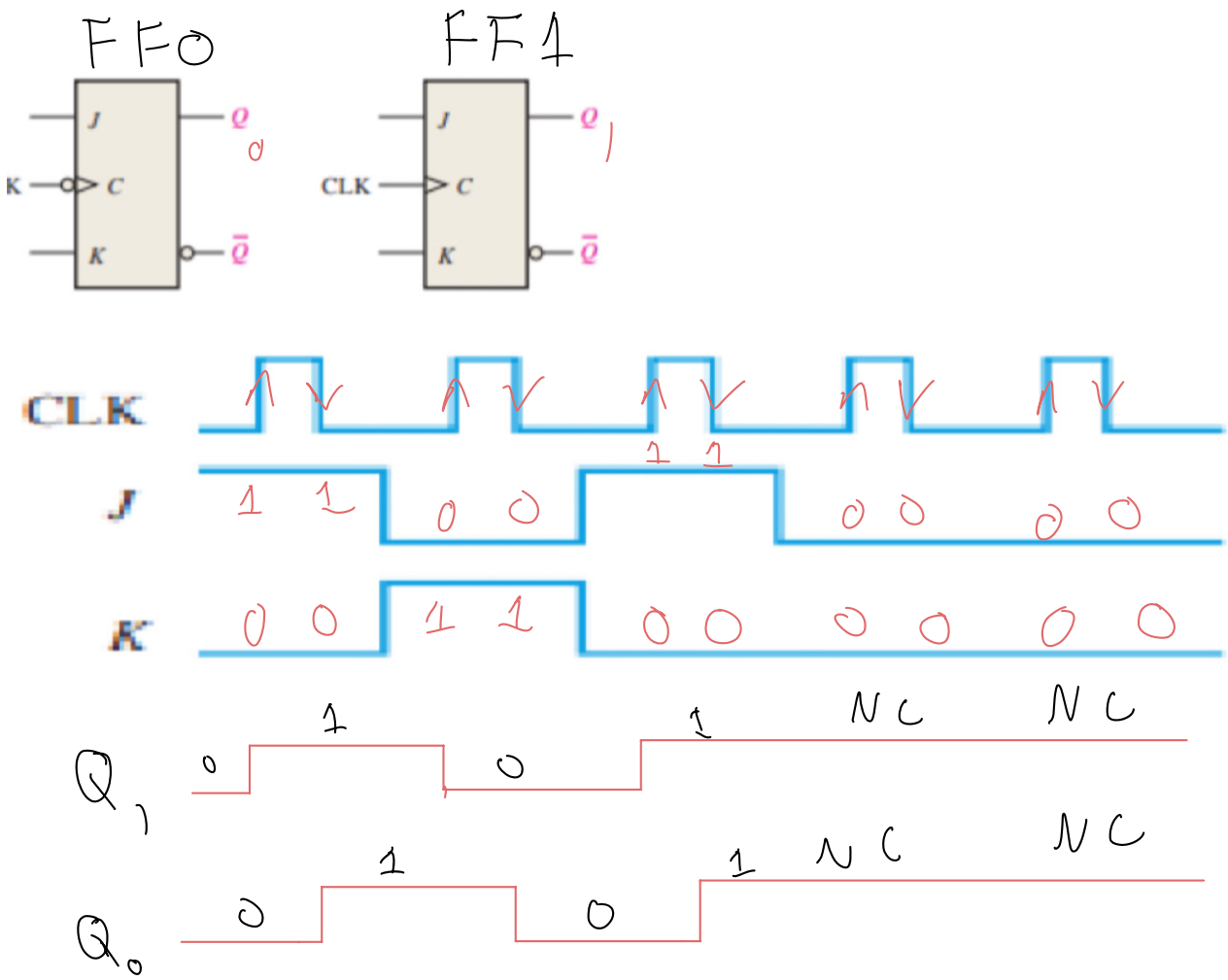
Good luck
Dr. Ahmet Turkmen





4. Two edge-triggered J-K flip-flops are shown in Figure 7–77. If the inputs are as shown, draw the Q output of each flip-flop relative to the clock, and explain the difference between the two. The flip-flops are initially RESET.





Difference between both signals of each JK FF is that for FF0 the value of the output Q_0 is changing accordingly with JK truth table as long at the points where the clock signal is at rising edge. However, for the JK FF1 the measured Q_1 is measured at the falling edge of the clock signal giving output Q_1 accordingly with JK FF truth table.

The difference is also a time delay between the changes between both FF's outputs in this case.