EE 2301 Lab # 5
Final Report

ECE Department

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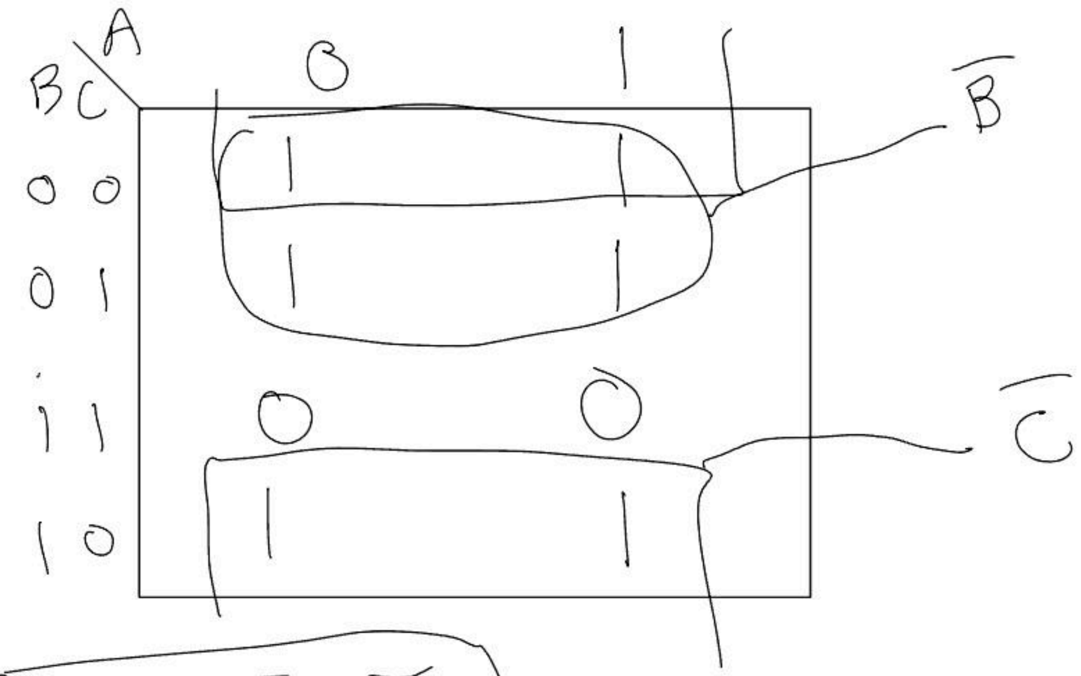
Lab 5a: State-Machines

1. K - Maps and Equations

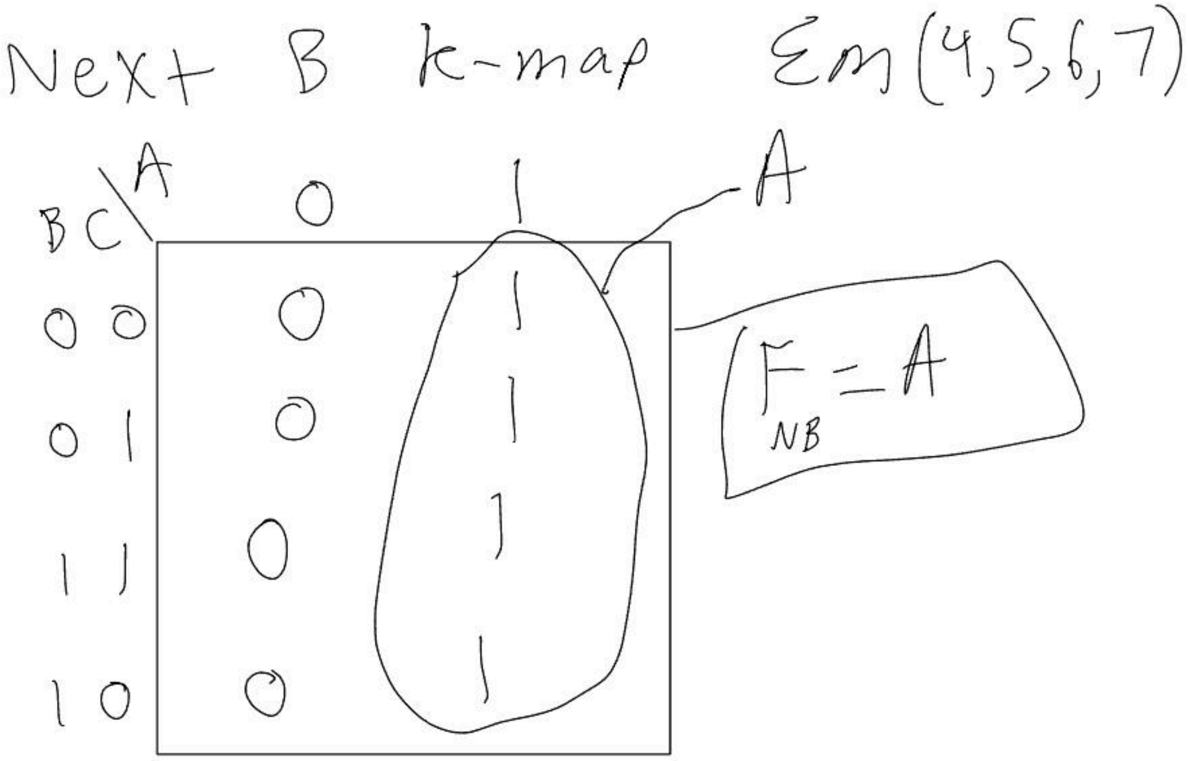
Next A k-map $\Sigma m(0,1,2,4,5,6)$



BC \ A	0	1
00	1	1
01	1	1
11	0	0
10	1	1

$$\boxed{F_{NA} = \overline{B} + \overline{C}}$$

K- Map and Equation for NA

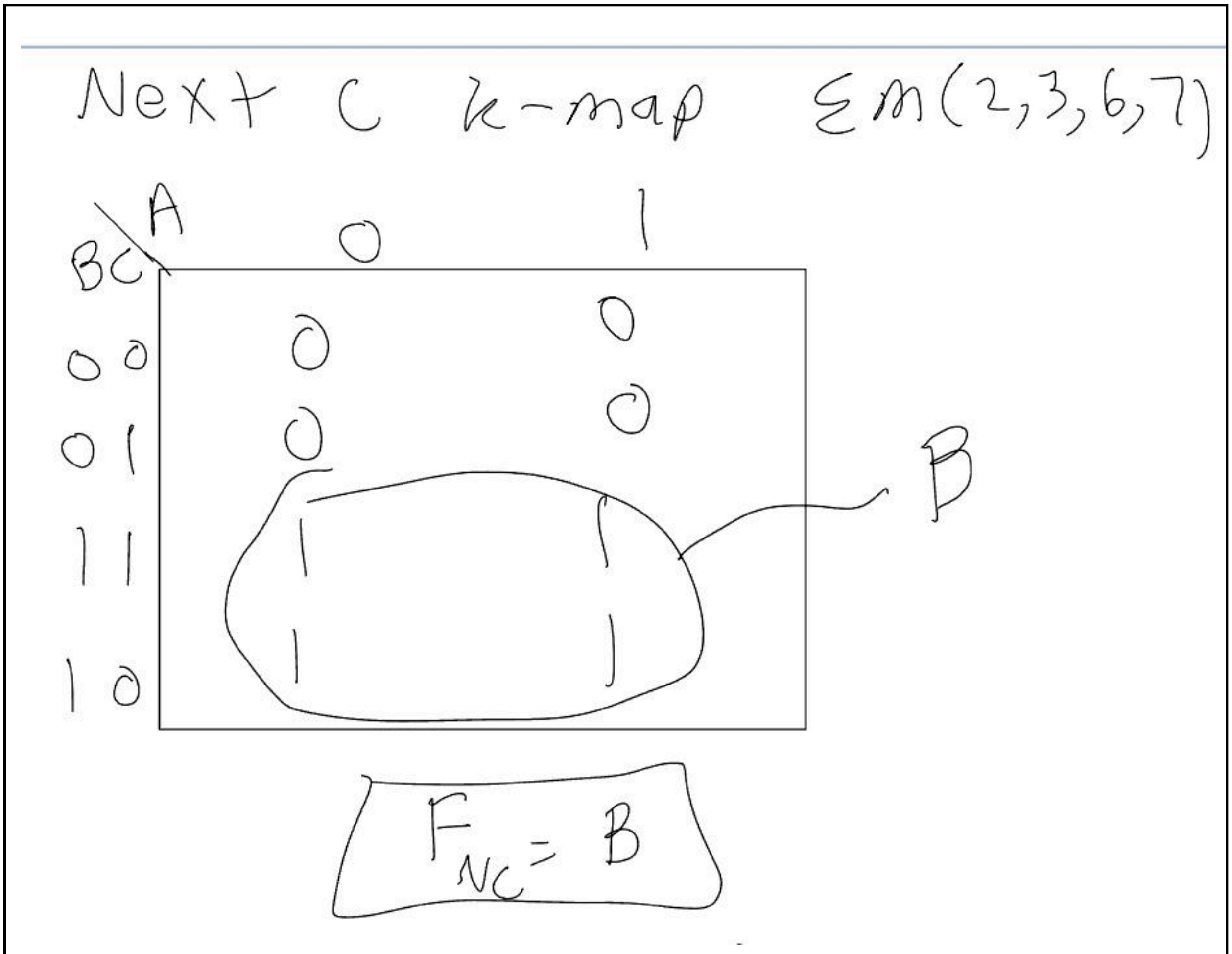


Next B K-map $\Sigma m(4,5,6,7)$

BC\A	0	1
00	0	1
01	0	1
11	0	1
10	0	1

$F_{NB} = A$

K- Map and Equation for NB



Next C k-map $\Sigma m(2,3,6,7)$

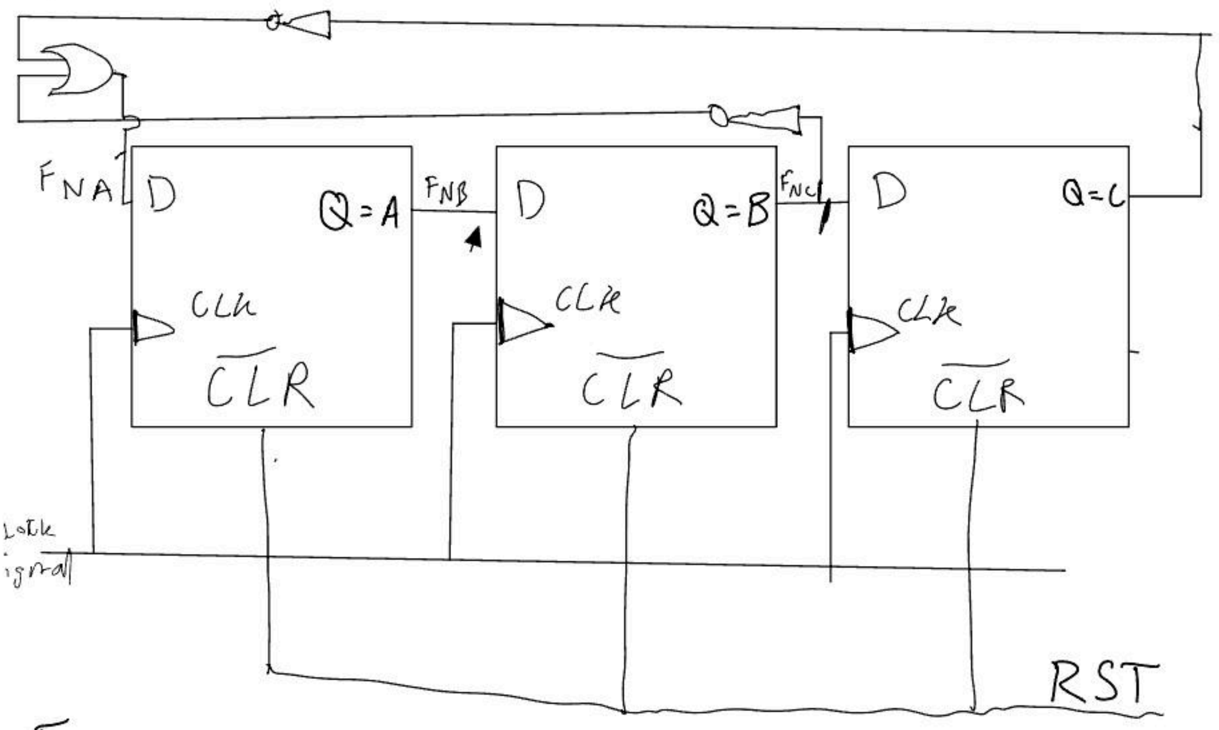
BC \ A	0	1
00	0	0
01	0	0
11	1	1
10	1	1

$F_{NC} = B$

K- Map and Equation for NC

2. Schematic for State-Transition

Schematic



F_{NC}: Next C ; F_{NA} = Next A ; F_{NB} = Next B

Schematic for the State-Transitions on Paper **(NOT the State-Transition Diagram)** **(Complete this on Paper)**

3. Verilog Code for State-Machine

DFF.v:

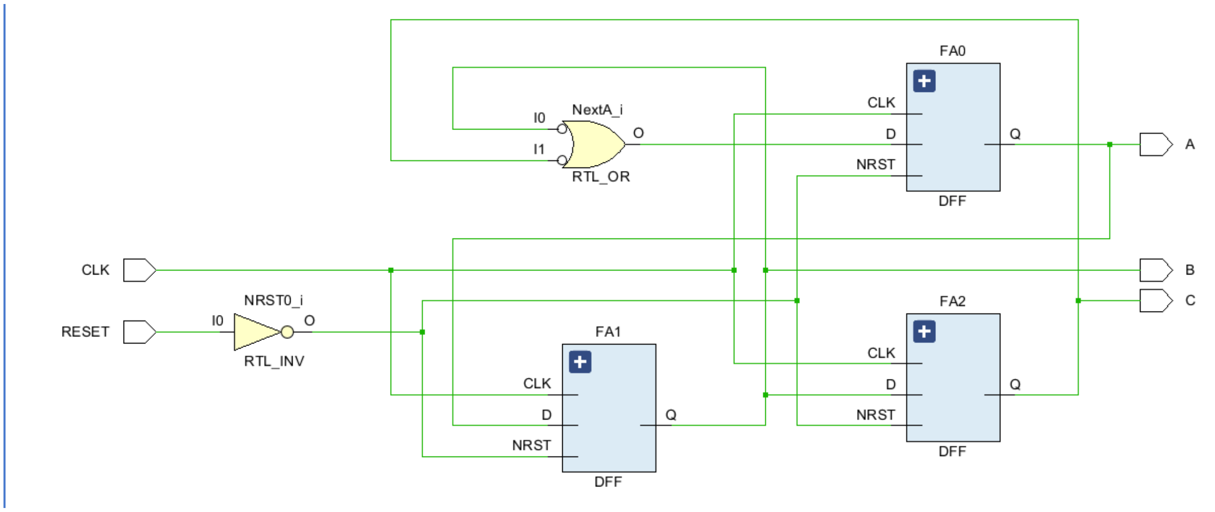
```
module DFF(
    output Q,
    input  D,
    input NRST,
    input CLK
    );

    reg Q;


    always @(posedge CLK, negedge NRST)
    begin
        if (~NRST)
            Q <= 1'b0;
        else
            Q <= D;
    end
endmodule
```

Lab5_Schem.v:

```
module Lab5_Schem(
    output A,
    output B,
    output C,
    input RESET,
    input CLK
    );

    wire NextA, NextB, NextC;

      assign NextA = (~B) | (~C);
      assign NextB = A;
      assign NextC = B;

    DFF FA0(A, NextA, ~RESET, CLK);
    DFF FA1(B, NextB, ~RESET, CLK);
    DFF FA2(C, NextC, ~RESET, CLK);

endmodule
```

Copy of Verilog Code

4. Schematic from Vivado



The only difference is that the RESET is inverted since in the D Flip Flop module the input NRST was inverted to become a regular RESET input. As a result the NRST is playing its part for the DFF module when the RESET is inverted proving that both the schematic on Vivado is the exact same as the schematic drawn in the prelab.

*Note the OR gate has both its inputs (NextC and NextB) inverted

Schematic for Asynchronous/Synchronous Reset **obtained after Elaboration of Verilog Design.**

If this matches the schematic on paper, you are awarded 10pts.
Else
Explain why there is a mismatch? (This gets you full points)

5. Testbench

```
module Lab5_TB (
    // list your ports here if any
);


 reg Reset, Clock;
 wire NA,NB,NC;

Lab5_Schem inst (
    .RESET(Reset),
    .CLK(Clock),
    .A(NA),
    .B(NB),
    .C(NC)
    );


initial
begin
    Clock = 0;
    Reset = 1;
    #25
    Reset = 0;
    #25

    Clock = 1;
    #50
    Clock = 0;
    #50
    Clock = 1;
    #50
    Clock = 0;
    #50
    Clock = 1;
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    Clock = 0;
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    Clock = 0;
    #50
    Clock = 1;
    #50
    Clock = 0;
    #50
    Clock = 1;
    #50
    Clock = 0;


     end

endmodule
```
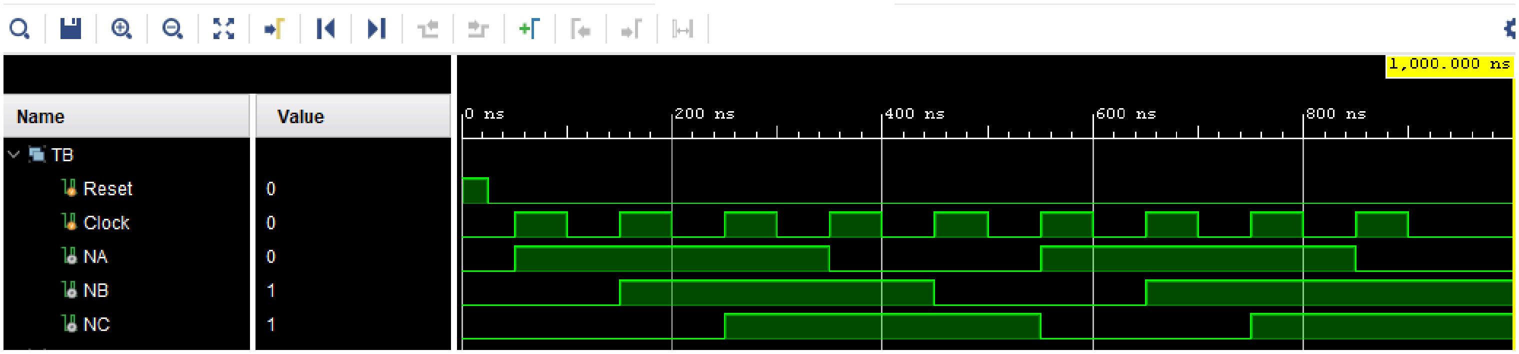

Copy of Testbench used for Simulation

6. Simulated Waveform



Screenshot of Waveforms after Behavioral Simulation

7. Constraint File

```
set_property PACKAGE_PIN V17 [get_ports {CLK}]
set_property IOSTANDARD LVCMOS33 [get_ports {CLK}]
set_property PACKAGE_PIN V16 [get_ports {RESET}]
set_property IOSTANDARD LVCMOS33 [get_ports {RESET}]


set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets {CLK_IBUF}]
set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets {CLK_IBUF_BUFG}]

## LEDs
set_property PACKAGE_PIN U16 [get_ports {A}]
set_property IOSTANDARD LVCMOS33 [get_ports {A}]
set_property PACKAGE_PIN E19 [get_ports {B}]
set_property IOSTANDARD LVCMOS33 [get_ports {B}]
set_property PACKAGE_PIN U19 [get_ports {C}]
set_property IOSTANDARD LVCMOS33 [get_ports {C}]
```

Copy of Constraint File used for Implementation

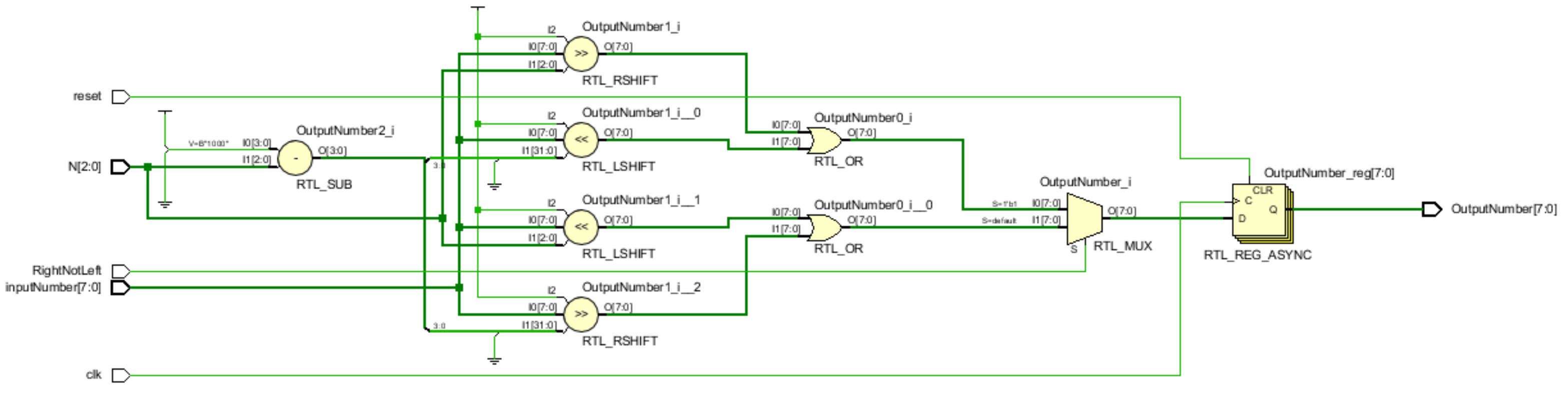
Lab 5b: Bi-Directional Shift Register

1. Verilog Code for State-Machine

```
`timescale 1ns / 1ps



module Lab5BFinal(
input [7:0] inputNumber,
input RightNotLeft,
input [2:0]N,
input reset,
input clk,
output [7:0] OutputNumber
   );
 reg [7:0]OutputNumber;

always @(posedge clk or posedge reset)
 begin
   if (reset) begin
      OutputNumber <= 8'b0;
   end
   else begin
      if(RightNotLeft)
      OutputNumber <= (inputNumber>>N) | (inputNumber<<(8-N));
      else
      OutputNumber <=( inputNumber << N )| ( inputNumber >>(8-N));
   end
 end

endmodule
```

Copy of Verilog Code with Asynchronous Reset Low

2. Schematic from Vivado



Schematic of Bi-directional Shift Register with Asynchronous Reset **obtained after Elaboration of Verilog Design.**

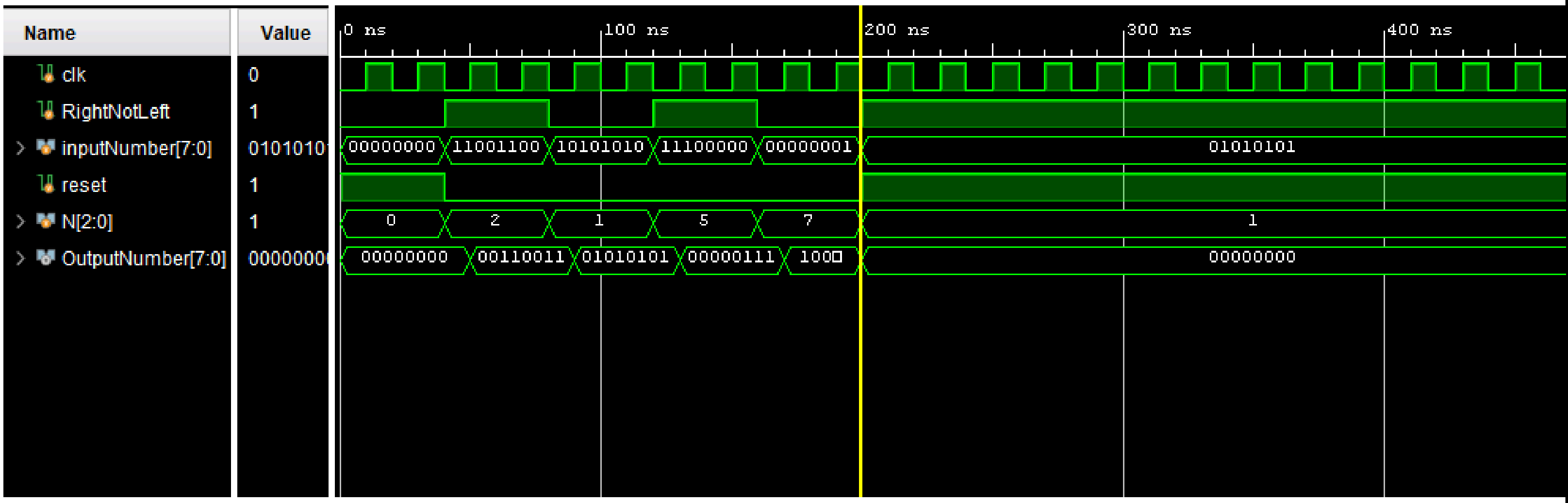
3. Testbench

```
`timescale 1ns / 1ps



module Lab5bfinal_tb(

    );
reg clk = 0;
reg RightNotLeft;
reg[7:0] inputNumber;
reg reset=0;
reg [2:0] N;
wire [7:0]OutputNumber;

Lab5BFinal inst(
 .inputNumber(inputNumber),
 .clk(clk),
 .reset(reset),
 .RightNotLeft(RightNotLeft),
 .N(N),
 .OutputNumber(OutputNumber)
  );
    always #10 begin
        clk<=~clk;
    end
    initial
    begin
         inputNumber = 8'b00000000; N = 3'd0; RightNotLeft = 0;reset = 1;
        #40
        inputNumber=8'b11001100; RightNotLeft=1; N=3'd2;reset=0;
        #40
        inputNumber = 8'b10101010; RightNotLeft = 0; N = 3'd1;reset = 0;
        #40
        inputNumber =8'b11100000; RightNotLeft=1; N=3'd5; reset = 0;
        #40
        inputNumber = 8'b00000001; RightNotLeft = 0; N = 3'd7; reset = 0;
        #40
        inputNumber = 8'b01010101; RightNotLeft = 1;  N = 3'd1;reset = 1;

        end
```

```
endmodule
```

Copy of Testbench used for Simulation

4. Simulated Waveform



Screenshot of Waveforms after Behavioral Simulation

5. Constraint File

```
## Switches
set_property PACKAGE_PIN V17 [get_ports {inputNumber[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {inputNumber[0]}]
set_property PACKAGE_PIN V16 [get_ports {inputNumber[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {inputNumber[1]}]
set_property PACKAGE_PIN W16 [get_ports {inputNumber[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {inputNumber[2]}]
set_property PACKAGE_PIN W17 [get_ports {inputNumber[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {inputNumber[3]}]
set_property PACKAGE_PIN W15 [get_ports {inputNumber[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {inputNumber[4]}]
set_property PACKAGE_PIN V15 [get_ports {inputNumber[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {inputNumber[5]}]
set_property PACKAGE_PIN W14 [get_ports {inputNumber[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {inputNumber[6]}]
set_property PACKAGE_PIN W13 [get_ports {inputNumber[7]}]
set_property IOSTANDARD LVCMOS33 [get_ports {inputNumber[7]}]
set_property PACKAGE_PIN T2 [get_ports {N[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {N[0]}]
set_property PACKAGE_PIN R3 [get_ports {N[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {N[1]}]
set_property PACKAGE_PIN W2 [get_ports {N[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {N[2]}]
set_property PACKAGE_PIN U1 [get_ports {clk}]
   set_property IOSTANDARD LVCMOS33 [get_ports {clk}]
set_property PACKAGE_PIN T1 [get_ports {RightNotLeft}]
set_property IOSTANDARD LVCMOS33 [get_ports {RightNotLeft}]
set_property PACKAGE_PIN R2 [get_ports {reset}]
set_property IOSTANDARD LVCMOS33 [get_ports {reset}]


## LEDs
set_property PACKAGE_PIN U16 [get_ports {OutputNumber[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {OutputNumber[0]}]
set_property PACKAGE_PIN E19 [get_ports {OutputNumber[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {OutputNumber[1]}]
set_property PACKAGE_PIN U19 [get_ports {OutputNumber[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {OutputNumber[2]}]
set_property PACKAGE_PIN V19 [get_ports {OutputNumber[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {OutputNumber[3]}]
set_property PACKAGE_PIN W18 [get_ports {OutputNumber[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {OutputNumber[4]}]
set_property PACKAGE_PIN U15 [get_ports {OutputNumber[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {OutputNumber[5]}]
set_property PACKAGE_PIN U14 [get_ports {OutputNumber[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {OutputNumber[6]}]
set_property PACKAGE_PIN V14 [get_ports {OutputNumber[7]}]
set_property IOSTANDARD LVCMOS33 [get_ports {OutputNumber[7]}]

#Clock Signal every 10ns

#create_clock -period 10.000 -name sys_clk_pin -waveform {0.000 5.000} -add [get_ports clk]
set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets {clk_IBUF}]
set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets {clk_IBUF_BUFG}]
```

Copy of Constraint File used for Implementation