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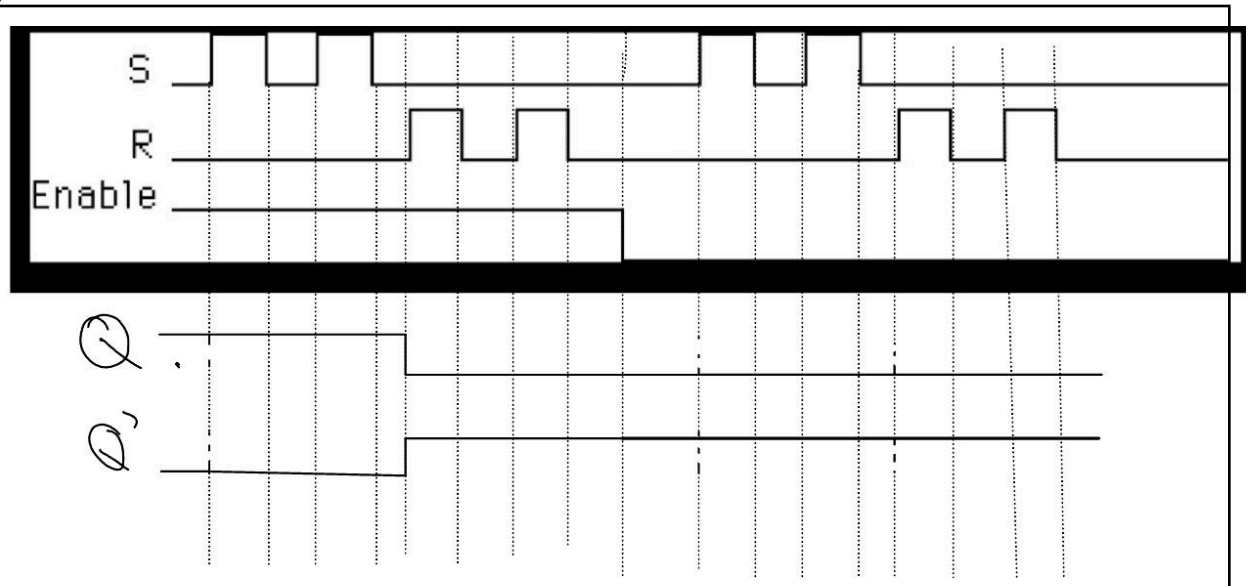
Lab 4: Latches and Flip-Flops

I. *RS Latch with Enable*

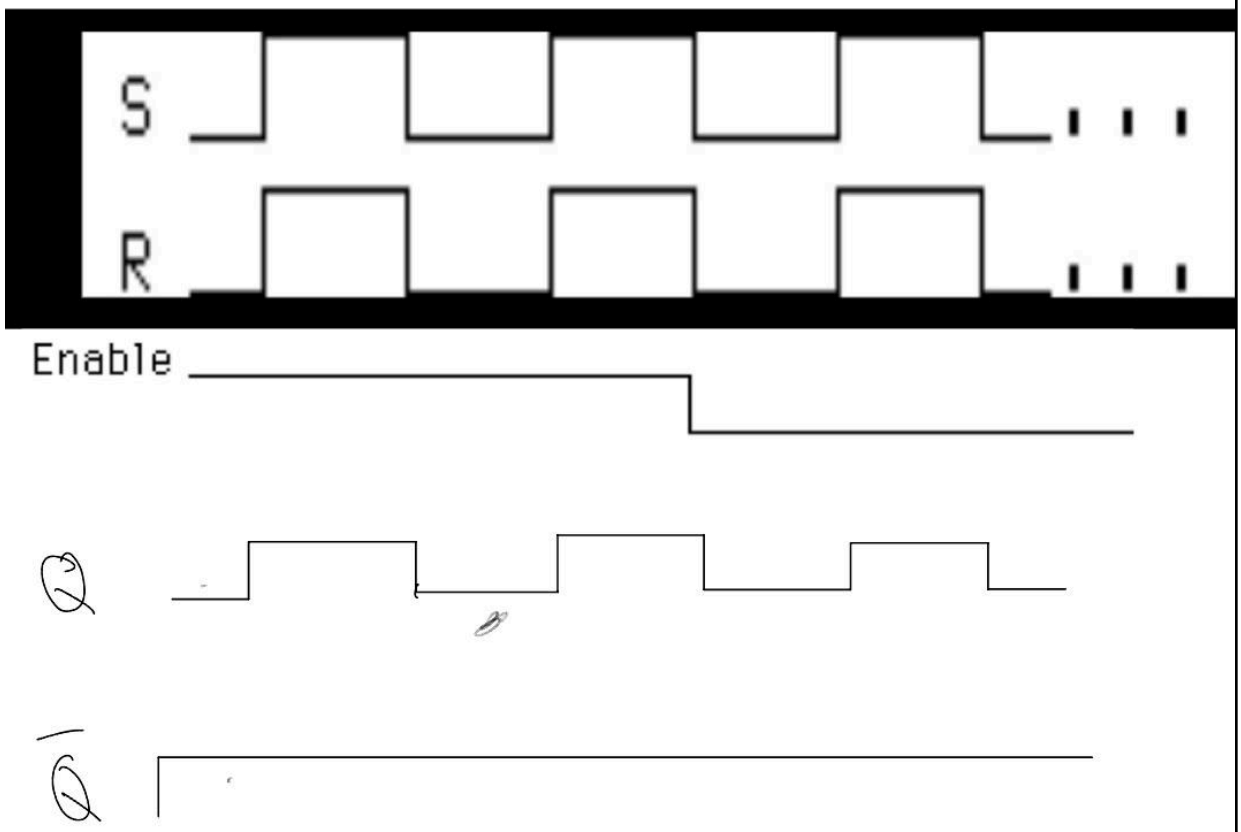
a)



Note *Q starts at high based on the recorded data from the lab

Plot the response of the gated S-R NAND latch you observed for the following input sequence in part A.4

b).



Plot the response of the gated S-R NAND latch you observed for the following input sequence in part A.5

c).

Explanation:

No, in the second plot it clearly makes the SET and RESET to turn on with a single LED switch that when the signal is sent out to the circuit the output signal returned by Q always toggled when both SET and RESET inputs return to 0 at the same time.

Reason 1:
Shown in the second plot when both the set and reset change at the same time the Q' is staying the exact same throughout unlike the Q output which is a result of the signal sent out to the

switch reaches the SET pin and then branches out to reach the RESET pin causing a time delay where the change of inputs causes the Q' that goes through the chip to be an unexpected Q' when looking at output Q.

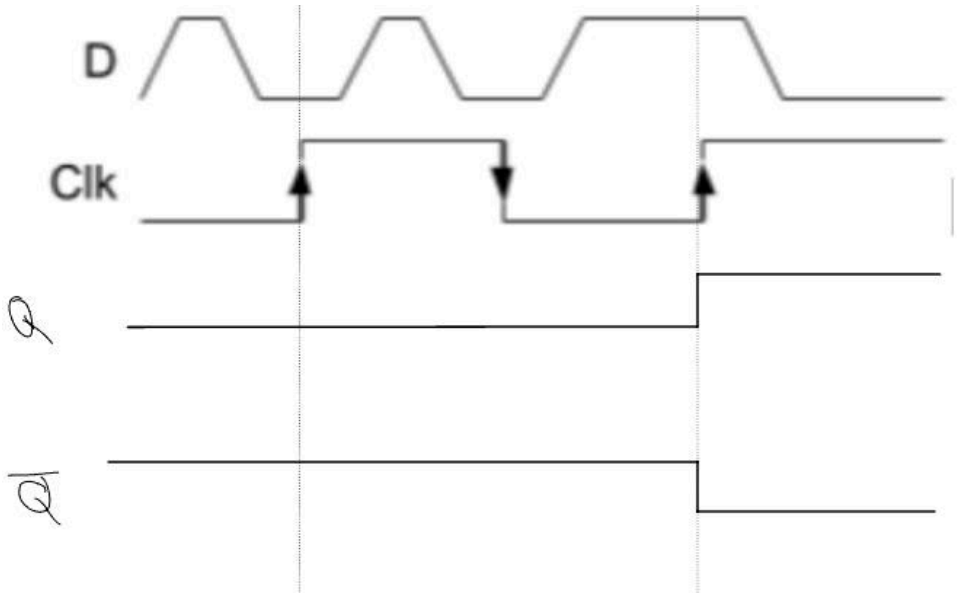
Reason 2:
When the SET and RESET inputs are both 0 and then the new inputs for RESET and SET become both 1 simultaneously, the state of the S-R latch gives an invalid(unpredictable) output.

Does the latch always have the same output value on Q after both S and R return to 0 at the same time? If so, might this change if the upper and lower gates were swapped in the circuit? Explain.

Give two reasons why this latch should not be used with both inputs simultaneously 1.

II. D Flip-Flop

a)



Plot the response of the D Flip-Flop you observed for the following input sequence in part B.7

b)

Explain the function on the PRE and CLR inputs.

These inputs are independent of a clock signal as they are the inputs that cause RESET or SET. If both inputs are high whatever the input D is at the rise of the clock signal will be outputted to Q as the PRE and CLR with their interconnections allow signals to pass through the Flip Flop with the clock signal for enabling output Q to reflect input Q for that instance and hold that till the next rise of the clock signal at a new (or not new) value for the input D. PRE is putting an attempt to make output Q to equal 0 and CLR is putting an attempt to make output Q to equal 1 both independent from data(D) and the clock signal.

What happens when you leave PRE and CLR are left open?

The capacitors that are in PRE and CLR are still holding onto charge that causes there to be an output for both in Q and Q' as the CLK and Data(D) are turned on in different combinations there will still be an output of Q and/or Q' resulting from that leftover charge in the PRE and CLR.

Explain the function on the PRE and CLR inputs.
What happens when you leave PRE and CLR are left open?

c)

Yes, since the CLK acts as an asynchronous signal causing immediate changes to the SET and RESET inputs when there is no CLK (Low) present. If the DFF is not synchronized properly with the CLK there are potential glitches resulting with unpredictable changes to the outputs Q and Q'.

With the Step B.9 Can you cause the output to change abnormally when CLK is HIGH or LOW? Explain

When comparing the S-R latch to the D Flip Flop it was clear that the S-R latch was much more dependent on the block signal for when generating outputs based on the S and R inputs along with how the D Flip Flop is utilizing the clock signal as an input based on the rise of the signal. As we may know the latch tends to change according to the clock signal as well as the inputs given in real time with no memory which is worse in performance due to a change in input can cause a large or no change in the output. Furthermore, the reason edge triggered flip flops are potentially better(FF advantage) than basic latches is the control the person has with the use of the clock signal helps achieve different outputs based on the given inputted Data (dependent on PRE and CLR). However, an advantage of the basic latch can change its output along with the inputs(not always the case due to clock signal interfering) . You change the input that with a basic latch design the S and/or R inputs must change in order for the desired output to be achieved. If there was ever a situation when the user wants to be able to control the timings on an output an edge-triggered flip-flop will work perfectly.

Write a brief description of the operation of the various latches and flip-flops based on your laboratory observations. Basically Compare the performance of the basic latch and the

edge-triggered flip-flop. What are the advantages and disadvantages of each design? For what applications are each best suited?