Supplement to

Logic and Computer Design Fundamentals
3rd Edition[1]

TEXT ERRATA

Printing 1[2] **- Version 4.3** (Last updated 9/21/06)

General

The following references in the text to the color "blue" should be to the color "green."(Added 9/1/04; page & line numbers added 2/8/05)

Location by Page/Line Numbers (B indicates lines counted from bottom of the page)

8/7	15/3B	15/6B	16/14	119/11	206/11	210/24	267/13	275/11	280/8	333/2B	370/10B	382/18
405/1B	431/9	442/5	442/7	443/3B	458/1	463/3B	529/13	532/2B	536/2B	548/1	548/10	549/9

Chapter 1

Chapter 2

p. 67, line 17 In the equation for H, replace "ACE + ACF" with "ABE + ABF" **(**Added 10/27/04**)**
p. 68, line 18 In the equation for H, replace "A" with "AF"**(**Added 10/27/04**)**
p. 86, Problem 2-34: Replace "2-32" with "2-33"
p. 86, Problem 2-35(a): Replace "2-33" with "2-34"

Chapter 3

p. 93, line 18: Replace "VDHL" with "VHDL" (Added 10/27/04)
p.133, Problem 3-1: Change "F" in the second equation to "G"
p. 138, Problem 3-24: Replace equations with "F = $\overline{W}$" and "G = $\overline{W}$ $\overline{Y}$ + WZ" Use the circuit in the figure at the top of the next page for 2-to-4 Decoder diagram/table. The two 2-to-4 Decoder symbols including the "bubbles" in Figure 3-34 represent this circuit.**(Updated 9/21/06)**

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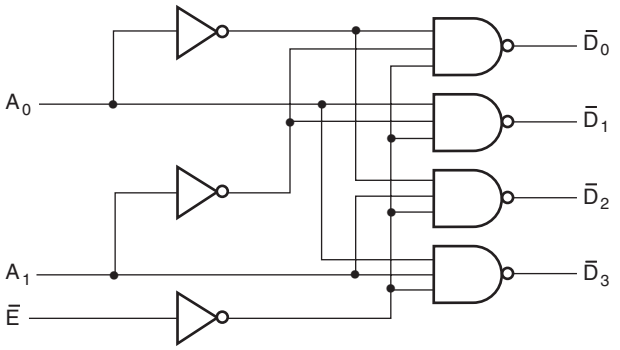
[2] Many of the errors listed may have been corrected in subsequent printings.



(a) Logic diagram

Ē	A_1	A_0	$\bar{D}_0$	$\bar{D}_1$	$\bar{D}_2$	$\bar{D}_3$
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0
1	X	X	1	1	1	1

(b) Truth table

$$\bar{D}_0 = \overline{E\ \bar{A}_1\ \bar{A}_0}$$
$$\bar{D}_1 = \overline{E\ \bar{A}_1\ A_0}$$
$$\bar{D}_2 = \overline{E\ A_1\ \bar{A}_0}$$
$$\bar{D}_3 = \overline{E\ A_1\ A_0}$$

(c) Logic Equations

p. 139, Problem 3-25: Hint: Compare your equation results to those in the figure above to assist you in describing the function. **(Updated 9/21/06)**

Chapter 4

p. 165, Figure 4-21, Input $I_{1,0}$: Replace Z with $\overline{Z}$. Input $I_{2,0}$: Replace Z with $\overline{Z}$. (Added 10/27/04)
p. 193, Problem 4-7: Replace "four" with "two" and "48" with "32"
p. 193, Problem 4-11: Replace "BCD" with "decimal"
p. 193, Problem 4-14: Replace "decoder" with "multiplexer" (Added 1/16/04)
p. 193, Problem 4-15: Remove "-" between "eight" and "3"
p. 195, Problem 4-27: OR gates or 3-state outputs on ROMs are also needed. (Added 2/26/04)

Chapter 5

Chapter 6

p. 246, line 9 from bottom and line 8 from bottom: Change *S* to $\overline{S}$ **(Added 9/21/06)**

p. 246, line 7 from bottom: Change *R* to $\overline{R}$ **(Added 9/21/06)**

p. 247, Figure 6-6: Change *S* to $\overline{S}$ and *R* to $\overline{R}$ in both the figure and the table (four changes total) **(Added 9/21/06)**
p. 254, Figure 6-14(b): Remove center input from 3rd flip-flop; remove center input from 4th flip-flop and add "bubble" to bottom input (Added 2/26/04)
p. 272, Table 6-3 heading:Replace "6-21" with "6-24" (Added 9/1/04, page no. corrected 2/8/05)
p. 276, Equation for B(t+1):Replace "C" with "X" (Added 9/1/04)
p. 288, Figure 6-32, line 23 (including blank lines): Delete "end if" (Added 2/26/04)
p. 300, Figure 6-37: Add ⌉ to the left of the SR flip-flop outputs (to designate the flip-flop as master-slave).
p. 300, Figure 6-37: For flip-flop 1, the setup time, t_s, is equal to the length of time the clock is high, t_{ch} **(Added 9/21/06)**
p. 301, Problem 6-9: Add "*" after "6-9."**(Added 9/21/06)**

p. 302, Table 6-10: Change “Problem 6-9” to “Problems 6-9, 6-29 and 6-30” Change “Input s” to “Inputs” (two places).
p. 303, Problem 6-12, line 2: Replace “input Y” with “output Y” **(Added 9/21/06)**
p. 304, Problem 6-19(b): Change last two bits of NRZI Message from “01” to “10”
p. 306, Problem 6-25: Change “Table 6-5” to “state diagram in Figure 6-25(d)”
p. 307, Problem 6-28: Change “6-25” to “6-23” and “Table 6-6” to “Figure 6-40” Change “Z” to “Y”

Chapter 7

p. 315, lines 12-13 from bottom: Delete “, in the same manner as for bytes in Chapter 1” (Added 2/26/04**,** clarified 3/4/04)
p. 330, Table 7-7: In table heading, change 7-7 to 7-11. **(Added 9/21/06)**
p. 336, Figure 7-14: Between each XOR gate and OR gate, add a 2-input AND gate with $\overline{\text{Load}}$ as the second input (Added 2/26/04). Replace the AND gate with $\overline{\text{Load}}$ and Count as inputs with a wire connected only to Count. **(Added 9/21/06)**
p. 343, Table 7-12: Delete the 3rd column “0/0” and “0/1” in rows 0 and 1, respectively **(Added 9/21/06)**
p. 348, line 2 from bottom: Replace “7-2” with “7-21(a)” (Added 10/27/04)
p. 350, Figure 7-22: On the top register, replace “Register B” with “Register A” (Added 3/4/04)
p. 358, Problem 7-14: Replace “Figure 7-13” with “Figure 7-14” (Added 10/27/04)
p. 359, Problem 7-22, line 2:Replace “fourth” with “fifth” (Added 9/1/04)
p.359, Problem 7-22, lines 14-15:Replace “outputs that are ... .” with “three outputs: the two select variables for the multiplexer and the load signal for register R4.” (Added 9/1/04)
p. 360, Problem 7-27: Replace “7-2” with “7-22” (Added 2/26/04)
p. 360, Problem 7-30: Replace “bus system” with “circuit” (Added 2/26/04)

Chapter 8

p. 383, Figure 8-12. Interchange the wire connections to D0 and D1 on the bottom DEMUX with Z as its input **(Added 9/21/06)**
p. 389, Figure 8-16, line 16: Add < before = A (Added 2/8/05)

Chapter 9

Chapter 10

p. 438, Figure 10-7: Disconnect the S_0 input of block “One Stage of Logic Circuit” from C_i and attach it to a new input, C_{in}. (Added 2/26/04)
p. 439, line 2: Replace “C_i with C_{in}” (Added 9/1/04)
p. 439, Section 10-4, 7th line: Replace “Bus A” with “Bus B” (Added 2/26/04)
p. 441, line 12: Replace “12-2” with “12-3” (Added 9/1/04)
p. 447, Table 10-6 In the line “R7 ← R7 + 1”, column MB, replace Register with — **(Added 9/21/06)**

p. 447, Table 10-7 In the line "R7 ← R7 + 1", column MB, replace 0 with × **(Added 9/21/06)**
p. 454, Table 10-8, Status Bits column: The status bits N and Z are also valid for the following operations: Add Immediate (ADI), Branch on Zero (BRZ), and Branch on Negative (BRN). **(Added 9/21/06)**
p. 478, Problem 10-12: Delete parts **(b)** and **(c)** (changed 3/4/04)
p. 480, Problem 10-20: Delete "the opcode is 0010001"

Chapter 11

p. 489, line 19: Replace "addition" with "arithmetic evaluation" (Added 10/27/04)
p. 507, line 1, after "left." Add: "In most architectures, the Logical Shift, Arithmetic Shift, and Rotate place the outgoing bit into the carry bit." **(Added 9/21/06)**
p. 507, line 12. Add: "For shifts of greater than one bit position, a reasonable decision needs to be made on how to fill the positions vacated, and what if anything to load into the carry bit." **(Added 9/21/06)**
p. 515, Table 11-9: Change "Branch if lower" to "Branch if below" and "BL" to "BB" Change "Branch if lower or equal" to "Branch if below or equal" and "BLE" to "BBE" **(Added 9/21/06)**
p. 522, Problem 11-1: Change "Section 11-1" to "11-2" For SUB, the operand order is: difference ← minuend − subtrahend. For DIV, the operand order is: quotient ← dividend/divisor. **(Added 9/21/06)**
p. 522, Problem 11-4: Add "Y =" to beginning of expression. **(Added 9/21/06)**

Chapter 12

p. 545, Table 12-2, 3rd line, 2nd column: Add code "01"
p. 565, Table 12-5, 4th line, last column: Change "$\overline{PS}$" to "PS"
p. 576, Problem 12-3: Replace "below Figure 12-5" with "on page 536"
p. 577, Problem 12-19: Replace "12-4" with "12-5"

Chapter 13

p. 584, line 23: Replace "ms" with "μs" (Added 10/27/04, page no. corrected 2/8/05)

Chapter 14

Index

p. 655: Delete "v" in "tpdv" (Added 2/26/04)

Please e-mail errors to: crkime@writphotec.com. Thanks to those of you providing error information. A special thanks to Professor De Boer of Dordt College for use of his Textbook Errata in identifying errors resulting in many of the 9/16/06 additions here and in the Problem Solutions.