Scope of Work (SoW)

For

Design and Development of

DFCC MKII PSU Card

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List of Abbreviations

Abbreviation	Description
DFCC	Digital Flight Control Computer
PSU	Power Supply Unit
ADT	Air Data Transducer
RSA	Rate Sensor Assemblies
ASA	Accelerator sensor assemblies
SOV	Solenoid Operated Valve
LVDT	Linear Variable Differential Transformer
LVA	Low voltage Alarm
PTOR	Power Turn on Reset
NVM	Non-volatile Memory
BOM	Bill of Material
ATP	Acceptance Test Plan
SCIH	Standard Conditions In House
SC/EOL	Standard Conditions/End of Life
AEC/EOL	All Environmental Conditions/End of Life

1.0 Overview

The DFCC MKII PSU is a power supply module installed in the Digital flight control computer. The PSU receives 28VDC from the aircraft and converts it into regulated +5VDC, -5VDC, +15VDC and – 15VDC outputs for use by the DFCC Analog and Digital circuits modules.

The PSU also provides current limited DC power outputs to the Air Data Transducers (ADTs), Rate Sensor Assemblies (RSAs), Acceleration Sensor Assemblies (ASAs), and transient limited power to the solenoid Operated Valves (SOV's).

The PSU also provides AC excitation to the Linear Variable Differential Transformers (LVDTs) and the RSA Spin motors.

Finally, the PSU provides separate +5VDC power to the Digital module's SRAMs and separate +5VDC power to the Digital module's NVMs.

2.0 Scope of Work

The design and development of DFCC MKII PSU shall have the following scope of work

1. The Vendor shall design and develop the complete DFCC MK II PSU card as per the technical specifications.
2. The Vendor shall develop the firmware (FPGA) required for complete functionality of the card.
3. The Vendor shall fabricate the card as per mechanical form factor of the existing card.
4. The vendor shall procure the components as per BOM.
5. The Vendor shall assemble and test the card functionally as per the ATP document mutually agreed upon.

3.0 Functional Specifications:

The developed card shall have the following functionalities:

1. DC-DC Converter, Filter and Regulator circuits
2. Inrush current Limiter and Transient Voltage suppressor.
3. Current Limiting Circuits
4. LVA (Low voltage Alarm) and PTOR (Power turn on reset) Monitoring circuits
5. SRAM Power and NVM Power control circuits
6. High Voltage shut down circuits
7. RSA Spin motor excitation for Phase A and Phase B
8. LVDT Oscillator and LVDT in-phase and out-phase Drive circuits

4.0 Technical Specifications:

1. DC-DC Converter, Filter and Regulator circuits

The DC-DC converter shall take 28VDC aircraft supply as input and generate regulated outputs of +5VDC, -5VDC, +15VDC and – 15VDC as per the below table.

1.

Sl No.	Output (VDC)	Nominal Voltage (Volts)	SCIH (+/- Volts)	SC/EOL (+/- Volts)	AEC/EOL (+/- Volts)
1	+5V	5.00	0.11	0.13	0.15
2	-5V	-5.00	0.06	0.10	0.18
3	+15V	+15.00	0.23	0.33	0.55
4	-15V	-15.00	0.23	0.52	0.68
5	+15V_EXT_RSAASA	14.83	0.45	0.75	0.83
6	-15V_EXT_RSAASA	-14.83	0.45	0.75	0.83

Note: When 28V_IN less than 16.6 VDC; +5V may decrease to 4.75 VDC, +/- 15VDC may decrease to 14.3 VDC, and +/- 15V_EXT_RSAASA may decrease to 13.75VDC

Regulated DC Loads (Amps) and External Capacitive Loads for the power supplies shall be as per the table below:

Sl No.	Output (VDC)	Capacitive Load (µF)	Min(A)	Typ (A)	Max(A)
1	+5V	63.4µF	3.10	5.00	7.08
2	-5V	45.0µF	0.09	0.13	0.18
3	+15V	31.4µF	0.30	0.50	0.71
4	-15V	31.4µF	0.34	0.52	0.85
5.	+15V_EXT_RSAASA	None	0.070	0.143	0.285
6.	-15V_EXT_RSAASA	None	0.060	0.138	0.275

2. Inrush current Limiter and Transient Voltage suppressor.

The PSU shall also operate during normal transients from 28.0 VDC up to 50VDC and from 28.0 VDC down to 18VDC at the DFCC connector as per MIL-STD-704D.

3. Current Limiting Circuits

Current limiting shall be provided for +15V_EXT_RSAASA and -15V_EXT_RSAASA which will shut down once it trips the current limit which is 0.46A. A protected PSU output shall recover automatically once the output fault (over current or short circuit) is removed.

4. LVA (Low voltage Alarm) and PTOR (Power turn on reset) Monitoring circuits

The 5VDC output shall be monitored for a low voltage condition. LVA-0 shall remain logic high during normal operation. A falling 5VDC output voltage shall cause LVA-0 to transition to low. A rising 5VDC output voltage, causes LVA – 0 to reset to a high. PTOR-0 shall remain logic high during normal operation. The transition of LVA – 0 from a high to low state shall cause PTOR – 0 to also transition from high to low within 1 millisecond.

In addition, if LVA-0 is high, GSE_TEST_RESET-0 and GSE_CONN-0 can override LVA-0 and cause PTOR-0 to go low.

5. SRAM Power and NVM Power control circuits

The PSU shall provide “hold up” power to the DFCC’s SRAMs to prevent data losses due to short duration loss of DC/DC converter +5VDC power.

A control signal 5V_HU_MON shall indicate to the Digital Module whether or not to perform a SRAM initialization following the transition of PTOR – 0 to a high state at power up.

The PSU shall provide power to the DFCC's NVMs that is decay rate controlled.

6. High Voltage Shut Down circuits

The output signals shall be monitored for an overvoltage condition. An overvoltage condition on any monitored output shall engage hiccup mode, which shall temporarily shut down the PSU. Hiccup mode shall remain engaged until the overvoltage condition is removed. The PSU shall automatically recover from hiccup mode once the overvoltage condition is removed.

Once an over voltage has been detected, INH-0 shall be pulled low for 18.3 to 35.6ms.

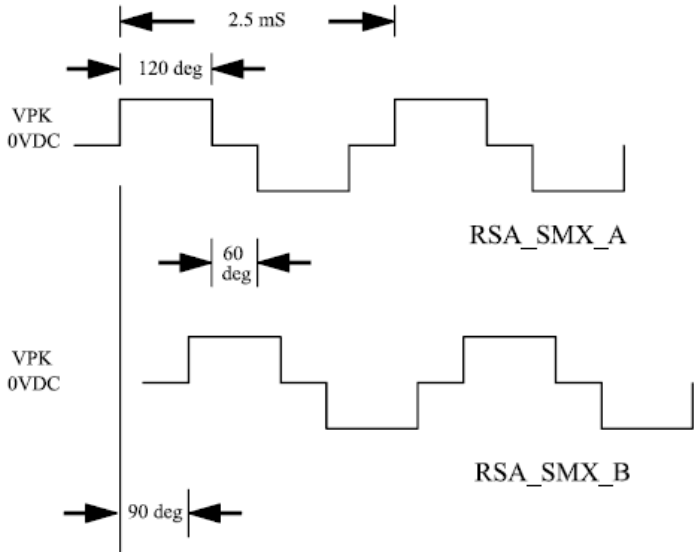
The High Voltage Shut down trip limits shall be as follows:

Sl No.	Output (VDC)	Nominal Voltage (Volts)	SCIH (+/- Volts)	SC/EOL (+/- Volts)	AEC/EOL (+/- Volts)
1	+5V	+5.67	+/- 0.07	+/-0.09	+/-0.10
2	-5V	-5.64	+/-0.10	+/-0.12	+/-0.15
3	+15V	+16.21	+/-0.21	+/-0.26	+/-0.31
4	-15V	-16.30	+/-0.25	+/-0.31	+/-0.37
5.	+15V_RSA	+16.21	+/-0.21	+/-0.26	+/-0.31
6.	-15V_RSA	-16.30	+/-0.25	+/-0.31	+/-0.37

7. RSA Spin motor excitation for Phase A and Phase B

The PSU shall provide excitation for the RSA's spin motors. The PSU shall supply two outputs, RSA_SMX_A– H and RSA_SMX_B– H, to the spin motors that differ in phase by 90 degrees.

The below figure shows the RSA motor excitation signal that shall be generated by the PSU card.



The RSA spin motor oscillator frequency Limits shall be as follows:

Sl No.	Output (k Hz)	SCIH (kHz)	SC/EOL (kHz)	AEC/EOL (kHz)
1	4.791	4.718 to 4.864	4.666 to 4.916	4.619 to 4.963

The RSA spin motor drive performance shall be as follows:

Sl No.	Output parameter	SCIH	SC/EOL	AEC/EOL
1	Voltage	10.5 Vrms to 12.8 Vrms	10.3 Vrms to 12.9 Vrms	10.1 Vrms to 13.0 Vrms
2	Frequency	393 Hz to 406 Hz	388 Hz to 410Hz	384Hz to 414Hz

2. LVDT Oscillator and LVDT Inphase and Outphase Drive circuits

The LVDT excitation function shall consist of an oscillator and 5 separate power op-amps. To avoid beating between channels in the DFCC, the oscillator's frequency shall be programmable based on the PSU's location in the DFCC. The frequency is set by the inputs FREQ_SEL_1 and FREQ_SEL_2.

The frequency generated shall be as follows:

FREQ_SEL2	FREQ_SEL1	FREQUENCY(Hz)
1	1	2778
1	0	3008
0	1	2893
0	0	3123

The LVDT Drive Performance shall be as follows:

Sl No.	**Output Parameter**	**Nominal Voltage (Volts)**	**SCIH (+/- Volts)**	**SC/EOL (+/- Volts)**	**AEC/EOL (+/- Volts)**
1	Voltage	7.07 Vrms	0.31	0.41	0.51

5.0 Power Supply Specification

The 28V DC source to the DFCC is defined as having 28VDC MIL-STD-704D power. The PSU shall operate with a steady state voltage of 15.8VDC to 32.0VDC
The PSU's input power shall be no greater than 149 Watts when supplied with 15.8 to 32.0 VDC at the 28V_IN input and loaded.

6.0 Mechanical Specification

The power supply card should have the same form factor as the existing DFCC MK-I Card.

7.0 Component Specification

All components selected shall be of MIL grade.

8.0 Deliverables

S No	Item Description	Qty
1	Fully assembled and tested DFCC PSU-MKII Card	2 Nos
2	Hardware and Software Design Document	1 set
3	All detailed circuit diagrams, BOM, Mechanical Drawings (in A3 Size paper)	1 set
4	Source Code of Firmware(FPGA) and Gerber Files in CD	1 Nos
5	Acceptance Test Procedure (ATP) and Acceptance Test Report (ATR)	1 set

6	Quality Reports	1 set

9.0 Delivery Time

Six months from the date of release of Purchase Order.

10.0 Vendor Qualification Criteria

- The vendor shall have worked on power supply designs previously especially DFCC PSU MK-II Card. Proof for the same shall be requested by BEL. Failure to furnish the proof shall result in dis qualification.
- The vendor shall have expertise in FPGA design and should have worked on Actel ProASIC3 FPGA's for the DFCC
- The vendor shall have prior experience in circuit analysis and simulation, PCB Layout design and Thermal Analysis.
- The vendor shall have worked on design of LVDT and RSA motor excitation circuits for the DFCC
- The vendor shall have experience in developing air-borne systems/cards compliant to MIL-STD-704D.
- The vendor shall be able to deliver the card with complete functionality tested within the given delivery time.