Security Level: internal

INRUSH CURRENT & RIPPLE & RELAY BOARD

User Guide

Application Department

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Outline

- **INRUSH CURRENT & RIPPLE & RELAY BOARD**
  - *Hardware Placement*
  - *GPIO & Level shift*
  - *Level shift & Decoder*
  - *RAMP Output Control*
  - *Sample Code*

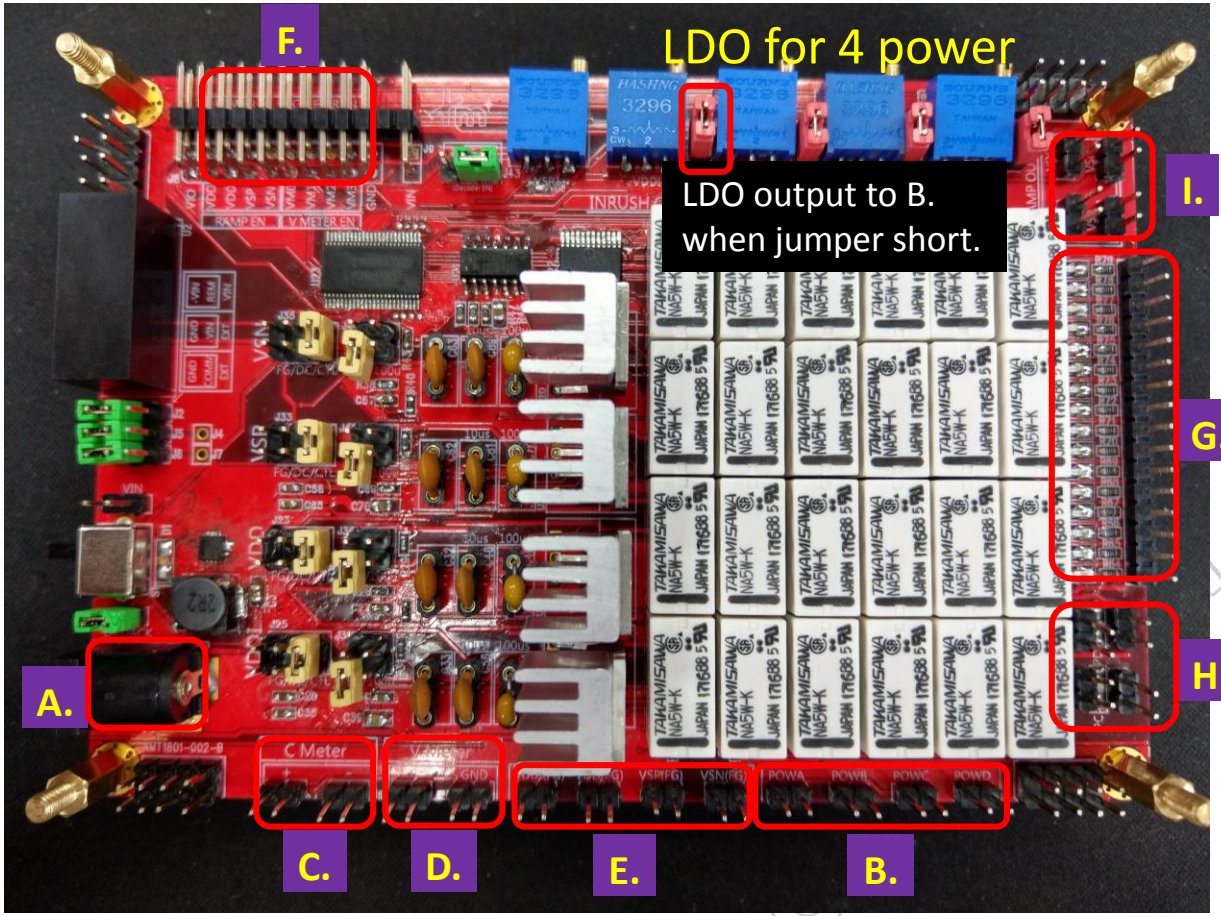
- **Verification items**
  - *Inrush Current*
  - *Power ripple test*
  - *Pass-Fail criteria for ripple immunity test*

Hardware Placement

INRUSH_RIPPLE_
ELAY_BOARD_not

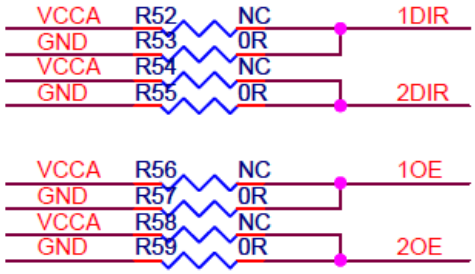
This board can support 4 different power inputs at different time (dependent on GPIO), current measurement (measure current once a power channel) ,16 point voltage measurement (once a voltage measure point) and 4 ramp power output for inrush current and power ripple test.

Part Name	Description
A. +6~+12V System Power	Input +6 to +12V for board use.
B. Power input x 4	User can import 4 diff. power
C. Current Meter (meas. Once a ch)	Connect to current meter
D. Voltage Meter (meas. Once a ch)	Connect to voltage meter
E. Function Generator input x 4	Input power ripple or others.
F. GPIO input	Input GPIO signal for relay control
G. Voltage meas. Point x 16	Connect to the point you want to meas.
H. Power output x 4	Connect to DUT power
I. Power Ramp output x 4	Supply 4 ch ramp power(0.1V/us MAX.)



GPIO & Level shift

1. IO0~3 : For 4bit decoder(detail as below Func. table2)
2. Meter CTRL : For Current Meter ON/OFF(control by GPIO)
3. Power CTRL : For Power ON/OFF(control by GPIO)



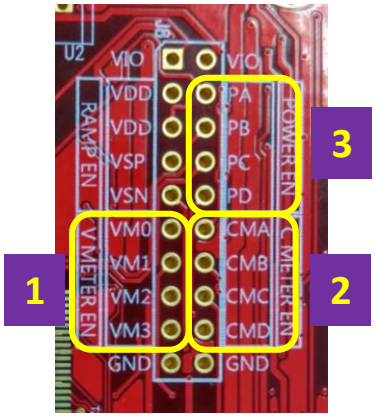


Table 1. Function Table (Each Transceiver)[1]

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

Table2 74HC4514 Function table

FUNCTION TABLE

INPUTS					OUTPUTS														
$\overline{E}$	A_0	A_1	A_2	A_3	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9	Q_{10}	Q_{11}	Q_{12}	Q_{13}	Q_{14}	Q_{15}
H	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	H	H	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L
L	L	L	L	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L
L	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L
L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L
L	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H

Notes

1. LE = HIGH
   H = HIGH voltage level
   L = LOW voltage level
   X = don't care

	PAMP BOARD			FPGA GPIO			
LSB	Low Byte	High Byte	LSB	LSB	High Byte	Low Byte	LSB
D0	VDD	PA	D0	D0	T20	P18	D0
D1	VDDI	PB	D1	D1	T19	P17	D1
D2	VSP	PC	D2	D2	T18	P16	D2
D3	VSN	PD	D3	D3	T17	P15	D3
D4	VM0	CMA	D4	D4	V20	R19	D4
D5	VM1	CMB	D5	D5	V19	R17	D5
D6	VM2	CMC	D6	D6	V18	R16	D6
D7	VM3	CMD	D7	D7	V17	R15	D7
MSB			MSB	MSB			MSB

PA = 1 PAWA output to PA
PB = 1 PAWB output to PB
PC = 1 PAWC output to PC
PD = 1 PAWD output to PD

VDD = 1 RAMP VDD output
VDDI = 1 RAMP VDDI output
VSP = 1 RAMP VSP output
VSN = 1 RAMP VSN output

CMA = 1 Current meter tandem with PA
CMB = 1 Current meter tandem with PB
CMC = 1 Current meter tandem with PC
CMD = 1 Current meter tandem with PD

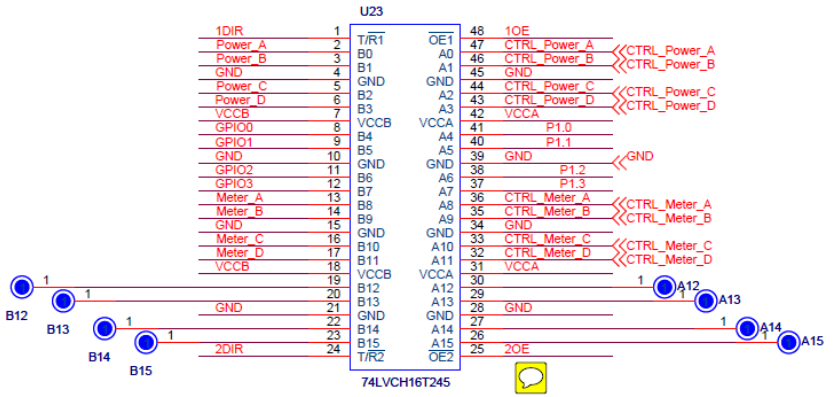
VM0 = 1 Voltage meter decoder D0
VM1 = 1 Voltage meter decoder D1
VM2 = 1 Voltage meter decoder D2
VM3 = 1 Voltage meter decoder D3

※CMX only support one switch on at a time

Level shift & Decoder

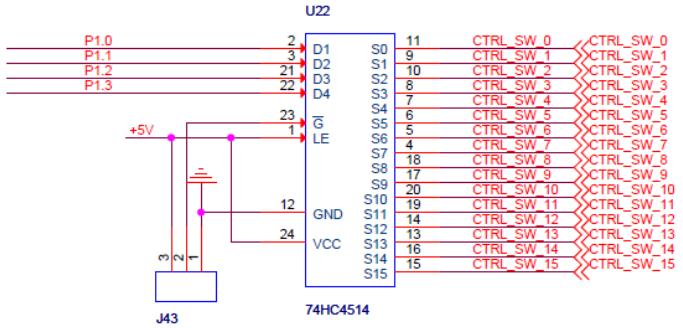
Power and Current meter switch circuit

Power and meter are control by GPIO independently. Power/Current Meter will turn on when GPIO=H.
You can switch on the current meter and power at the same time or sequential.



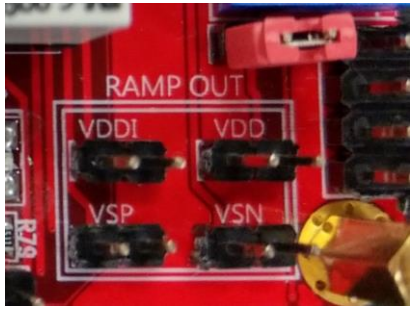
Voltage meter switch circuit

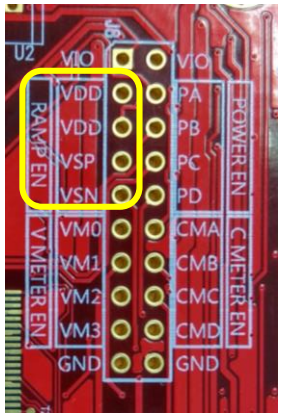
Voltage meter switch is control by 74HC4514(4-to-16 line decoder).
It will switch on one channel at a time.



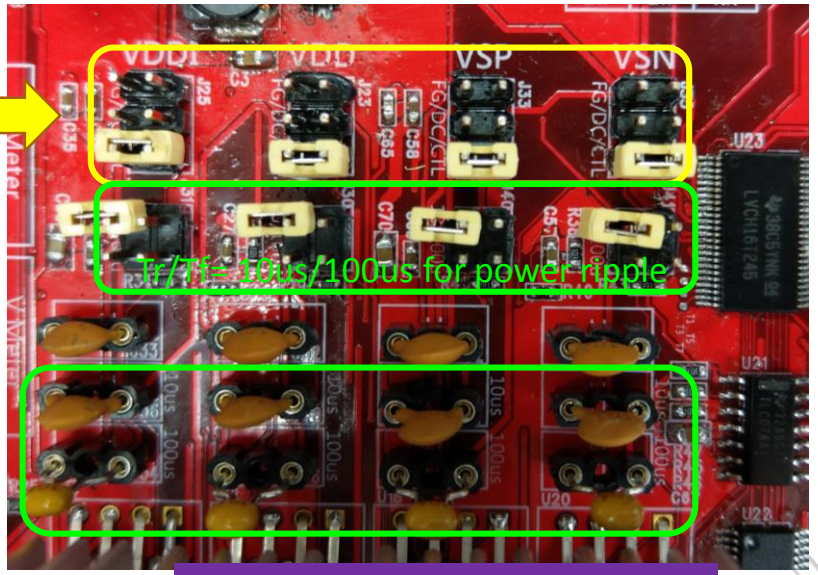
RAMP Output Control

- FC/DC/CTL :
  - FC = Function Generator output to RAMP OUT
  - DC = LDO output to RAMP OUT ,turn on manually.
  - CTL = LDO output to RAMP OUT ,control by GPIO.

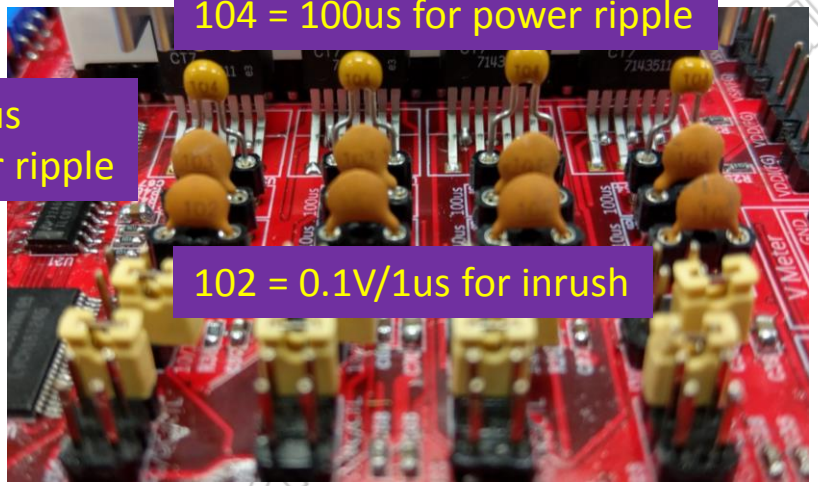




PA = 1 PAWA output to PA
PB = 1 PAWB output to PB
PC = 1 PAWC output to PC
PD = 1 PAWD output to PD



104 = 100us for power ripple



103 = 10us
for power ripple

102 = 0.1V/1us for inrush

Sample Code

PAMP BOARD	D7	D6	D5	D4	D3	D2	D1	D0
High Byte	CMD	CMC	CMB	CMA	PD	PC	PB	PA
Low Byte	VM3	VM2	VM1	VM0	VSN	VSP	VDDI	VDD

```
gpio.dir 0x11 // set direction 0x11 for output
gpio.h.set 0xXX // for GPIO high byte(P18~R15)
gpio.l.set 0xXX // for GPIO low byte(T20~V17)

//E.g. 1 set Power ramp VDDI on
gpio.dir 0x11
gpio.l.set 0x02 //ramp VDDI on

//E.g. 2 set Power PA & PB output
gpio.dir 0x11
gpio.h.set 0x03 //turn PA & PB on

//E.g. 3 set Voltage meter switch to E
gpio.dir 0x11
gpio.l.set 0x00 //set Voltage meter switch to A(idle)
gpio.l.set 0x04 //Voltage meter switch to E
```

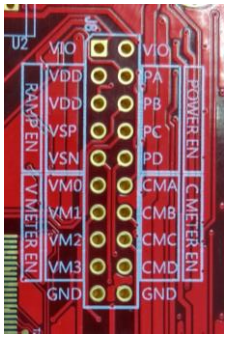
```
//E.g. 4 set Current meter switch to CMC
gpio.dir 0x11
gpio.h.set 0x0F //if we set all power on
delay 100
gpio.h.set 0x4F //Current meter switch on PC
delay 100
gpio.h.set 0x4B //PC off

//Measure current

delay 100
gpio.h.set 0x4F //PC ON
delay 100
gpio.h.set 0x0F //back to original
```

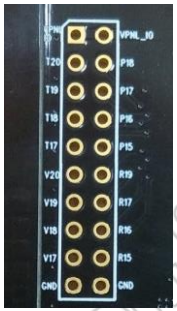
PAMP BOARD

LSB	Low Byte	High Byte	LSB
D0	VDD	PA	D0
D1	VDDI	PB	D1
D2	VSP	PC	D2
D3	VSN	PD	D3
D4	VM0	CMA	D4
D5	VM1	CMB	D5
D6	VM2	CMC	D6
D7	VM3	CMD	D7
MSB			MSB

FPGA GPIO

LSB	High Byte	Low Byte	LSB
D0	T20	P18	D0
D1	T19	P17	D1
D2	T18	P16	D2
D3	T17	P15	D3
D4	V20	R19	D4
D5	V19	R17	D5
D6	V18	R16	D6
D7	V17	R15	D7
MSB			MSB

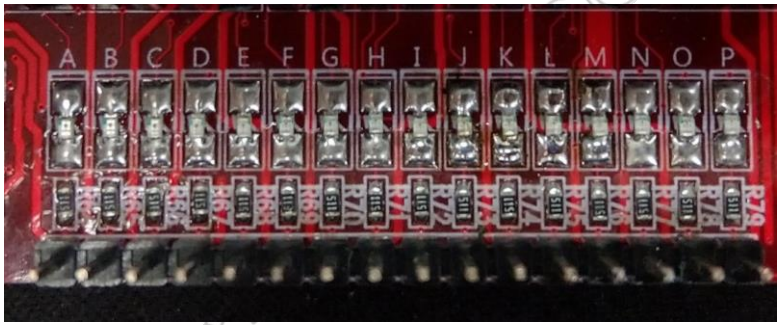




PA = 1	PAWA output to PA	VDD = 1	RAMP VDD output
PB = 1	PAWB output to PB	VDDI = 1	RAMP VDDI output
PC = 1	PAWC output to PC	VSP = 1	RAMP VSP output
PD = 1	PAWD output to PD	VSN = 1	RAMP VSN output

CMA = 1	Current meter tandem with PA	VM0 = 1	Voltage meter decoder D0
CMB = 1	Current meter tandem with PB	VM1 = 1	Voltage meter decoder D1
CMC = 1	Current meter tandem with PC	VM2 = 1	Voltage meter decoder D2
CMD = 1	Current meter tandem with PD	VM3 = 1	Voltage meter decoder D3

※CMX only support one switch on at a time



Inrush Current

Display Module ctrical Verification

ElectricalDSITest Template

- **Power On Inrush Current tests**
  - Supply voltages: VDD=2.75V or VPNL = 3.7V, VDDI=1.80V, panel voltages AVDD=ex.+5.4V AVEE=ex.-5.4V (panel voltage DC-level may differ depending on the display module architecture)
  - Waveform of max inrush current spike is captured
  - Display image data shall be written to display module before the tests.
  - The test cases are listed in the relevant Microsoft Test Report Template.
  - Pass/Fail criteria: the limits specified in the display module specification shall be met.

- **Peak Current test in Normal mode**
  - The purpose of the Peak Current test is to measure the peak current of the display module during operation. Measurement set up is the same as in the Power On Inrush Current test.
  - Conditions:
    - Supply voltages: Vdd=2.75V or VPNL = 3.7V and Vddi=1.80V panel voltages Avdd=ex.+5.4V Avee=ex.-5.4V (panel voltages may differ depending on the display module architecture)
  - Test images are defined in the relevant Microsoft Test Report Template
  - Waveform of max peak current spike is captured
  - Display image data should be written to the display module before the test.
  - Test cases:
    - The test cases are listed in the relevant Microsoft Test Report Template.
    - Pass/Fail criteria: the limits specified in the display module specification shall be met.

Power ripple test

- **Ripple Immunity test**
  - Supply voltage Ripple Immunity requirements for display modules are defined in display module specifications. Ripple Immunity test purpose is to verify how tolerant display module is against ripple that may occur in the power lines.
  - **Ripple Immunity test set up**
    - There are two different ripple tests:

1) Supply voltages: VDD, VDDI, AVDD and AVEE
   Ripple frequency range: 1 Hz - 100 MHz
   Ripple signal waveform: Sine wave, 100mVpp

2) Supply voltages: VPNL/VBAT
   a) GSM-TX simulation:
      Ripple frequency range: 205Hz - 225Hz
      Step: 1 Hz
      Ripple signal waveform: Pulse waveform,
      Duty cycle low pulse 12-15%
      SR=200kV/s, 500 mVpp

   b) Pulse waveform test:
      Ripple frequency range: 1Hz - 30kHz
      Ripple signal waveform: Pulse waveform,
      Duty cycle 50%
      SR=200kV/s, 500 mVpp

Pass-Fail criteria for ripple immunity test

1) VDD, VDDI, AVDD, AVEE: 1 Hz - 100 MHz; sine wave, 100 mVpp

There shall be no abnormal visible effects on the display.

When critical frequencies are found, suppliers have to agree with Microsoft about the corrective actions.

2) VPNL/VBAT: GSM-TX and 1 Hz - 30 kHz pulse waveform 500 mVpp

a) GSM-TX simulation:

There shall be no abnormal visible effects on the display.

b) Pulse waveform 1 Hz - 30 kHz test:

There shall be no abnormal visible effects on the display.

When critical frequencies are found, suppliers have to agree with Microsoft about the corrective actions.

Thank You !