PSD@CBM firmware description (draft, for internal use)

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Actual version of the document is avaliable at github:
`https://github.com/dfinogee/PSD-readout-manual/raw/main/PSD_readout_manual.pdf`

Contents

1 ADC data processing

1.1 Channel data collecting

Each channel collect data in FIFO (chdata_fifo) in hit packet format and emit ready signal after data stored in fifo. Ready signal is synchronous to signal threshold crossing and used for event ADC timestamp fig. 1. It is implemented in PSD_channel_calc.

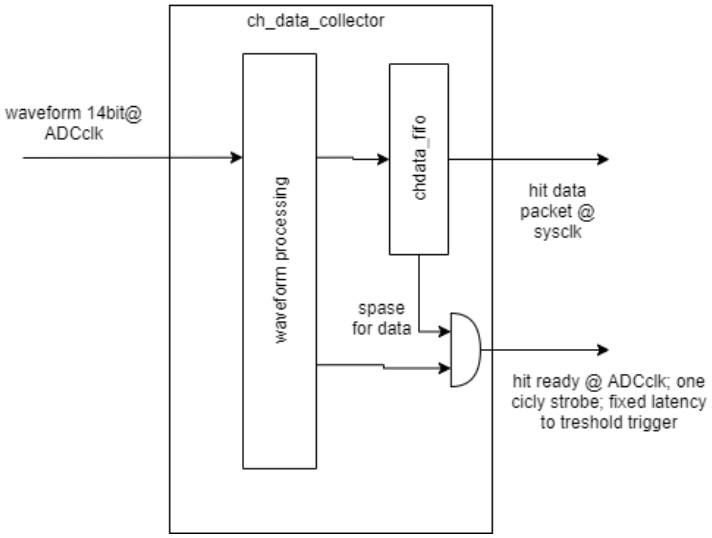

Figure 1: Channel data collecting scheme

Mean hit rate per channel = SYSCKL / total channels + 2 sys cycle / packet length. SYSCKL = n * ADCclk = 240MHz; total channels = 32; packet lenght = 1. Max mean hit rate is 7 MHz. (0.78 MHz with 80MHz and 2 waveform packets; 2.2 for 10 channels)

Hit packet forming is implemented in ch_data_colletcor with three fifos. raw_waveform_fifo write raw ADC data by wf_strobe signal. header_ch_fifo store zero level (if future all data avaliable at the beginning of waveform calculation) by strobe start signal. calc_ready signal raised for one cycle when charge (fit in future) is ready. By calc_ready signal hit header with charge and data from header_ch_fifo is written to chdata_fifo, header_ch_fifo is readed, counter started to read raw_waveform_fifo. fig. 2 Represents forming hit packet.

todo: data with out raw data todo: ch ready signal after packet pushed todo: readout rate, missing packets

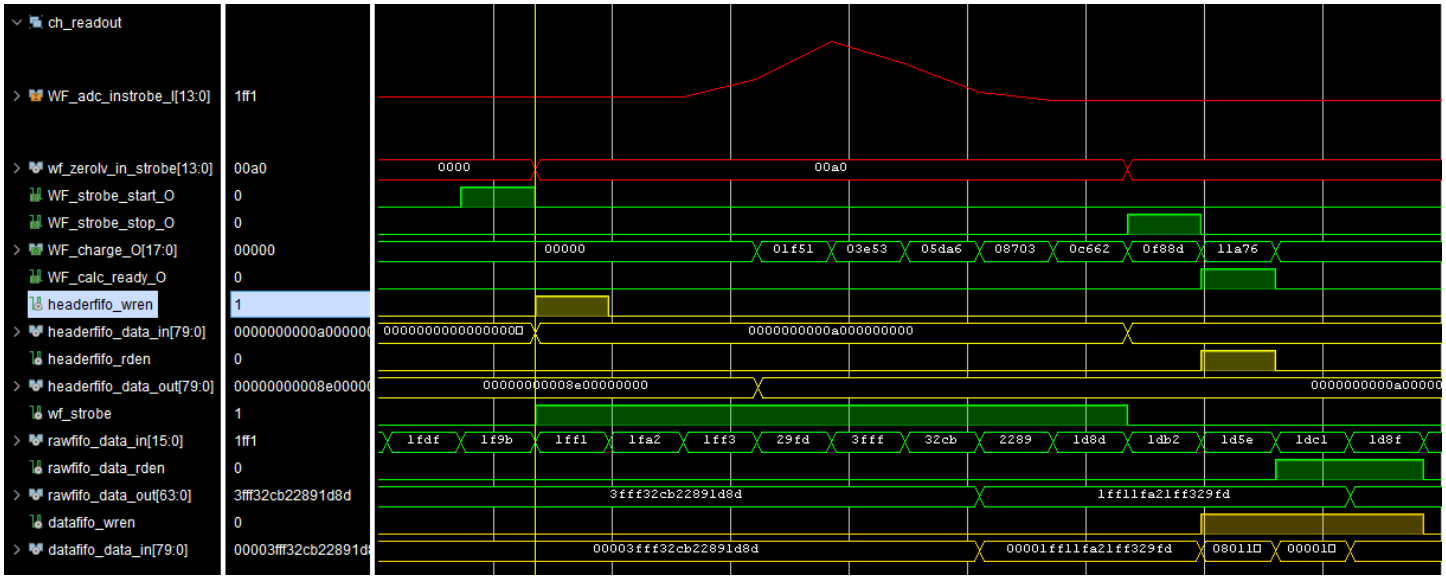

Figure 2: Channel data collecting signals

word	79 .. 72	71 .. 64	63 .. 34	33 .. 16	15 .. 0
1	num data words	channel	0x0	signal charge	waveform zero level

Table 1: hit packet header.

word	79 .. 64	63 .. 48	47 .. 32	31 .. 16	15 .. 0
1	0x0	waveform point n	waveform point n+1	waveform point n+2	waveform point n+3

Table 2: hit packet data word.

1.2 Data collecting from channels fifo

Each channel generate single strobe with fixed latency to threshold crossing indicating waveform measurement. 32 bit strobe word is trored to data_wf_calc_fifo with mc index and ADC timestamp. FSM read stored strobes and collect data from fired channels storing outputs to common_data_fifo, each event header word with timing and size info stored in common_header_fifo. Shematic represented on figure 3.

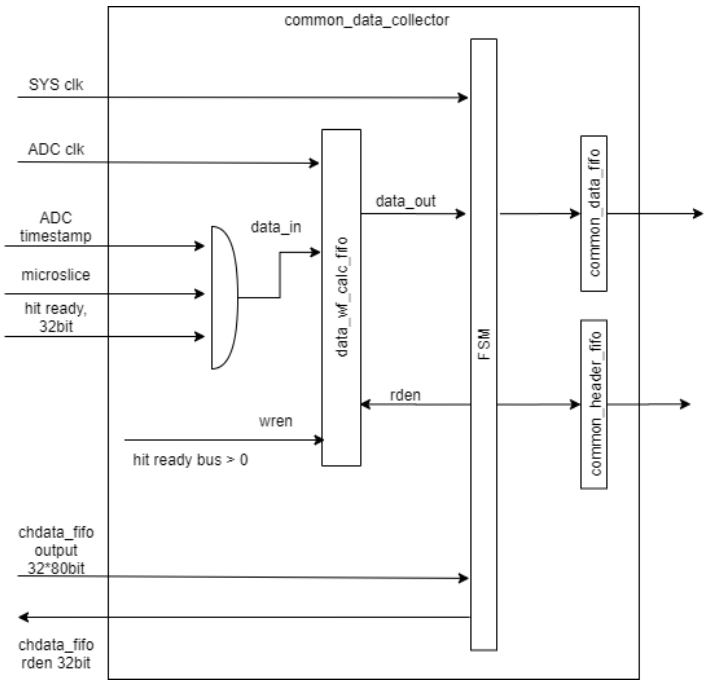

Figure 3: Data collecting scheme from all channels fifos

FSM is switched from wait to start state when data_wf_calc_fifo_isempty became '0' and fifo output is latched. Priority encoder show next fired channel from strobe and data collected from fired channel to common_data_fifo with hit_packet_iterator. input to priory encoder is shifted to bit after fired channel when iterator reach last number. Priority encoder could be equal or less than 32 bit. Simulation outputs presented on figure 4.

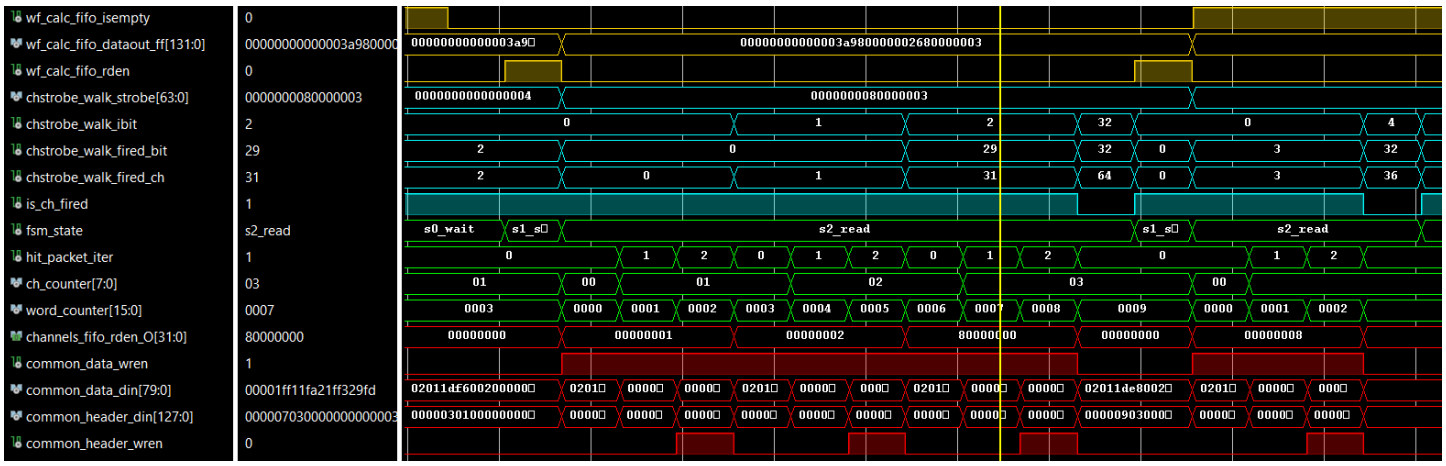

Figure 4: Data collecting signal from all channels fifos

todo: waveform bias todo: data without waveforms todo: reset wignal for data and sys clocks. todo: readout rate, missing packets

2 ADC control

2.1 control registers

addr	31 .. 30	29 .. 28	27 .. 24	23 .. 20	19 .. 16	15 .. 14	13 .. 12	11 .. 8	7 .. 4	3 .. 0
0	0x0	threshold ch1				0x0	threshold ch0			
1	0x0	threshold ch3				0x0	threshold ch2			
2	0x0	threshold ch5				0x0	threshold ch4			
3	0x0	threshold ch7				0x0	threshold ch6			
4	0x0	threshold ch9				0x0	threshold ch8			
5	0x0	threshold ch11				0x0	threshold ch10			
6	0x0	threshold ch13				0x0	threshold ch12			
7	0x0	threshold ch15				0x0	threshold ch14			
8	0x0	threshold ch17				0x0	threshold ch16			
9	0x0	threshold ch19				0x0	threshold ch18			
10	0x0	threshold ch21				0x0	threshold ch20			
11	0x0	threshold ch23				0x0	threshold ch22			
12	0x0	threshold ch25				0x0	threshold ch24			
13	0x0	threshold ch27				0x0	threshold ch26			
14	0x0	threshold ch29				0x0	threshold ch28			
15	0x0	threshold ch31				0x0	threshold ch30			

Table 3: ADC channels threshold control.

addr	31 .. 28	27 .. 24	23 .. 20	19 .. 16	15 .. 12	11 .. 8	7 .. 4	3 .. 0
16	0x0				waveform length 0..3 [(reg+1)*4]	strobe offset 0..12	control bits	
17	negative channel mask ibit = ich							

Table 4: ADC readout control.

bit	description
0	send waveform
1	ms gen standalone
2	readout fsm reset
3	errors reset

Table 5: Control bits

addr	31 .. 18	17 .. 17	16 .. 16	15 .. 8	7 .. 7	6 .. 0
18	0x0	WR	ENA	DATA	0x0	ADDR

Table 6: HV control via I2C.