

MODEL 430B SUPER I/O BOARD

INTRODUCTION

The OSI Model 430B is possibly the most powerful I/O Board available to the hobbyist. It is designed to provide on one board all the interfaces commonly used by the hobbyist. The board's low cost makes it economical even when only one of its several interfaces is used, and dozens of OSI 430B Boards can be used in a system.

The board can be maximally populated with an 8-bit tracking A/D converter, 8-channel analog multiplexer, two 8-bit D/A converters, a UART based audio cassette or RS232 interface, a Z-axis unblank one-shot, eight parallel input lines, eight parallel output lines (latching), and five fast single-pulse output lines.

The board can be configured for an ASCII or Baudot teletype, for FSK communications or RS232 instead of a cassette interface. If the A/D Converter is not used, 8 additional input lines are available. If the two 8 bit D/A converters are not used, three 8 bit output latches are available for other uses. Because of the complexity of the 430, the theory of operation of the board should be well understood before construction is begun.

THEORY OF OPERATION

To simplify this discussion, the board will be described in functional blocks.

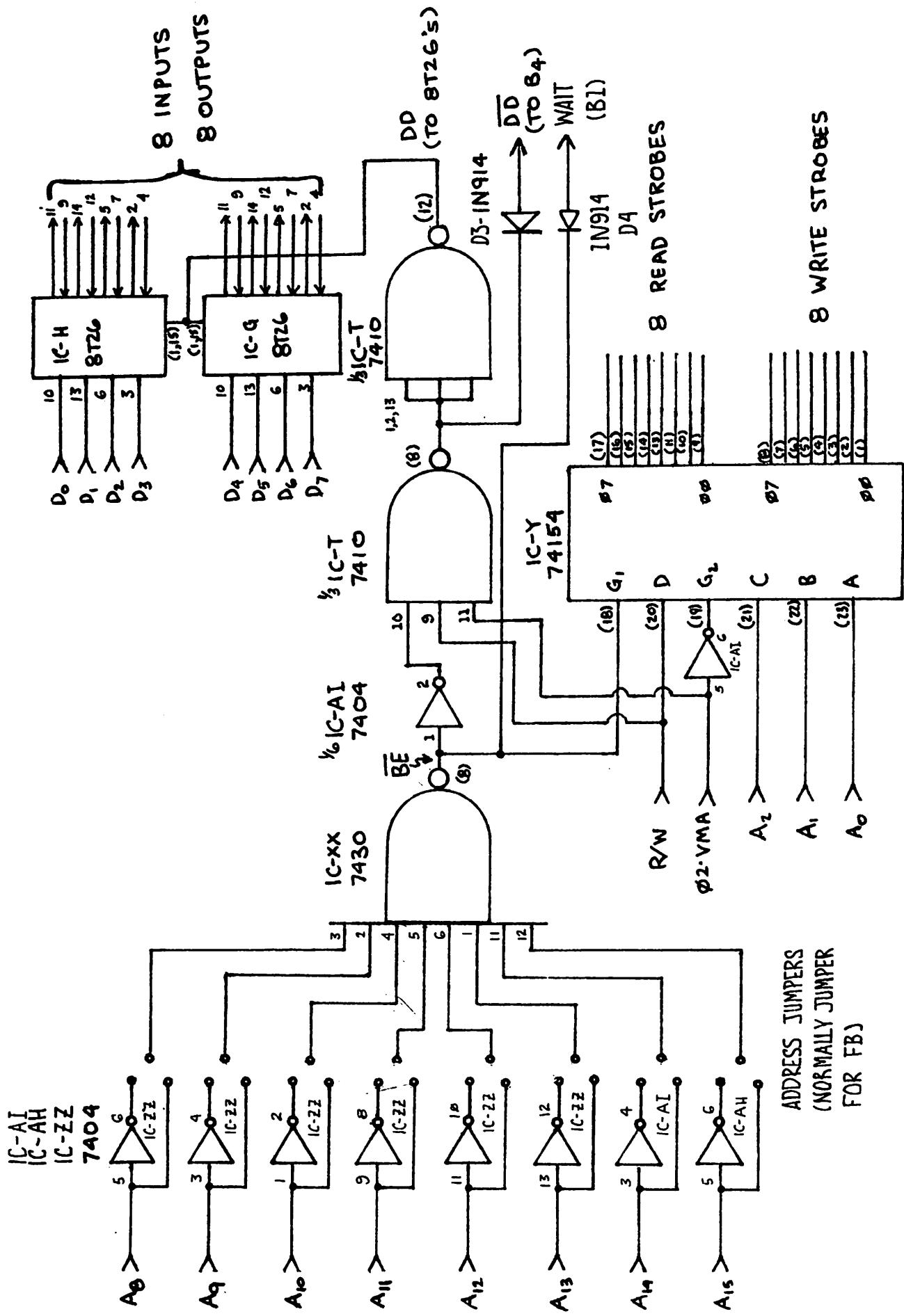
Address Circuitry

Refer to Diagram 1 in conjunction with this discussion. The board's address is set in the lower right corner of the board. For normal purposes the board must occupy FBXX to be compatible with OSI software. This address is set in foil, but for special purposes the tapes can be cut and any address jumpered in. The jumpers select non-inverted or inverted address lines A₀ through A₁₅ as the eight inputs to a 7430 nand gate which is \overline{BE} . \overline{BE} is inverted and nanded with $\emptyset 2 \cdot VMA$ and R/W to generate the Data Direction signal \overline{DD} through a 1N914 diode to B₄. This line is also inverted and fed to the 8T26 data buffers. \overline{BE} and $\emptyset 2 \cdot VMA$ enable the 74154 four to sixteen line decoder. The decoder generates a low on one output line in step with $\emptyset 2$ defined by the state of A₀, A₁, A₂ and R/W. This circuitry generates eight read strobes addressable by reading locations 00-07 on the board and eight write strobes by writing at locations 00-07 on the board. The use of these strobes directly is the simplest form of interfacing on the board. Each strobe pulse is only as long as $\emptyset 2$ but can be stretched via the 74121 or 74123 one shot on the board. The use of a strobe as an interface control line has several advantages over a line of a parallel output interface in some applications.

First of all, the output is non-latching so that no program steps are required to reset it. Secondly, the output requires fewer program steps because no data need actually be outputted.

The data direction lines are fed out to the bus and the 8T26 data buffers. These buffers separate the bi-directional bus signals into two unidirectional bus signals.

The circuitry is used by all other board circuitry.



Serial Interface

The central portion of the 430 Board is the generalized serial communications area. The system is based on an S1883 UART at IC-S (Diagram 2). The S1883 is an "industry standard" device which is interchangeable with several other manufacturer's parts. The complete specifications sheets for the S1883 UART are attached as Appendix 1. The user should carefully read this spec. sheet before proceeding.

Diagram 4 shows the 430 Board implementation of the UART. Both the transmitter and receiver status words are fully programmable by the CPU. Unlike the ACIA on the 400 CPU Board, the UART can be programmed for five level code, allowing it to handle Baudot code. Transmit and receive clocks at 16 times the Input/Output frequency and some form of input and output circuitry are required to use the UART.

The UART input and output signals can be tailored for Kansas City Standard Audio Cassette, RS232 interface, or 20ma teletype interface. Diagram 5 shows the latter two. The 430B does not implement the 20ma interface. However, the user can implement it in an off-board proto area if desired. For 60ma loops, two 7417 buffers may be paralleled and the pull-up resistors on transmit and receive should be adjusted accordingly. The 7417 can be used with compliance voltages up to 15 volts. If a 7407 is substituted, 30 volts is a maximum.

RS-232 Interface

The RS-232 interface used on the Model 430B is shown in Diagram 3. a 16X baud rate clock is used on both receiver and transmitter clock inputs. For some applications, it may be desirable to provide separate clocks. This can be done by cutting the foil between pin 40 of the UART and the small pad under the UART on the rear of the board. Jumper the external clock to the large pad near pin 1. The UART is now

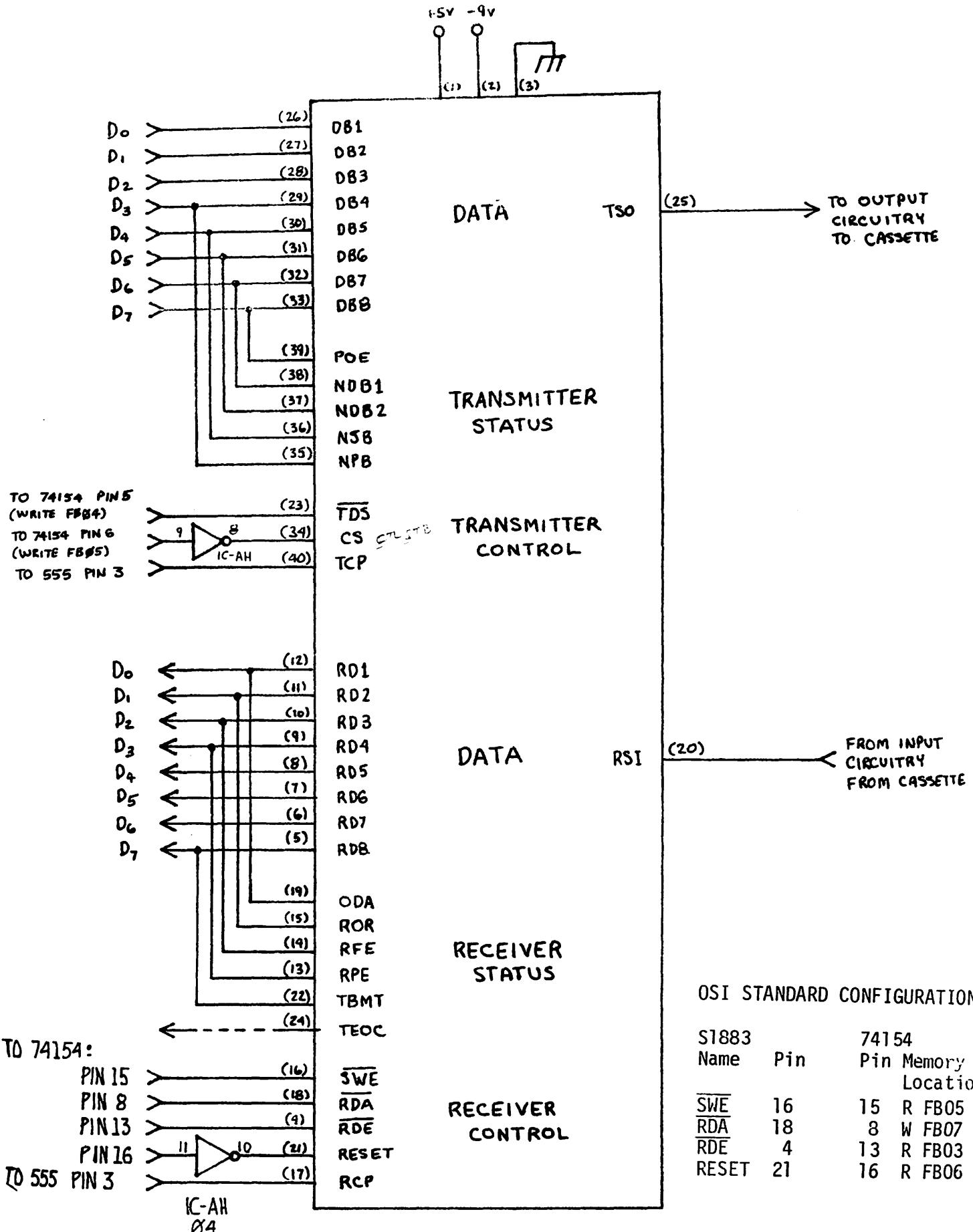
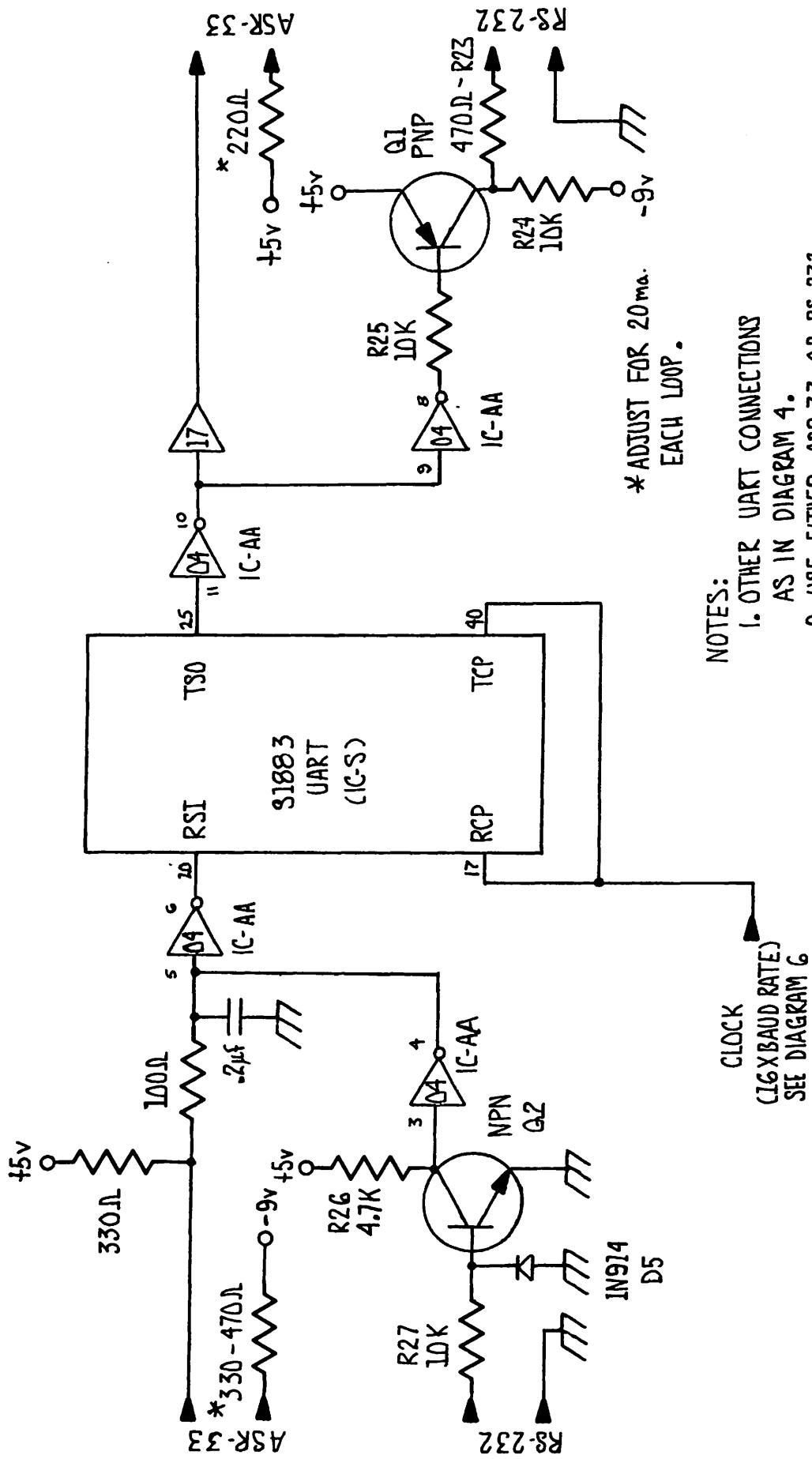


DIAGRAM Z - UART



NOTES:

2. USE EITHER ASR-33 OR RS-232.
 3. ASR-33 SHOWN FOR REFERENCE ONLY.
 - IT IS NOT IMPLEMENTED ON 430 BOARD.

DIAGRAM 3 - ASR-33 AND RS-232 INTERFACE

configured to use the on-board transmitter clock and external receiver clock. Note that the receiver clock must be 16X the receiver baud rate.

Audio Cassette

Since the UART has an accessible 16X clock, it will accept any of the commonly available audio cassette interface kits and virtually any digital cassette such as the National Multiplex CC-7A. However, the 430 Board has complete provisions for its own audio cassette interface.

The 430 Board's audio cassette or, more exactly, audio tape interface is designed to be compatible with the popular Kansas City Standard for Audio Cassette, so called because it originated from a meeting held in Kansas City by Byte magazine in late 1975. Byte magazine Vol. 1, issue 7 (March 1976) was devoted to the Kansas City Standard Audio Cassette and should be studied in conjunction with this discussion.

Basically, the format is as follows. Serial data (marks and spaces or highs and lows) are converted into audio tones. One bit of mark (high) is converted to eight cycles of a frequency 8 times the baud rate and one bit of space or low is converted into four cycles of a frequency four times the baud rate. Table 1 lists the pertinent data for this standard at different baud rates.

TABLE 1

Baud Rate (us)	16X Clock (Hz)	Mark (Hz)	Space (Hz)	Receive One Shot (μs)
110	1760	880	440	1515
300	4800	2400	1200	555
600	9600	4800	2400	278
1200	19200	9600	4800	140

Audio cassettes, the most popular tape media, are operated at 300 baud. This is because the 2400 Hz and 1200 Hz tones are easily handled by "voice quality" circuitry of cheap tape recorders. The best cassette decks can be operated at 600 baud, and good reel to reel recorders can be operated at 1200 baud.

Diagram 4 shows the clock circuitry of the serial interface subsystem. The 555 generates both transmitter and receiver clock pulses. The UART receiver is somewhat sensitive to the clock waveform; R13 may have to be trimmed for a symmetric clock waveform. Refer to Appendix 1 for data sheets covering component selection for various baud rates and symmetry. Alternatively, the board can be modified for an external receiver clock. Refer to the RS232 interface section for details.

Diagram 4 also shows the audio cassette transmitter. The first stage of the 7476 divides the clock frequency by one for a "mark" and two for a "space". The second stage always divides by two, producing the Kansas City format. The resistive divider R15-R16-R17 adjusts the voltage levels to the proper input levels for the recorder, while C8 rounds the corners of the square waves. C8 is optimized for 300 baud, and should be adjusted for each baud rate. LED 1 is a transmitter activity indicator. It lights each time the UART outputs a "space" condition.

The audio cassette receiver is shown in Diagram 5. A CA3130 converts the incoming signal, which is approximately a sine wave, into a TTL-level square wave. Diode clamps D1, D2 protect the input. Dual inverters are used to increase the fanout. C10 improves the noise immunity of the system by providing hysteresis at the inverter. A 74123 retriggerable one-shot decodes "mark" and "space" conditions.

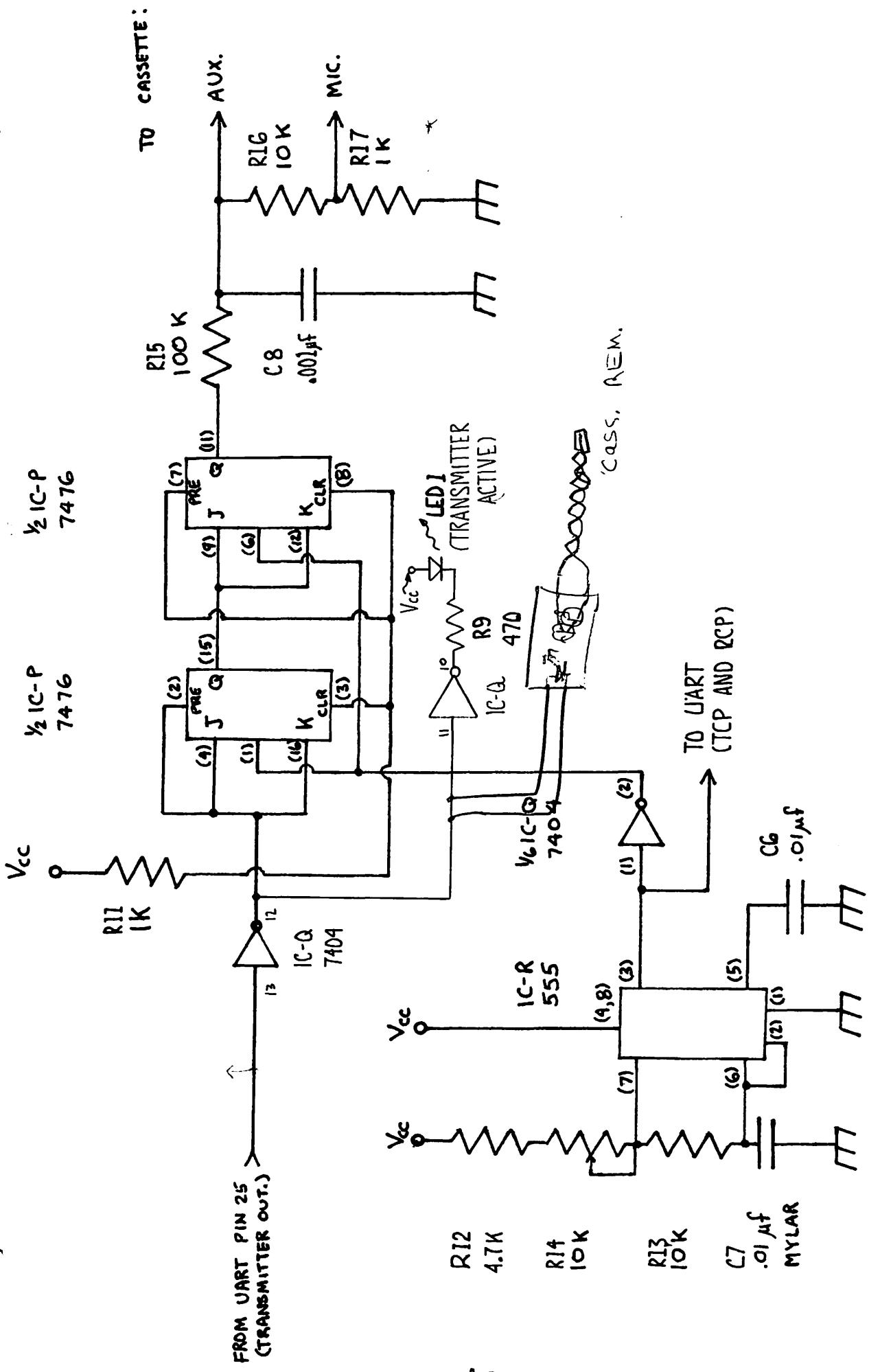
R18 adjusts the one-shot for a period midway between the high and low frequencies. A 7474 latches the output of the one-shot on the positive edge of every cycle of the input. On low frequencies ("space" condition) the one-shot times out, so a low is entered to the 7474 on the next cycle. On high frequencies the one-shot is retriggered before it times out, so its output is always high. The 7474 reads this on the next cycle. The 7474's output is a reconstruction of the original UART output. The inverting output of the 7474 is used to drive an LED receiver activity indicator, which lights whenever a "mark" is received.

Since the receiver clock runs independently of the received data, the inputed data must be at nearly the same baud rate as the clock, and must remain at that rate throughout playback. The tolerable baud rate difference depends on the framing action of the UART and the symmetry of the clock, and is on the order of a few percent. This is more than adequate for any "hi-fi" tape recorder.

If an OSI V series PROM is on-line, the tape interface can be used immediately on system power up. Reset the processor, then type "L" on the keyboard. The monitor transfers control from the keyboard to the UART. The cassette now has full control of the computer allowing it to perform any function normally entered from the keyboard. This includes the full range of monitor commands. It is thus possible to load a program, then, under cassette control, commence execution and return control to the keyboard.

OSI Auto-Load™ cassettes make full use of this feature. To load Blackjack, for example, just insert the cassette, type "L", and sit back. When the program is loaded the computer automatically displays the game instructions, and it's ready to go!

DIAGRAM 4- AUDIO CASSETTE TRANSMITTER



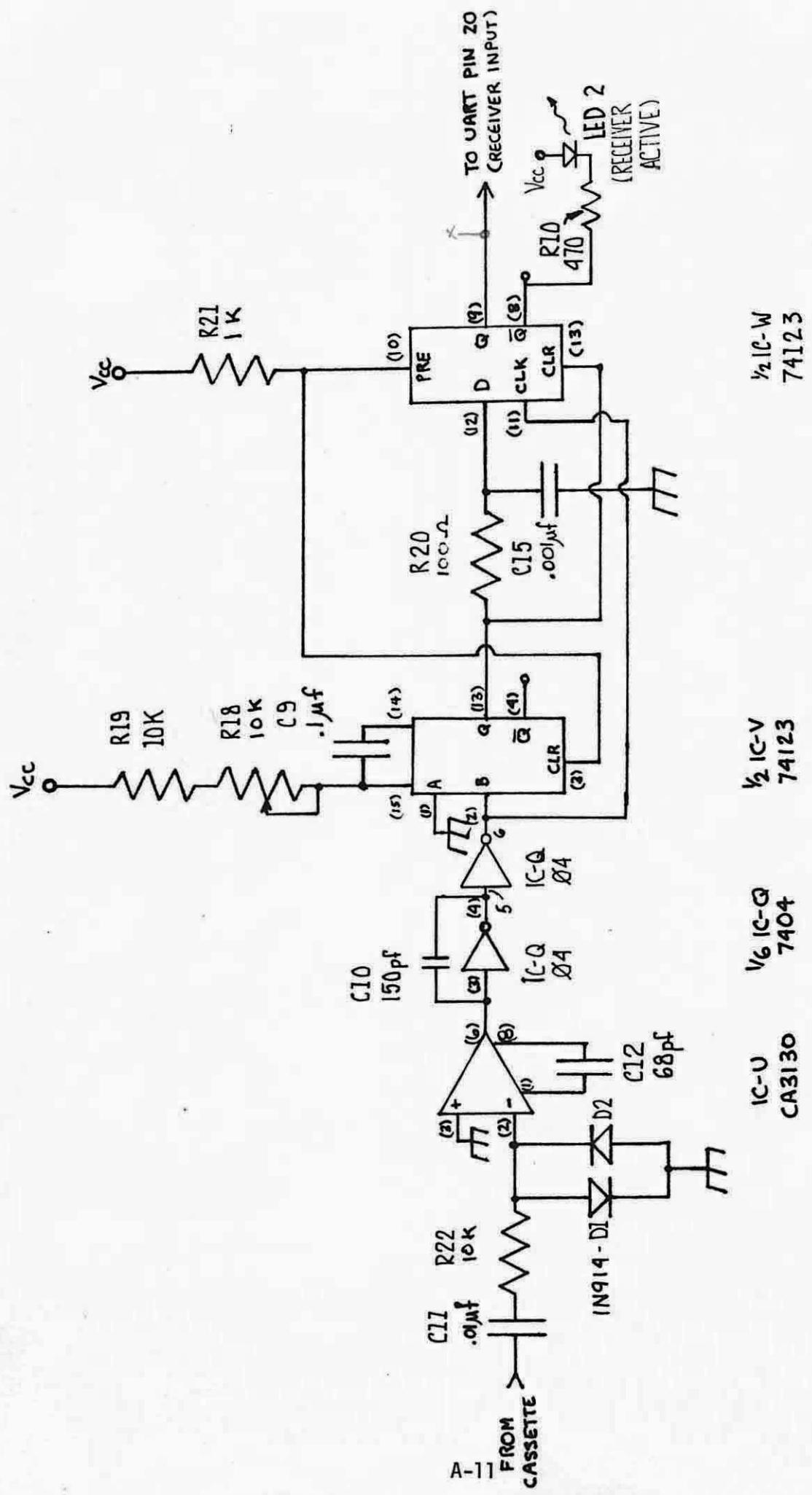


DIAGRAM 5 - AUDIO CASSETTE RECEIVER

D/A Converters

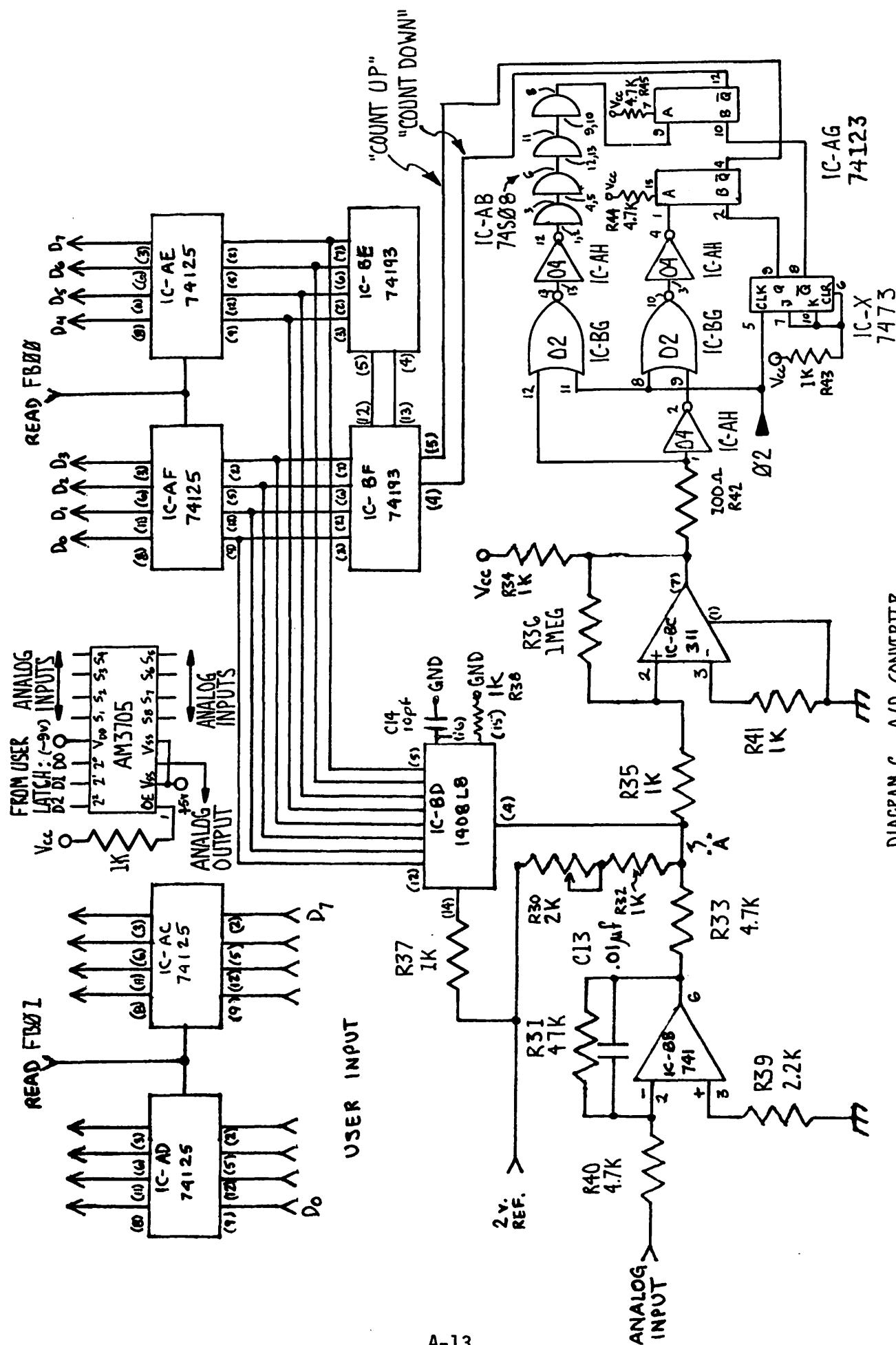
The Model 430 will accommodate up to two D/A converters, plus a one-shot for CRT unblank control (Diagram 7). Input data to the 1408L8 converters is latched via two 7475 latches. Additionally, one latched 8-bit output port is available to the user at IC-I and IC-J. The output lines are brought out to C5-C12.

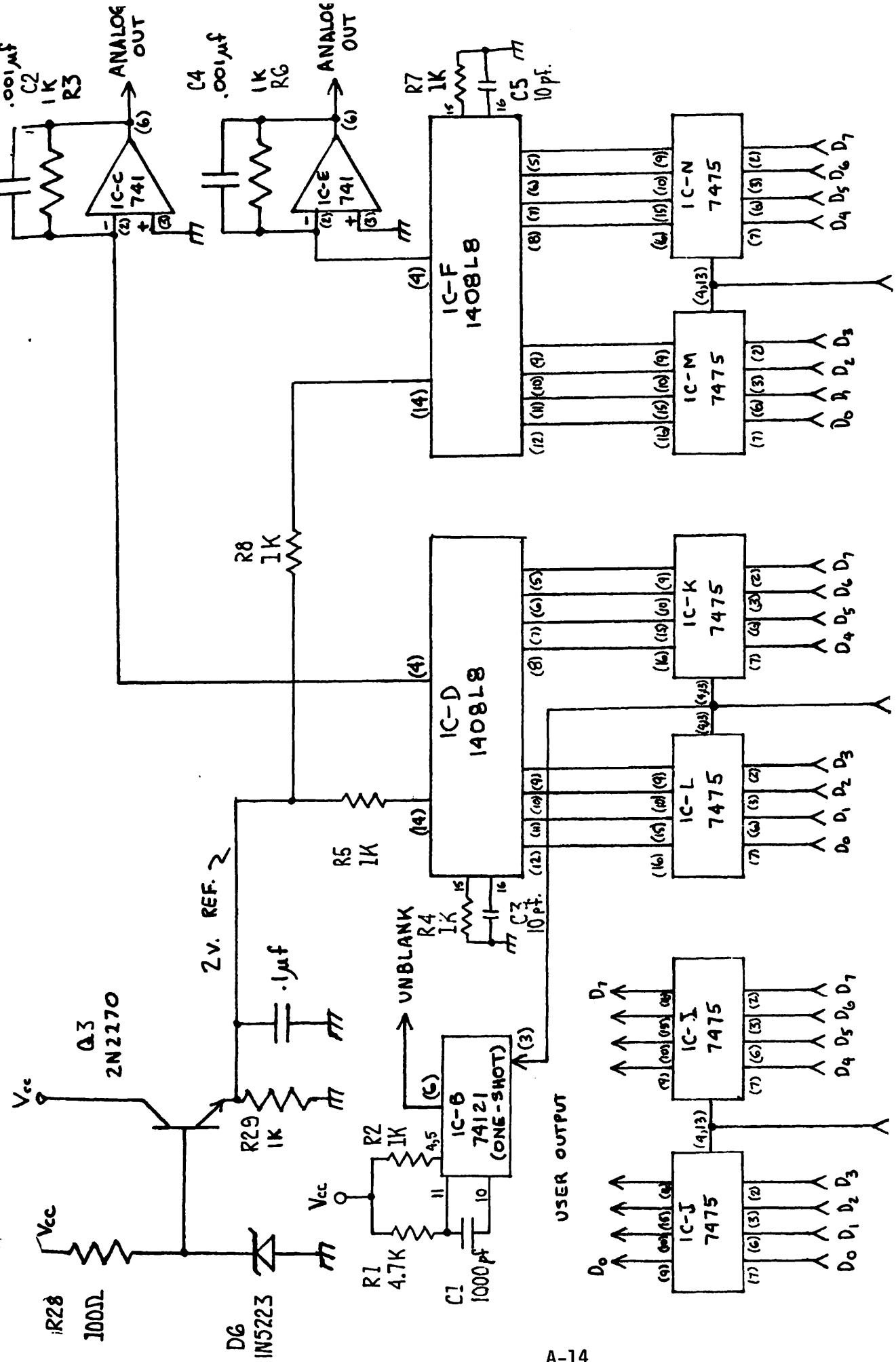
The 1408L8 converters require a two volt reference provided by a zener diode and emitter follower. The outputs of the D/A converters are currents which are converted to voltage outputs via the op amps. 741 op amps can be used for low speed applications such as audio output but faster op amps such as 5556s should be used for CRT graphics. The gain of the op amp is determined via the feedback resistors and the bandwidth can be controlled by feedback capacitance. The FB01 D/A's strobe is also fed to a 74121 one shot which is triggered via the negative edge of the strobe. This one shot would be used to control the z-axis of a CRT for dot graphics. The FB00 D/A converter would be loaded with one coordinate, then the FB01 D/A would be loaded with the other. Immediately on loading the second converter, the one shot would fire, unblanking the screen for a few microseconds, forming a dot. This eliminates smearing during the loading of the D/As and protects the phosphor from burns if the D/As are not constantly being loaded.

In applications requiring only one D/A converter, OSI software assumes the converter is located at FB01. The user should build up this converter first.

A/D Converter

The lower left corner of the board contains the A/D converter, 8 channel multiplexer, and 8-bit parallel input (Diagram 6). If the





WRITE FBG2

WRITE FBG1

DIAGRAM 7 - D/A CONVERTERS

WRITE FBGA

A/D converter is not used an additional 8-bit input port is available at IC-AE and IC-AF.

The synchronous tracking A/D converter is very simple to use. It counts using θ_2 (not $\theta_2 \cdot VMA$) and therefore is always in sync with the processor. This means that the output of the converter can be read as any other memory location to obtain the current digital value of the input waveform.

The two 74193 up-down counters are clocked by θ_2 and controlled by the LM311 comparitor. An enable pulse is applied to the "A" input of the appropriate one-shot. The one-shot is also enabled at the "B" input by the 7473 on every other clock cycle. This prevents the counters from attempting to simultaneously count up and down, which can occur occasionally on transitions. The 74S08 delay line eliminates race conditions which also can occur on transitions. The output of the counters is fed to both the input port and a 1408L8 D/A converter. The converter provides an output current to the current summing junction (A) proportional to the digital number present at the output of the counters. When this current just cancels the input current from the op amp (representing the analog input) and the zero control pot R30, the comparitor switches which causes the counter to switch. This brings the current out of balance which causes the comparitor to switch again. Thus, the converter always oscillates one least significant bit with a constant input. As the input varies, the comparitor will switch and the counters will follow or track the input signal. The fastest that the converter can move is one-half of θ_2 bits-per-second. If the input is adjusted for ± 1 volt input (via the zero pot and the feedback resistor on the op amp), then 128 bits correspond to 1 volt. At a θ_2 of 1MHz, the

converter will track at 3900V/sec. At 3 MHz, it will track at 11500V/sec. The converter will track a triangle wave with the full voltage range of the converter at 1 KHz for a 1 MHz system and 3 KHz for a 3 MHz system; at half amplitude the frequency will be twice as high and so on. This type of converter is ideal for audio digitization since its conversion rates closely match the requirements for audio inputs. The converter can also be used with a multiplexer to monitor several analog voltages. Since it takes a maximum of 512 clock cycles per conversion, this would allow multiplex rates of nearly 2 KHz for a 1 MHz system or 6 KHz for a 3 MHz system. This converter is clearly much faster than anything else available to the hobbyist!

Analog Multiplexer

The Model 430B allows up to eight analog inputs to be multiplexed using an AM3705. Possible applications include multiplexing several audio channels, monitoring remote sensors such as thermisters, or in games.

The desired input channel is selected by setting up data bits D0-D2 at the user output latch (IC-J), address FB02. Note that if the multiplexer is used, the "analog input" line at connector C36 cannot be used.

Notes on Model 430A:

If your Challenger contains an "A" series board (designated by no letter after 430), note the following differences on your board:

- (1) Several modifications to circuitry have been made which are not in foil on the "A" series board. On any options which you install, refer to the schematics for additional parts. You may have to tack-solder some parts in where no pads exist for them. If you are installing a UART-based option, refer to Diagram 2 for jumper configurations.
- (2) If installing the 555 clock: on capacitor C7, cut the line which runs to ground near IC-M and jumper that side of C7 to ground near IC-R.
- (3) "A" series boards do not have an RS232 interface or analog multiplexer. Also, they have only one I/O connector (left edge of board) rather than three. If desired, these additional circuits may be wired in the proto areas.
- (4) The red-blue artwork and overlay will not conform to your board.

PARTS LIST-

Board Decoder

- 1 - 430B Board
 - 3 - 7404 (IC-AH, AI, ZZ)
 - 1 - 7410 (IC-T)
 - 1 - 7430 (IC-XX)
 - 1 - 74154 (IC-Y)
 - 2 - 8T26 (IC-G, H)
 - 1 - 1N914 (D3)
 - 1 - 25uf 15V (C-18)
 - 4 - Molex KK-156 Connectors
 - 1 - 3 - Molex KK-156 Connectors (left edge, as desired)
 - 3 - .1uf Bypass Capacitors
- All Resistors 1/4 watt unless specified.

Audio Cassette

- 1 - S1883 UART (IC-S)
- 1 - 7404 (IC-Q)
- 1 - 7474 (IC-W)
- 1 - 7476 (IC-P)
- 1 - 74123 (IC-V)
- 1 - 555 (IC-R)
- 1 - CA3130 (IC-U)
- 1 - 100 (R20)
- 2 - 470 (R9, R10)
- 3 - 1K (R11, R17, R21)
- 1 - 4.7K (R12)
- 4 - 10K (R13, R16, R19, R22)
- 1 - 100K (R15)
- 2 - 10K TRIMPOT (R14, R18)
- 1 - 150pf (C12)
- 1 - 1000pf (C15)
- 3 - .01uf (C6, C8, C11)
- 1 - .01uf MYLAR (C7)
- 1 - .1uf MYLAR (C9)
- 3 - 1N914 (D1, D2, D4)
- 2 - LED (LED1, LED2)
- 3 - .1uf Bypass Capacitors

NOTE: Values given above are for 300 baud. For other rates adjust R12, R13, R14, C7 according to Appendix 1.

RS232

- 1 - S1883 UART (IC-S)
- 1 - 7404 (IC-AA)
- 1 - 555 (IC-R)
- 1 - 470 (R23)
- 1 - 4.7K (R26)
- 3 - 10K (R24, R25, R27)
- 2 - 1N914 (D4), (D5)
- 1 - General Purpose PNP (Q1)
- 1 - General Purpose NPN (Q2)

- 1 - .01uf (C6)
- 2 - .1uf Bypass Capacitors

R12, R13, R14, C7 determine baud rate. Select from Appendix 1 for desired rate.

NOTE: Audio Cassette and RS232 cannot both be implemented.

D/A Converters

- 2 - 7475 (IC-K, L) (IC-M, N)
- 1 - 741 (IC-C) (IC-E)
- 1 - 1408L8 (IC-D) (IC-F)
- 3 - 1K (R3, R4, R5) (R6, R7, R8)
- 1 - 1000pf (C2) (C4)
- 1 - 10pf (C3) (C5)
- 3 - .1uf Bypass Capacitors

NOTE: 430B contains 2 D/A Converters. Quantities shown are for one only. For one, install parts in first parentheses. If both are desired, install parts in second parentheses also. Also, 2-volt reference source must be installed.

2-Volt Reference Source

Install for D/A and/or A/D Converters

- 1 - 100 (R28)
- 1 - 1K (R29)
- 1 - 1N5223 (D6)
- 1 - 2N2270 or equivalent (Q3)
- 3 - .1uf Bypass Capacitors

Unblank One-Shot

- 1 - 74121 (IC-B)
- 1 - 1K (R2)
- 1 - 4.7K (R1)
- 1 - 1000pf (C1)

R1, C1 may be varied to obtain different pulse widths.
See Appendix 1. Values given are 2-3 μ s pulse.

Parallel Output Port

- 2 - 7475 (IC-I, J)
- 1 - .1uf Bypass Capacitor

Parallel Input Port

- 2 - 74125 (IC-AC, AD)

A/D Converters

1 - 7402 (IC-BG)
1 - 74S08 (IC-AB)
1 - 7473 (IC-X)
1 - 74123 (IC-AG)
2 - 74125 (IC-AE, AF)
2 - 74193 (IC-BE, BF)
1 - 741 (IC-BB)
1 - LM311 (IC-BC)
1 - 1408L8 (IC-BD)
1 - 100 (R42)
8 - 1K (R21, R32, R34, R35, R37, R38, R41, R43)
1 - 2.2K (R39)
5 - 4.7K (R31, R33, R40, R44, R45)
1 - 1MEG (R36)
1 - 2K TRIMPOT (R30)
1 - 10pf (C14)
1 - .01uf (C13)
2 - 25uf 15V (C16, C17)
4 - .1uf Bypass Capacitors

The 2-volt reference source must also be installed.

Analog Multiplexer

1 - AM3705 (IC-Z)
1 - 7475 (IC-J)
1 - 1K (R21)

CONSTRUCTION

Construction of the board will be broken down into the major subsystems. Except for the first section, these are independent and may be implemented in any order or combination, except as noted. Refer to the overlay for parts placement.

Board Decoder (Implement for all board configurations)

1. 430B is set for address FBXX, which makes it compatible with OSI software. Normally no jumpers are required, however, for some specialized applications the address may have to be changed. Cut the foil runs going to the leftmost row of pads in the address jumper area, and jumper as desired.
2. Install all ICs under this section of parts list. Install diode D3. Install four bypass capacitors near IC-N, T, AH, ZZ, and capacitor C18. Install four Molex connectors along right edge of board. Refer to pinouts for output Molex connectors (along the left edge of the board) and install as desired.
3. (Testing) Power the board up off-line to verify that there are no power line shorts. Insert the board into the system and, using the monitor, examine locations FB00 and up. FFs should be received. Temporarily ground pin 9 of IC-H. FE's should now be received, indicating board address and data direction circuitry is working.

Audio Cassette Interface

1. Install a 555 at IC-R. Install C6, R12, R13, R14, C7. These parts comprise the UART clock circuit. Install the UART at IC-S. Install bypass capacitors near IC-I and IC-R.

Audio Cassette Interface (continued)

2. (Transmitter) Install 7404 at IC-Q, 7476 at IC-P. Install R9, R11, R15, R16, R17, C8, and LED 1. On systems faster than 1 MHz, install D4.
3. (Testing) Install 430B in the system. Using a scope or frequency meter, verify operation of the clock (clock output - IC-R pin 3). Adjust R14 for frequency of 4800 Hz (for 300 baud). Load the I/O routines described in Appendix 2. Verify transmitter operation by repetitively outputting a character and observing on a scope (IC-P pin 11). Marks should be one-half the clock frequency and spaces should be one-fourth the frequency. The output to the tape recorder should appear to be between a triangle wave and a square wave. The LED should light when transmitting.
4. (Receiver) Install CA3130 at IC-U, 74123 at IC-V, 7474 at IC-W. Install R18, R19, R20, R21, R22, C9, C10, C11, C12, C15, D1, D2, and LED 2. Install bypass capacitors near IC-U and IC-V.
5. (Testing) Load the I/O routines in Appendix 2. Connect the transmitter output (Molex pin C13) to receiver input (pin C16) and, with a scope on IC-W pin 9, adjust R18 halfway between the point where the one-shot retriggers on mark conditions and the point where it retriggers on space conditions.

Audio Cassette Interface (continued)

6. The interface is now ready to record and play back data. Refer to the subroutines in Appendix 2 for this purpose. The user with V-series monitor can now load any OSI programs from Auto-LoadTM Cassette by merely typing "L" on the keyboard.

RS232 Interface

The RS232 interface can be installed instead of the audio cassette, however both cannot be installed together.

1. Install a 555 at IC-R. Install C6, R12, R13, R14, C7. (Values depend on baud rate desired. See Appendix 1.) These parts comprise the UART clock circuit. Install the UART at IC-S. Install bypass capacitors near IC-R and IC-AA.
2. Install a 7404 at IC-AA. Install R23, R24, R25, R26, R27. Install Q1, Q2, D5. On systems faster than 1 MHz, install D4.
3. (Testing) Install the board in the system. Using a scope or frequency meter, verify operation of the clock (clock output-IC-R pin 3). Adjust R14 for a frequency 16 times the desired baud rate. Load the I/O routine (repetitive character) listed in Appendix 2. Verify transmitter operation by outputting a character and observing on a scope (IC-AA pin 8). Load "keyboard echo" program for appropriate processor/monitor combination. Connect RS232 output (C13) to input (C16) and execute the program. If everything is working properly, the user should get a double echo of any character typed.
4. The interface is now ready to be connected to an external RS232 device.

D/A Converters

The construction procedure given is for one D/A. If the user desires both, repeat the procedure substituting the second set of parts on the parts list.

1. (Two volt reference source) Install R28, R29, D6, Q3. Install bypass capacitors near D6 and near R34. Power up the board off-line and verify two-volt output (from collector of Q3).
2. Install a 7475 at IC-K and IC-L. Install 741 or better at IC-C. Install C2, C3, R3, R4, R5. Install a 1408L8 at IC-D. Install bypass capacitors near IC-B and IC-J, and between IC-J and IC-K.
3. (Testing) Install the board in the system. Using the system monitor load location FB01 (FB00 for second D/A) with 00. Use a voltmeter or scope to measure the output voltage (output - Molex connector C2 or C1), which should be near 0 v. Likewise, loading FB01 (FB00) with FF should output about 2 volts. The "sawtooth" program from Appendix 2 will produce a smooth sawtooth waveform at the output of a properly working D/A converter. If any major steps are apparent, check for open or shorted data lines.

Unblank One-Shot

1. Install a 74121 at IC-B. Install R1, R2, C1. Install a bypass capacitor near IC-B.
2. (Testing) Load and execute "unblank" program from Appendix 2. A 2 μ s to 3 μ s long pulse should be observed at C3.

Parallel Output Port

1. Install a 7475 at IC-I and IC-J. Install bypass capacitors to the left of IC-J and near IC-P.

Parallel Output Port (continued)

2. (Testing) Use the system monitor to load FB02 with various values. Verify by comparing to bit values at C5-C12 measured with a scope or voltmeter.

Parallel Input Port

1. Install a 74125 at IC-AC and IC-AD. Install bypass capacitors near D6 and IC-AE.

A/D Converter:

Construction of the A/D converter requires a working D/A converter, a good wideband oscilloscope, and a signal generator.

1. (Two volt reference source) This should have been constructed with the D/A converters.
2. Install 7402, 74S08, 7473, 74123, two 74125s, and two 74193s. Install a 741 at IC-BB and a LM311 at IC-BC. Install R21, R30-R45. Install C13, C14, C16, C17. Install bypass capacitors near IC-U, IC-AF, IC-BF, IC-BD, IC-BC, and two capacitors to the left of IC-BB.
3. (Testing) Install the board in the system without a 1408L8 at IC-BD. Adjust R30 to bring point A on Diagram 3 to the lowest possible positive voltage. Load and execute "A/D Test" program from Appendix 2. Scope the output of the D/A converter at FB01 (C2) and apply a slowly varying bi-polar voltage in the range ± 1 volt to the input of the A/D converter (C36). You should observe a sawtooth waveform which changes from positive going to negative going as the input to the A/D converter changes polarity. The ramp should be smooth with no large steps. If the ramp is not smooth and straight, a data line from the counters

A/D Converter (continued)

may be shorted. If the sawtooth doesn't change direction, check the op amp, comparitor, and count up/down logic for the proper operation.

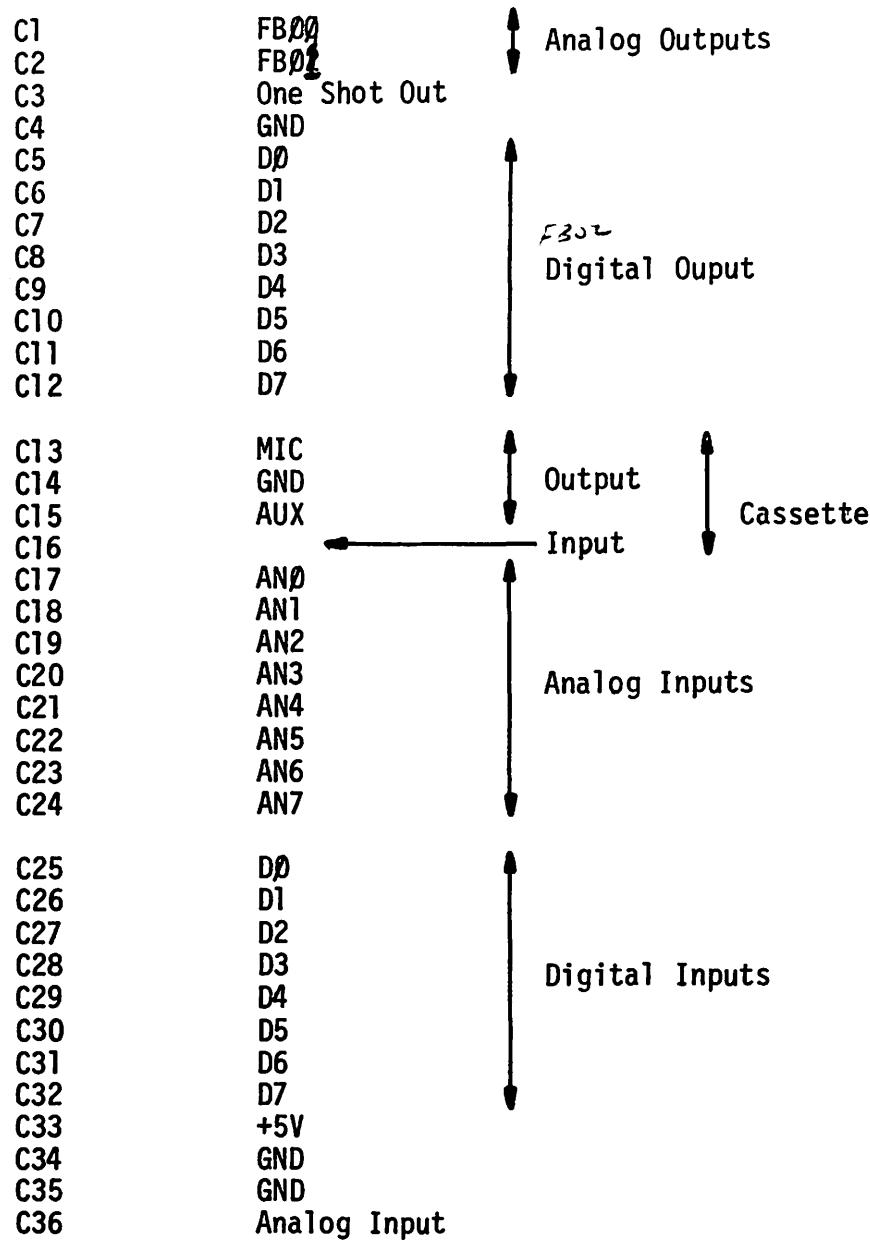
4. Remove the board from the system and install a 1408L8 at IC-BD.
5. (Testing) Reinstall the board and load and execute "A/D Test". With a 0 volt input, adjust R30 for mid-range output on the D/A converter (about 80₁₆). Apply a low amplitude 1 KHz sine wave to the A/D converter input (C36). The sine wave should be observed at the D/A output. Increase the amplitude until A/D converter breaks out of track on either the positive or negative peak of the waveform. Adjust R30 to eliminate breakout and increase the amplitude a little bit more. Repeat until the breakout is symmetric.
6. If there is noise on the A/D converter, R36 may have to be adjusted. Lowering the value will decrease the sensitivity to noise, but will slow the comparitor causing the converter to oscillate several least significant bits.

Analog Multiplexer

If the analog multiplexer is installed, do not use the analog input at C36. Do not implement this circuit until the A/D portion is operational.

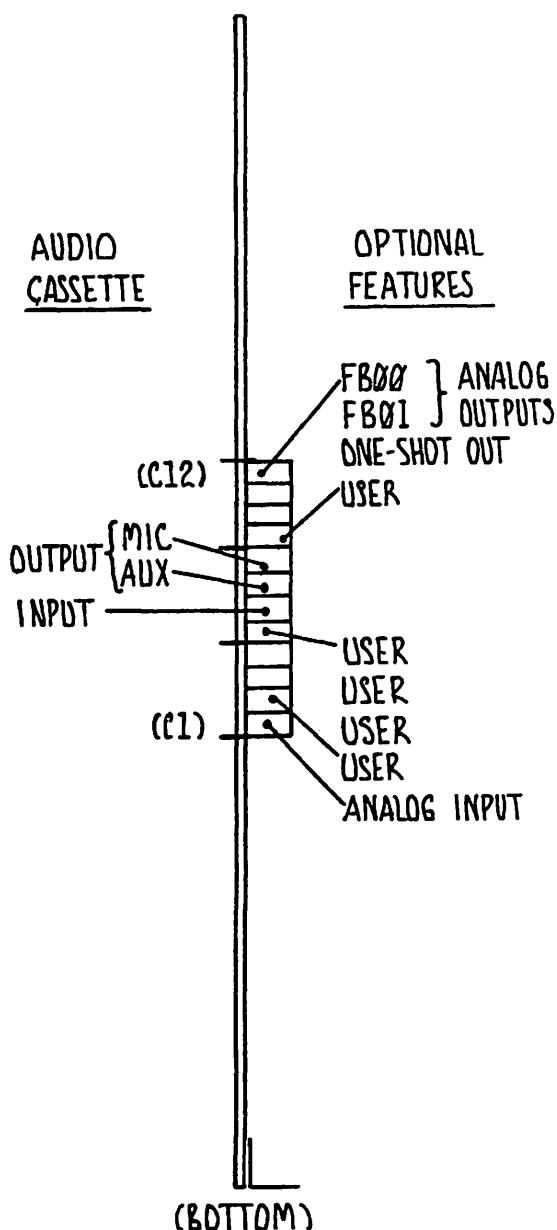
1. Install a 7475 at IC-J and an AM3705 at IC-Z. Install R21.
2. Refer to Theory of Operation for instructions on use.

430B Connector Pinout

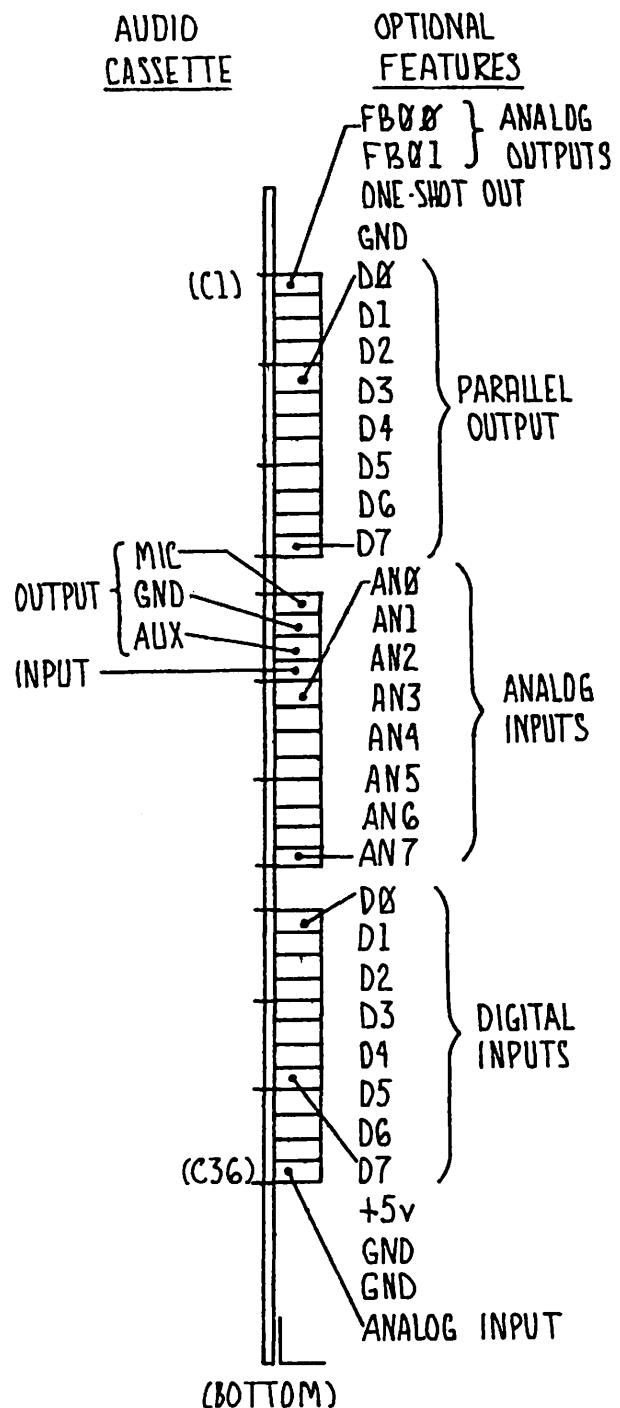


430 BOARD CONNECTIONS FOR AUDIO CASSETTE
AND OPTIONAL A/D AND D/A CONVERTERS

430 A



430 B



Appendix 1

This appendix contains pinouts for all IC used on the 430B. It also contains data on adjusting the baud rate on the serial interface.

1.1 IC Data Sheets

The following pages list all ICs used on the 430B. This includes timing data on both one-shots and on the 555 timer.

1.2 Baud Rate Adjustments

The table lists values of R12-R14, C7 for common baud rates.

Baud Rate	Freq (16X)	C7	R12/R14	R13
110	1760	.01uf	20K/5K	30K
300	4800	.01uf	4.7K/5K	10K
600	9600	.01uf	2.2K/5K	5.6K
1200	19200	1000pf	25K/5K	20K
2400	B8400	1000pf	7.5K/5K	13K
4800	76800	1000pf	2.2K/5K	6.8K
9600	153600	1000pf	100/5K	3.6K

1.3 Unused Gates

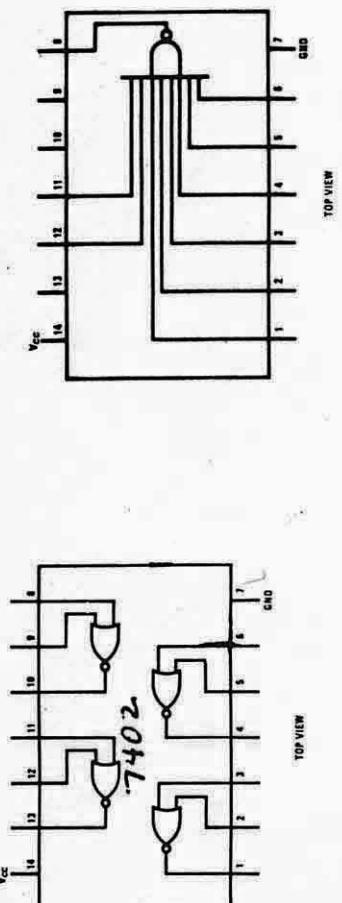
The following IC's contain unused gates. These may be used for user modifications.

2-7402	IC-BG
1-7404	IC-AA (only if RS232 is installed)
1-7410	IC-T
1-74123	IC-V

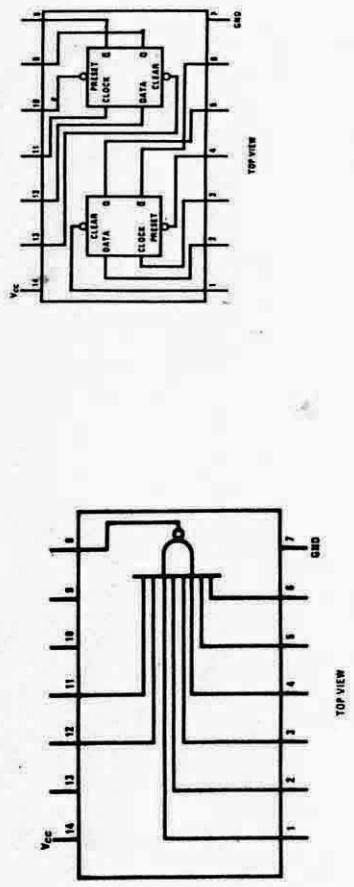
The following outputs are available from the 74154, and may be used as strobe lines:

PIN	ADDRESS
4	(W)FB03
7	(W)FB06
11	(R)FB02
14	(R)FB04
17	(R)FB07

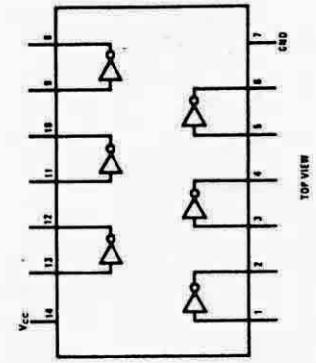
DM5430/DM7430
Dual-In-Line Package



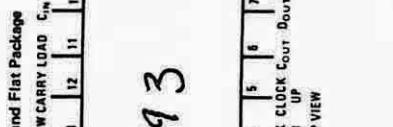
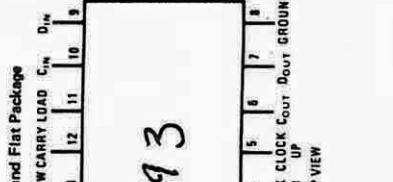
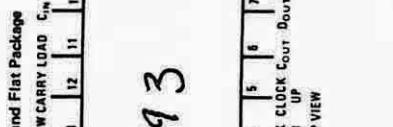
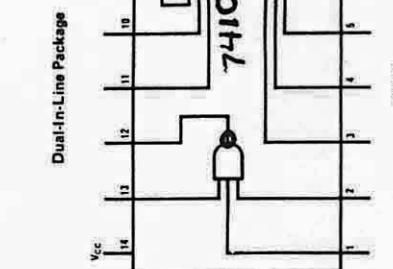
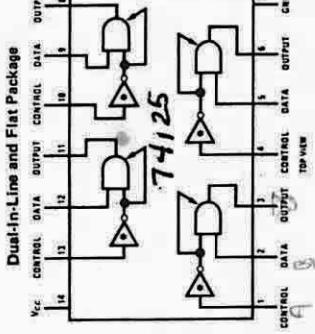
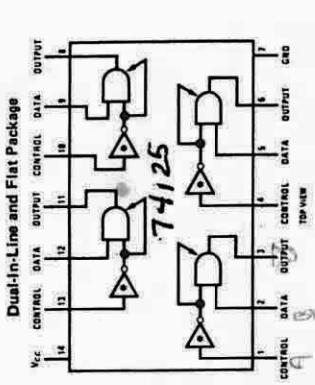
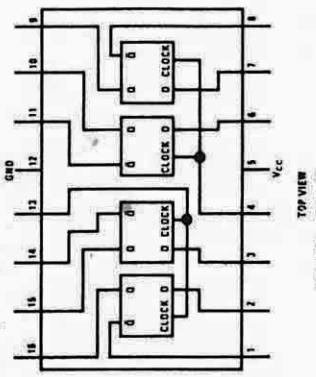
DM5474/DM7474
Dual-In-Line Package



DM5404/DM7404
Dual-In-Line Package

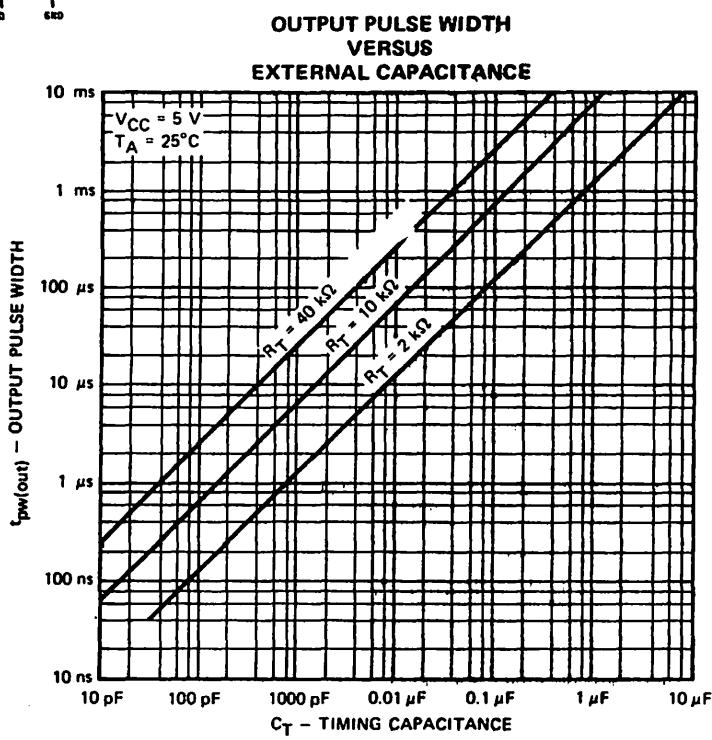
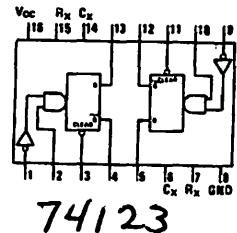
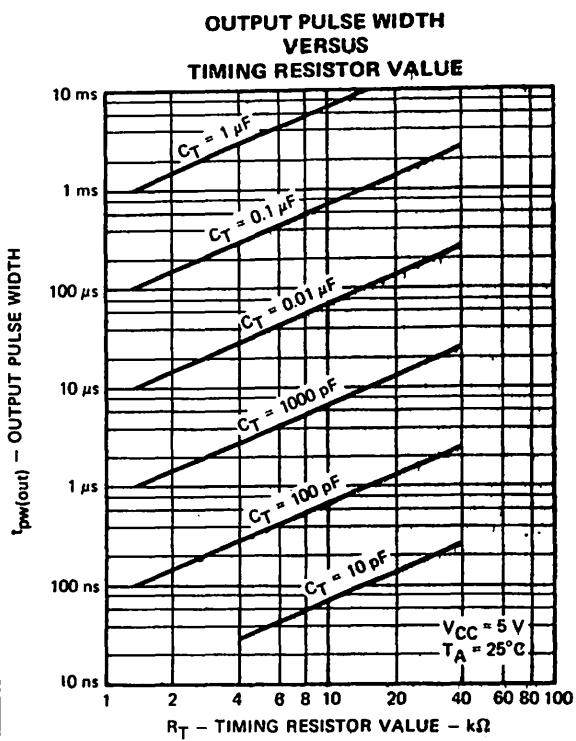
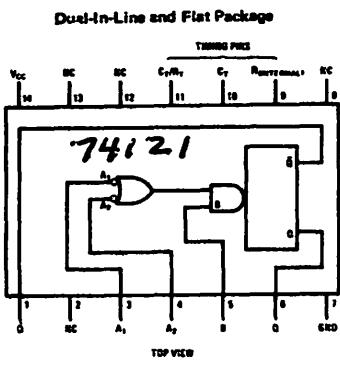


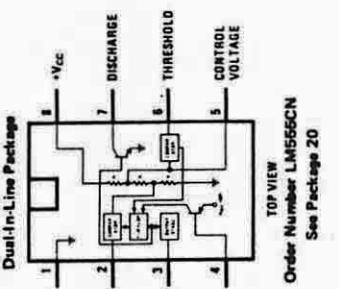
logic and connection diagram
Dual-In-Line and Flat Package



DM5473/DM7473

DM5476/DM7476





The charge time (output high) is given by:
 $t_1 = 0.693 (R_A + R_B) C$

And the discharge time (output low) by:
 $t_2 = 0.693 (R_B) C$

Thus the total period is:
 $T = t_1 + t_2 = 0.693 (R_A + 2R_B) C$

The frequency of oscillation is:

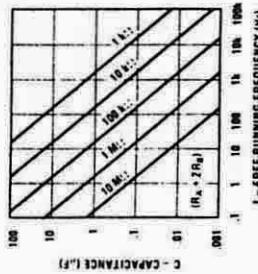
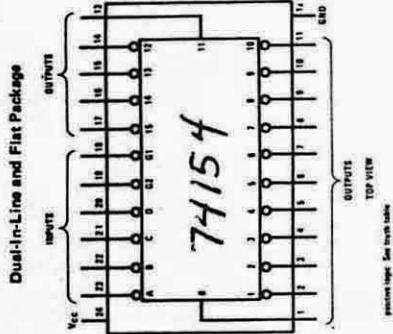
$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B) C}$$


FIGURE 6. Free Running Frequency

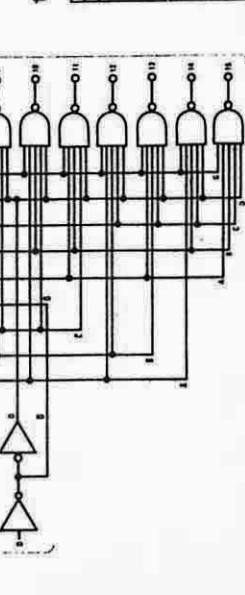
Figure 6 may be used for quick determination of these RC values.

$$\text{The duty cycle is: } D = \frac{R_B}{R_A + 2R_B}$$

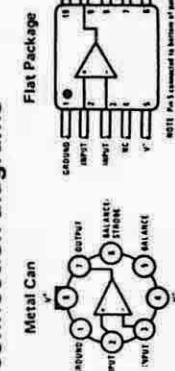


truth table

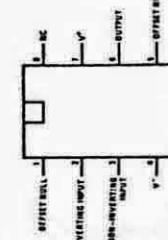
		GND																	
		Q11	Q12	Q13	Q14	Q15	Q16	Q17	Q18	Q19	Q20	Q21	Q22	Q23	Q24	Q25	Q26	Q27	Q28
INPUT	GND	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Q11	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Q12	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Q13	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Q14	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Q15	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Q16	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Q17	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Q18	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Q19	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Q20	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Q21	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Q22	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Q23	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Q24	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Q25	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Q26	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Q27	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Q28	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1



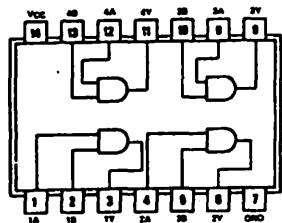
connection diagrams *



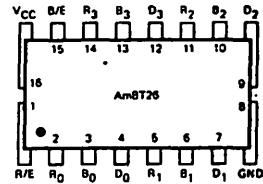
*Pin connections shown on schematic diagram and typical applications are for TO-5 package.



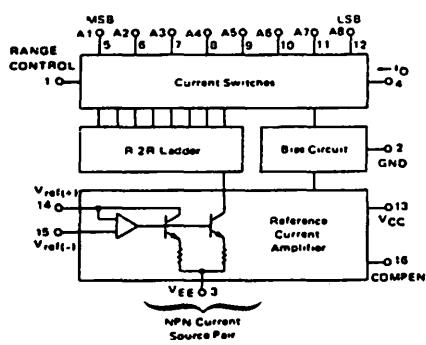
Order Number LM741CN



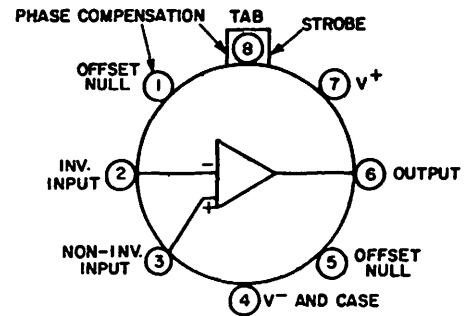
74S08



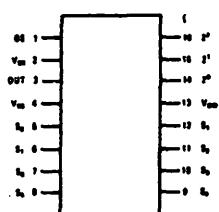
8T26



1408L8
D/A CONVERTER



CA3130



AM3705 - ANALOG MULTIPLEXER

truth table

LOGIC INPUTS				CHANNEL
Z^*	Z^*	Z^*	OE	ON
L	L	L	H	S ₁
H	L	L	H	S ₂
L	H	L	H	S ₃
H	L	H	H	S ₄
L	H	H	H	S ₅
H	H	H	H	S ₆
X	X	X	L	OFF

Appendix 2: I/O Utilities

This appendix describes utilities useful in testing the various 430B subsystems. Some of these are listed in machine code for both 6502 and 6800 processors; a few depend on the processor/monitor configuration of the particular machine and so are described in general terms. The user can easily code these for his own system configuration.

2.1 UART I/O Utilities

The following two pages list UART utility subroutines for 6502 and 6800. Several useful programs for testing and adjusting the audio cassette interface are described below.

Repetitive Character Output:

This is useful in determining if the UART transmitter and receiver are operating and in aligning the UART clock and receiver pot R18. The steps are as follows:

- (1) Jump to UART initialization subroutine.
- (2) Load accumulator with some fixed character.
- (3) Jump to UART output subroutine.
- (4) Branch to Step (3).

Keyboard Echo

This program will read the keyboard and double echo it if the audio cassette interface is operating properly.

- (1) Jump to keyboard input subroutine.
- * (2) Output character to teletype/TV.
- (3) Jump to UART output subroutine.
- (4) Jump to UART input subroutine.
- (5) Output character to teletype/TV.
- (6) Branch to Step (1).

Keyboard input routines are present in the monitor. Use step 2 only for V-series monitors, which do not automatically echo an input character.

2.2 D/A and A/D Routines

Sawtooth Generator

This program is useful in testing the D/A converters. It should produce a smooth ramp. Any gaps or jumps indicate shorted or broken data lines.

- (1) Load accumulator with zero.
- (2) Store accumulator in D/A converter.
- (3) Increment accumulator
- (4) Branch to Step (2).

This routine will also fire the unblank one-shot when the D/A converter at FB01 is used.

A/D Test Routine:

These routines read a waveform at the A/D input and echo it to the D/A converter at FB01. For 6800:

Start	Location	Code	Comment
	0000	B6	LDA
	01	FB	A/D Address
	02	00	
	03	B7	STAA
	04	FB	
	05	01	D/A Address
	06	7E	Jump to start
	07	00	
	08	00	

For 650X:

Start	Location	AD	LDA
	0000	00	A/D Address
	01	FB	
	02	8D	STA
	03	01	D/A Address
	04	FB	
	05	4C	Jump to start
	06	00	
	07	00	
	08	00	

Program UART ROUTINES Starting Address — Page —

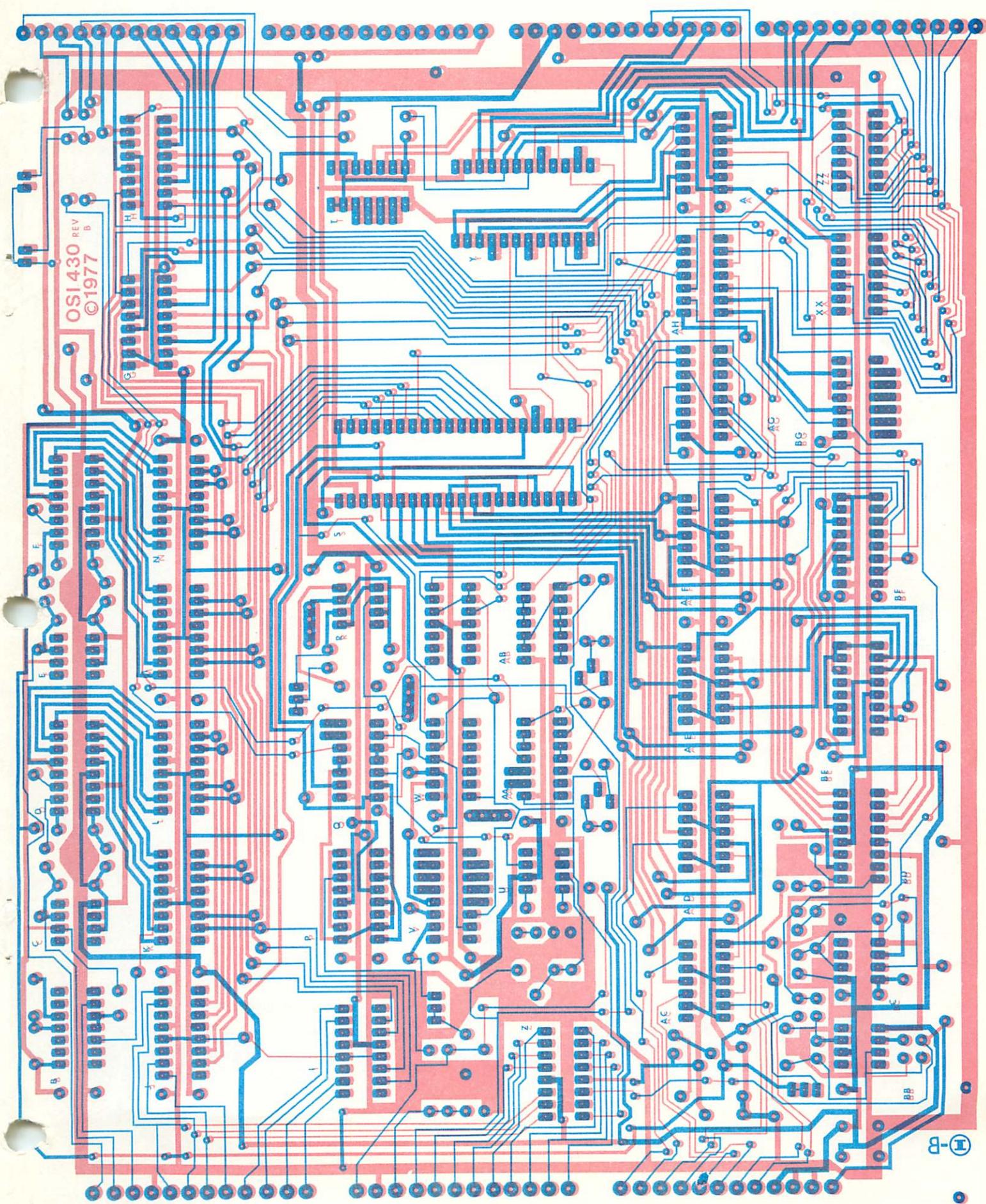
Program Number _____ Programmer _____ Date _____

Location	Op Code	Label	Instruction	Comments
FOR	650X			
		INITIALIZATION ROUTINE		
AD	INT	LDA		
0G				RESET LOCATION
FR				
AG		LDA		
FF				UART STATUS CODE
8D		STA		
05				STATUS WORD LOCATION
FB				
60		RTS		RETURN
INPUT A Character to Accumulator				
AD	INCH	LDA		
05				STATUS REG.
FB				
HA		LSR		Inc. Shift Right (ODA to CHREG)
90		BCC		
FA	(b)	INCH		RAM array } wait for data. → INCH }
AD		LDA		
03				DATA WORD
FB				[FB03]
8D		STA		
07				
FB				
60		RTS		RESET ODA
OUTPUT A character from Accumulator				
4B	OUTCH	PHA		Push Acc.
AD	WAIT	LDA		
05				STATUS REG.
FB				
10		BPL		if NEB > 7BMT :: all through
FB		Wait		
68		PLA		
8D		STA		Pop Acc.
04				OUTPUT Word
FB				
60		RTS		RETURN

Program UART ROUTINES Starting Address _____ Page _____

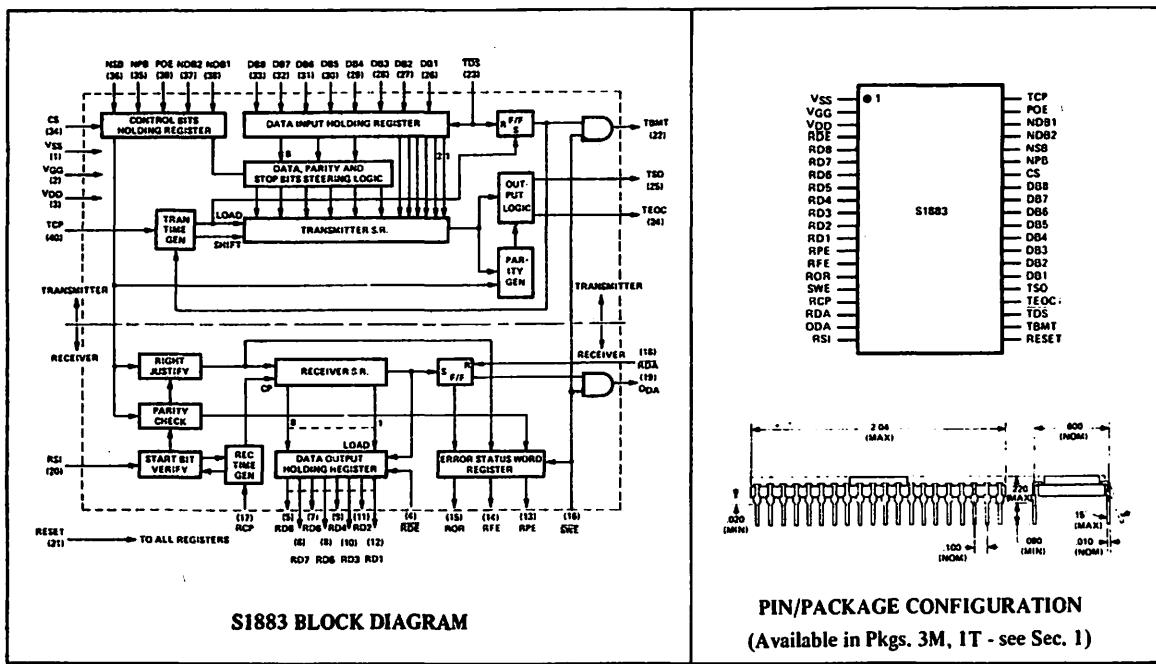
Program Number _____ Programmer _____ Date _____

Location	Op Code	Label	Instruction	Comments
FOR 6800				
INITIALIZATION		ROUTINE		
B6	INT	LDAA		
FB				RESET LOCATION
06				
86		LDAA		
FF				UART STATUS CODE
37		STAA		
FB				STATUS WORD LOCATION
05				
39		RTS		RETURN
INPUT A Character		to Accumulator A		
B6	INCH	LDAA		
FB				STATUS REG.
05				
44		LSRA		
24		BCC		
FA		INCH		
B6		LDAA		
FB				DATA WORD
03				
B7		STAA		
FB				RESET ODA
07				
39		RTS		RETURN
Output A Character from Accumulator -				
36	OUTCH	PSHA		
B6	WAIT	LDAA		
FB				STATUS REG.
05				
9A		BPL		
FB		WAIT		
32		PULA		
B7		STAA		
FB				OUTPUT WORD
04				
39		RTS		RETURN



S1883

UART



FEATURES

- 12.5 Baud Data Rates
- 5-8 Bit Word Length
- Parity Generation/Checking Odd, Even, None
- Framing and Overflow Error Detection
- 1, 1.5, or 2 Stop Bits
- Double Buffered Input/Output
- Independent Transmit/Receive Rates
- Start and Stop Bits Generated and Detected
- Interchangeable with TMS6011, COM2017, TR1602, AY-5-1013
- Tri-State Outputs

FUNCTIONAL DESCRIPTION

The S1883 Universal Asynchronous Receiver Transmitter (UART) is a single chip MOS/LSI device that totally replaces the asynchronous parallel to serial and serial to parallel conversion logic required to interface a word parallel controller or data terminal to a bit serial communication network.

For asynchronous data transmission with a non-contiguous data bit stream, the UART automatically inserts a START bit

preceding each character and under program control 1, 1.5, or 2 stop bits at the end of each character. To detect incoming characters in a noisy environment the UART employs a START bit detection network and allows errorless recovery of data with up to 42% distortion.

The UART will transmit or receive data characters of 5, 6, 7, or 8 bit length. Options allow the generation and checking of odd, even parity or no parity. The odd or even parity bit is automatically added to the character length for transmission.

S1883 UART

The parity bit is removed, checked and an error flag set if incorrectly received.

The data or baud rate at the receiver input and transmitter output are determined independently by external clock inputs. The clock inputs must be 16 times the data rate required at the serial input and output. The independent clocks allow for either half or full duplex operation.

The UART provides a buffer register in both the transmitter and receiver to allow a full character time for responding to a received data ready or transmit data request signal. The UART generates a MARK signal if the transmit register is not loaded with a data character and also indicates an overflow error if two characters are received without a RDA input.

TYPICAL APPLICATIONS

- Computer Peripherals
- Communication Concentrators
- Integrated Modems
- Industrial Data Transmission
- TTY Terminals
- Time Division Multiplexing

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	-65°C to +150°C
Positive Voltage on Any Pin with Respect to V _{SS}+3 Volt
Negative Voltage on Any Pin with Respect to V _{SS}	-20.0 Volt

NOTE: Stresses greater than those listed as Maximum Ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operation section of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC (STATIC) CHARACTERISTICS

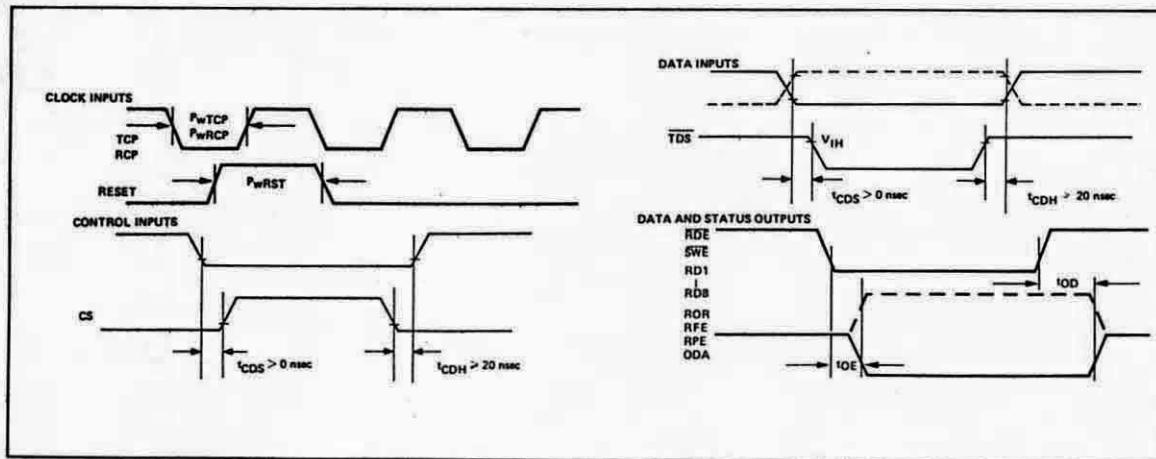
T_A = 0° - +70°C, V_{SS} = +5 Volt ±5%, V_{GG} = -12 Volt ±5%

Symbol	Parameter	Min	Max	Unit	Condition
V _{IH}	Input High Voltage	V _{SS} -1.0	V _{SS} +0.3	Volt	Internal Pull-up Resistor Provided
V _{IL}	Input Low Voltage	V _{GG}	0.8	Volt	
I _{LI}	Input Load Current		-1.2	mamp	V _{IN} = 0 Volt
V _{OH}	Output High Voltage	2.4		Volt	I _{OH} = -100 uamp
V _{OL}	Output Low Voltage		.4	Volt	I _{OL} = 1.6 mamp
C _{IN}	Input Capacitance		20	pf	V _{IN} = V _{SS}
C _{OUT}	Output Capacitance		10	pf	V _{OUT} = V _{SS}
I _{SS}	V _{SS} Supply Current		30	mamp	SWE = RDE = V _{IL}
I _{GG}	V _{GG} Supply Current		40	mamp	ITTL Load

AC (DYNAMIC) CHARACTERISTICS
 $T_A = 0^\circ\text{C} - +70^\circ\text{C}$; $V_{SS} = +5 \text{ Volt} \pm 5\%$; $V_{GG} = -12 \text{ Volt} \pm 5\%$

Symbol	Parameter	Min	Max	Unit	Condition
TCP, RCP	Clock Frequency	DC	200	KHz	
Input Pulse Widths					
PWTCP	Transmit Clock	2.5		usec	$C_L = 20\text{pf}$
PWRCP	Receive Clock	2.5		usec	1 TTL Load
PWCS	Control Strobe	250		nsec	
PWTDS	Transmit Data Strobe	250		nsec	
PWRST	RESET	1.0		μsec	
PWSWE	Status Word Enable	500		nsec	
PWRDA	Reset Data Available	500		nsec	
PWRDE	Receive Data Enable	250		nsec	
Switching Characteristics					
t _{CDS}	Control Set Up Time	0		nsec	Figure 1
t _{CDH}	Control Hold Time	20		nsec	Figure 1
t _{OE}	Output Enable Time		500	nsec	
t _{OD}	Output Disable Time		500	nsec	

TIMING WAVE FORMS (Figure 1)



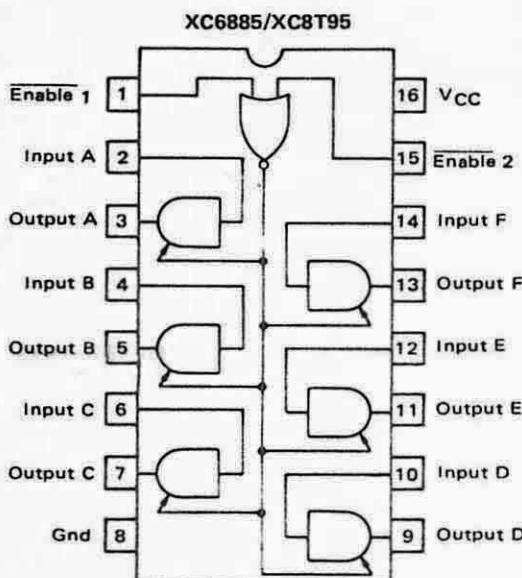
(31)	DB6	transmitted following the START bit. For data words less than eight bits, the unused bits are don't care inputs.
(32)	DB7	
(33)	DB8	
(23)	TDS	TRANSMITTER DATA STROBE. A V _I L enters data on the DB1-DB8 inputs into the INPUT HOLDING REGISTER. If the transmitter is in the idle state with both TBMT and TEOC at V _O H, the START bit will be generated on the first negative transition of the input clock TCP following the return of TDS to a V _I H state.
(25)	TSO	TRANSMITTER SERIAL OUTPUT. Data entered on DB1-DB8 are serially transmitted on TSO. A START (SPACE) bit precedes each character. A PARITY bit, if selected, and the correct number of STOP bits follow the last valid data bit. The TSO output is V _O H (MARK) when a valid character is not being transmitted.
(22)	TBMT	TRANSMITTER BUFFER EMPTY. A V _O H indicates the character in the INPUT HOLDING REGISTER has been transferred into the transmitter and a new character may be loaded into the INPUT HOLDING REGISTER. One complete character time (START BIT, DATA BITS, PARITY BIT, AND STOP BIT(S)) is available to load the next character. If a TDS is not generated within the time allotted, the TSO output will go into an idle state of V _O H or a MARK condition. TBMT will remain in the tri state mode unless SW _E is a UZL.
(24)	TEOC	TRANSMITTER END OF CHARACTER. A V _O L to V _O H transition indicates the transmission of the character and stop bits have been completed. The V _O H is maintained until the leading edge of the next START bit (MARK to SPACE transition) is generated.
(40)	TCP	TRANSMITTER CLOCK PULSE. The transmitter input clock must be 16 times faster than the desired baud rate at TSO.
(17)	RCP	RECEIVER CLOCK PULSE. The receiver input clock must be 16 times the baud rate of data received on RSI.
(20)	RSI	RECEIVER SERIAL INPUT. Serial input data is received on RSI at a baud rate 1/16th the rate of RCP. The V _I H to V _I L (MARK to SPACE) transition beginning each START bit synchronizes the receiver to the incoming data. Data is assumed to be received least significant bit first.
(12)	RD1	RECEIVER DATA. Data outputs from the DATA OUTPUT HOLDING REGISTER are active only when RD _E is a V _I L. The eight data outputs are in a tri-state mode if RD _E is a V _I H. Data is presented at the outputs right justified with RD1 the least significant bit. For data word lengths less than 8 bits the unused bits will appear as V _O L.
(11)	RD2	
(10)	RD3	
(9)	RD4	
(8)	RD5	
(7)	RD6	
(6)	RD7	
(5)	RD8	
(4)	RD _E	RECEIVER DATA ENABLE. A V _I L enables data in the DATA OUTPUT HOLDING REGISTER to the RECEIVER DATA output pins. For an output configuration not requiring a tri-state condition for RD1-RD8 the RD _E input can be tied directly to ground enabling the data outputs at all times.
(19)	ODA	OUTPUT DATA AVAILABLE. A V _O H indicates a complete character has been received and transferred to the DATA OUTPUT HOLDING REGISTER. The ODA output will be in the tri-state mode unless SW _E is a V _I L.

S1883
UART

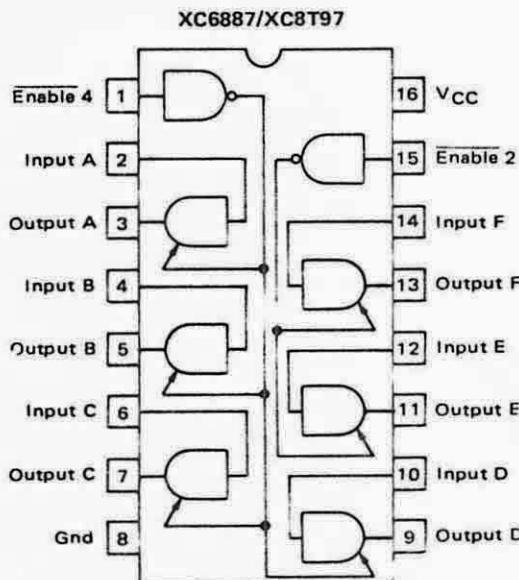
PIN DEFINITIONS

Pin	Label	Function			
(1)	V _{SS}	+5 Volt ± 5%			
(2)	V _{GG}	-12 Volt ± 5%			
(3)	V _{DD}	Ground			
(21)	RESET	A V _{IH} resets all internal registers and counters. The transmitter status outputs TBMT and TEOC are set to V _{OH} indicating the input transmitter buffer register is empty. The TSO output generates V _{OH} or MARK until a valid data character has been loaded into the transmitter and valid data transmission begins. The receiver status output ODA, is reset to the V _{OL} state.			
(38)	NDB1	Number Data Bits/Character			
(37)	NDB2	Number Data Bits/Character			
(36)	NSB	Number Stop Bits			
		The bit length of each data character and the number of stop bits added to each transmitted character are defined by these three inputs.			
		The character word length does not include the parity bit and is common to both the transmitter and receiver if operating in the full duplex mode.			
NSB	NDB2	NDB1	BITS/CHARACTER	STOP BITS	
V _{IL}	V _{IL}	V _{IL}	5	1	
V _{IL}	V _{IL}	V _{IH}	6	1	
V _{IL}	V _{IH}	V _{IL}	7	1	
V _{IL}	V _{IH}	V _{IH}	8	1	
V _{IH}	V _{IL}	V _{IL}	5	1.5	
V _{IH}	V _{IL}	V _{IH}	6	2	
V _{IH}	V _{IH}	V _{IL}	7	2	
V _{IH}	V _{IH}	V _{IH}	8	2	
(35)	NPB	NO PARITY BIT. A V _{IH} eliminates the PARITY bit from being transmitted causing the STOP bit(s) to immediately follow the last data bit. The receiver assumes the bit(s) following the last data bit to be STOP bits. The RPE output is also forced to a V _{OL} condition.			
(39)	POE	PARITY ODD/EVEN. If the NPB input is V _{IL} , the parity mode is ODD if POE is V _{IL} and EVEN if POE is V _{IH} .			
		The parity mode is the same for both the transmitter and receiver.			
(34)	CS	CONTROL STROBE. A V _{IH} loads POE, NDB1, NDB2, NPB, NSB into the CONTROL HOLDING REGISTER.			
		To load the control inputs for static operation CS can be hard-wired to V _{IH} .			
(26)	DB1	TRANSMITTER DATA BITS. Input data on DB1-DB8 are strobed into the DATA INPUT HOLDING REGISTER by TDS.			
(27)	DB2				
(28)	DB3	Input data is assumed right justified so DB1 is always the least significant bit and is the bit			
(29)	DB4				
(30)	DB5				

BUFFERS/DRIVERS



Enable 2	Enable 1	Input	Output
L	L	L	L
L	L	H	H
L	H	X	O
H	L	X	O
H	H	X	O



Enable	Input	Output
L	L	L
L	H	H
H	X	O

L = Low Logic State
H = High Logic State
O = high Impedance State
X = irrelevant

PIN CONNECTIONS – MC6880 MC8T26

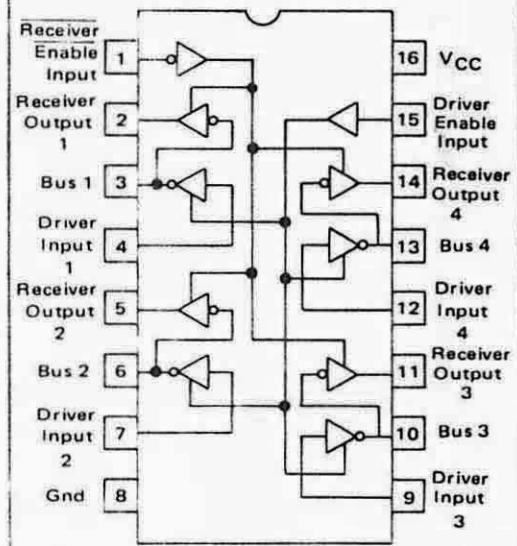


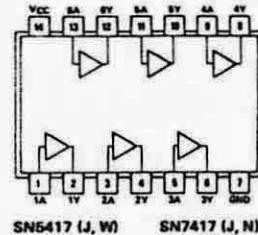
TABLE 1

B/E	I/E	OPERATION
0	0	Driver Disabled, Receiver Enabled
0	1	Driver Disabled, Receiver Disabled
1	0	Driver Enabled, Receiver Enabled
1	1	Driver Enabled, Receiver Disabled

HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

17

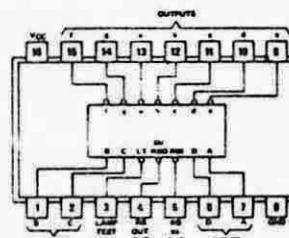
positive logic:
Y = A



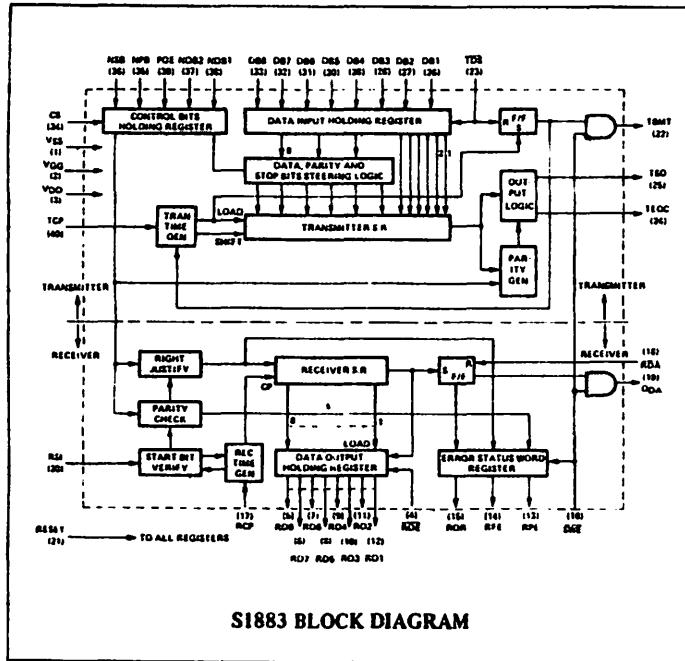
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

46 ACTIVE-LOW, OPEN-COLLECTOR, 30-V OUTPUTS

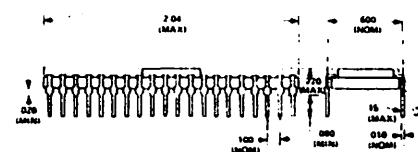
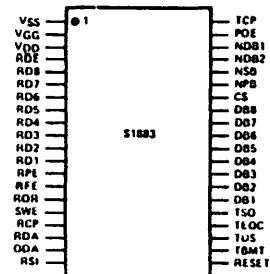
47 ACTIVE-LOW, OPEN-COLLECTOR, 15-V OUTPUTS



SN5446A (J, W)	SN7446A (J, N)
SN54L46 (J)	SN74L46 (J, N)
SN5447A (J, W)	SN7447A (J, N)
SN54L47 (J)	SN74L47 (J, N)
SN54LS47 (J, W)	SN74LS47 (J, N)



S1883 BLOCK DIAGRAM

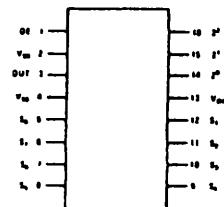


PIN/PACKAGE CONFIGURATION
(Available in Pkgs. 3M, 1T - see Sec. 1)

1	O	CA1	40
2	PA0	CA2	39
3	PA1	IRQA	38
4	PA2	IRQB	37
5	PA3	RS0	36
6	PA4	RS1	35
7	PA5	Reset	34
8	PA6	D0	33
9	PA7	D1	32
10	PB0	D2	31
11	PB1	D3	30
12	PB2	D4	29
13	PB3	D5	28
14	PB4	D6	27
15	PB5	D7	26
16	PB6	E	25
17	PB7	CS1	24
18	CB1	CS2	23
19	CB2	CS0	22
20	VCC	R/W	21

1	•	V _{SS}	CTS	24
2		Rx Data	DCD	23
3		Rx Clk	D0	22
4		Tx Clk	D1	21
5		RTS	D2	20
6		Tx Data	D3	19
7		iRO	D4	18
8		CS0	D5	17
9		CS2	D6	16
10		CS1	D7	15
11		RS	E	14
12		V _{DD}	R/W	13

MC68850

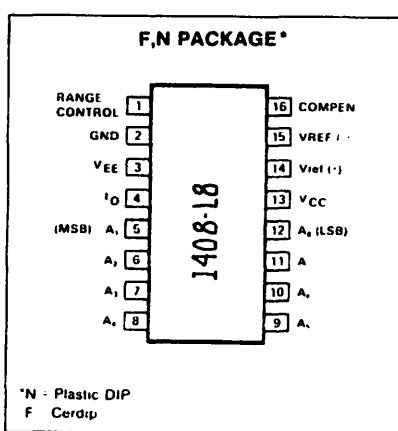


Order Number
AM3705 or AM3705CD
See Package 2
AM3705F or AM3705CF
See Package 5

truth table

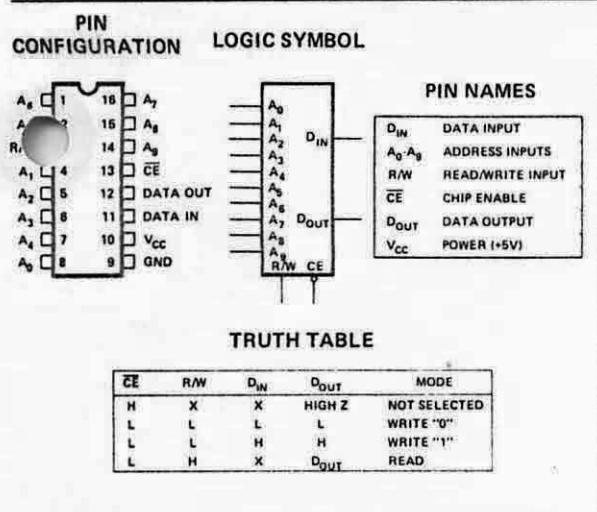
LOGIC INPUTS		CHANNEL		
I [#]	I ¹	I ²	OE	ON
L	L	L	H	S ₁
H	L	L	H	S ₂
L	H	L	H	S ₃
H	H	L	H	S ₄
L	L	H	H	S ₅
H	H	H	H	S ₆
L	H	H	H	S ₇
H	L	H	H	S ₈
X	X	X	L	OFF

**AM3705 - 8 CHANNEL
ANALOG MULTIPLEXER**



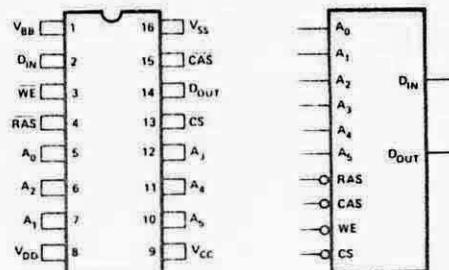
*N = Plastic DIP
F = Cerdip

I/O DEVICES / LINEAR



2102A

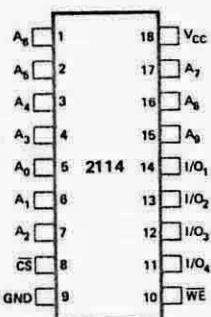
PIN CONFIGURATION LOGIC DIAGRAM



PIN NAMES

A ₀ -A ₉	ADDRESS INPUTS	WE	WRITE ENABLE
CAS	COLUMN ADDRESS STROBE	V _{BB}	POWER (-5V)
CS	CHIP SELECT	V _{CC}	POWER (+5V)
D _{IN}	DATA IN	V _{DD}	POWER (+12V)
D _{OUT}	DATA OUT	V _{SS}	GROUND
RAS	ROW ADDRESS STROBE		

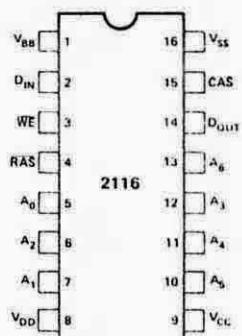
2104



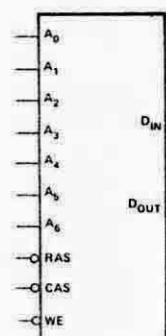
PIN NAMES

A ₀ -A ₉	ADDRESS INPUTS	V _{CC}	POWER (+5V)
WE	WRITE ENABLE	GND	GROUND
CS	CHIP SELECT		
I/O ₁ -I/O ₄	DATA INPUT/OUTPUT		

PIN CONFIGURATION



LOGIC SYMBOL



PIN NAMES

A ₀ -A ₆	ADDRESS INPUTS	WE	WRITE ENABLE
CAS	COLUMN ADDRESS STROBE	V _{BB}	POWER (-5V)
D _{IN}	DATA IN	V _{CC}	POWER (+5V)
D _{OUT}	DATA OUT	V _{DD}	POWER (+12V)
RAS	ROW ADDRESS STROBE	V _{SS}	GROUND

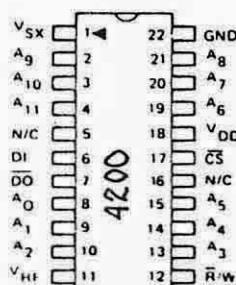
22 PIN DUAL IN-LINE

1	Gnd	O	V _{CC}	24
2	D ₀	A ₀	23	
3	D ₁	A ₁	22	
4	D ₂	A ₂	21	
5	D ₃	A ₃	20	
6	D ₄	A ₄	19	
7	D ₅	A ₅	18	
8	D ₆	A ₆	17	
9	D ₇	R/W	16	
10	CS0	CS5	15	
11	CS1	CS4	14	
12	CS2	CS3	13	

MCG810

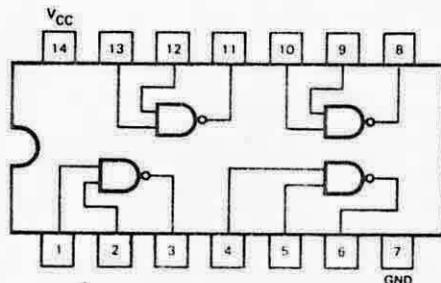
RAM

TOP VIEW



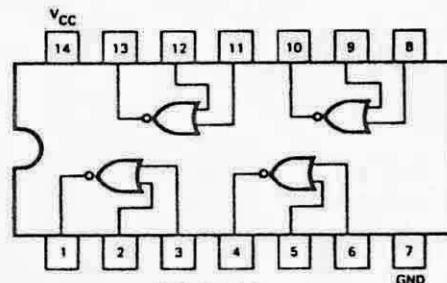
PIN ASSIGNMENT

QUAD 2-INPUT NAND GATE



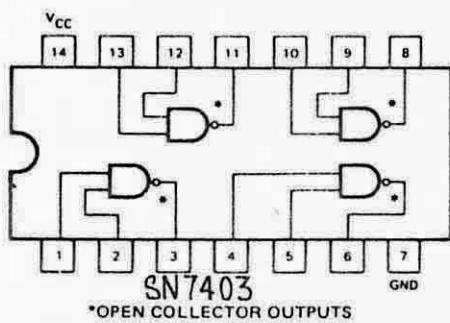
SN7400

QUAD 2-INPUT NOR GATE



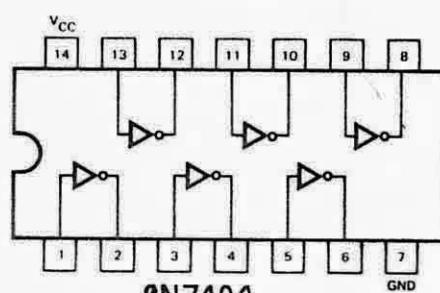
SN7402

QUAD 2-INPUT NAND GATE



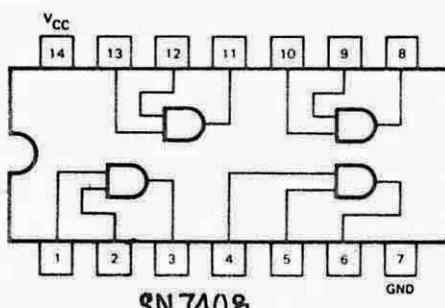
SN7403

HEX INVERTER



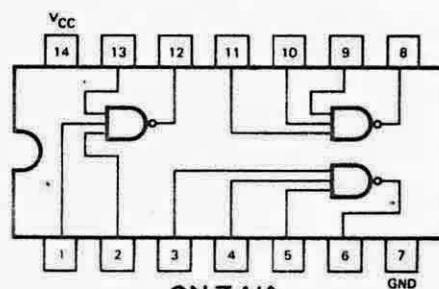
SN7404

QUAD 2-INPUT AND GATE



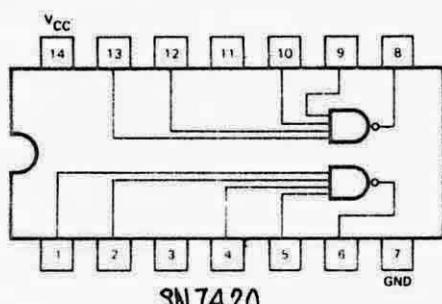
SN7408

TRIPLE 3-INPUT NAND GATE



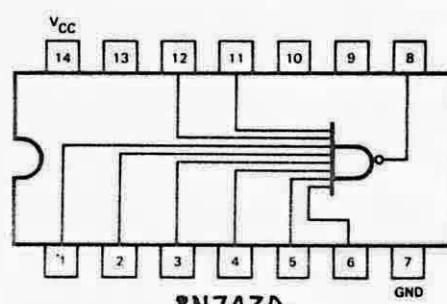
SN7410

DUAL 4-INPUT NAND GATE



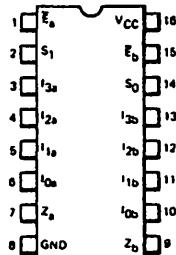
SN7420

8-INPUT NAND GATE



SN7430

TTL



SN74153

TRUTH TABLE								
SELECT INPUTS		INPUTS (a or b)					OUTPUT	
S ₀	S ₁	\bar{E}	I ₀	I ₁	I ₂	I ₃	Z	
X	X	H	X	X	X	X		L
L	L	L	L	X	X	X		L
L	L	L	H	X	X	X		H
H	L	L	X	L	X	X		L
H	L	L	X	H	X	X		H
L	H	L	X	X	L	X		L
L	H	L	X	X	H	X		H
H	H	L	X	X	X	L		L
H	H	L	X	X	X	H		H

H = HIGH Voltage Level

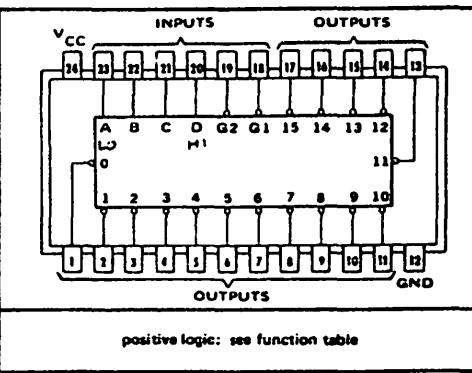
L = Low Voltage Level

- Don't Care

FUNCTION TABLE

level, L = low level, X = irrelevant

**SN54154...J OR W PACKAGE
SN54L154...J PACKAGE
74154, SN74L154...J OR N PACKAGE
(TOP VIEW)**



SN 74154

TRUTH TABLE

1	E _S	V _{CC}	16
2	E _b	E _b	15
3	A ₁	E _b	14
4	Ø _{2a}	A ₀	13
5	Ø _{2b}	Ø _{2b}	12
6	Ø _{1a}	Ø _{2b}	11
7	Ø _{1b}	Ø _{1b}	10
8	GND	Ø _{0b}	9

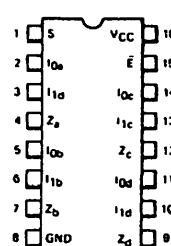
ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A ₀	A ₁	E _a	\bar{E}_a	\bar{O}_0	\bar{O}_1	\bar{O}_2	\bar{O}_3	\bar{E}_b	\bar{E}_b	\bar{O}_0	\bar{O}_1	\bar{O}_2	\bar{O}_3
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

SN74155

H ■ HIGH Voltage Level

L = Low Voltage Level

X = Don't Care



SN 74157

TRUTH TABLE				
ENABLE	SELECT INPUT	INPUTS		OUTPUT
\bar{E}	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

MODE SELECT TABLE

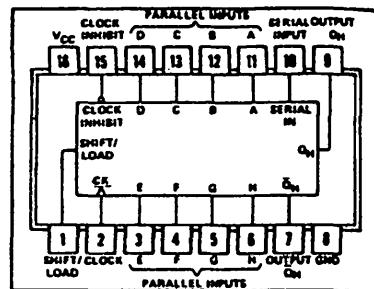
	\bar{MR}	V_{CC}	16	*SR	PE	CET	CEP	Action on the Rising Clock Edge (\bar{J})
1				L	X	X	X	RESET (Clear)
2	CP	TC	15	H	L	X	X	LOAD ($P_n \rightarrow Q_n$)
3	P_0	Q_0	14	H	H	H	H	COUNT (Increment)
4	P_1	Q_1	13	H	H	L	X	NO CHANGE (Hold)
5	P_2	Q_2	12	H	H	X	L	NO CHANGE (Hold)
6	P_3	Q_3	11					
7	CEP	CET	10					
8	GND	PE	9					

*For the 162 and 163 only.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SN74163

*MR for 160 and 161
*SR for 162 and 163

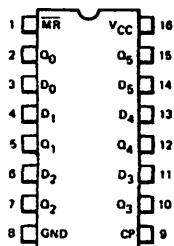
SNS4165, SN54LS165...J OR W PACKAGE
SN74165, SN74LS165...J OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

SHIFT/ LOAD	CLOCK INHIBIT	INPUTS		INTERNAL OUTPUTS		OUTPUT Q_H
		CLOCK	SERIAL	PARALLEL	A...H	
L	X	X	X	X	a...h	a b h
H	L	L	X	X	X	$Q_{A0} Q_{B0} Q_H$
H	L	↑	H	X	X	$H Q_{A_n} Q_{G_n}$
H	L	↑	L	X	X	$L Q_{A_n} Q_{G_n}$
H	H	X	X	X	$Q_{A0} Q_{B0}$	$Q_{A0} Q_{B0} Q_H$

SN74165



TRUTH TABLE

Inputs ($t = n$, $\bar{MR} = H$)		Outputs ($t = n+1$) Note 1	
D		Q	
H		H	
L		L	

Note 1: $t = n + 1$ indicates conditions after next clock.

SN74174

MODE SELECT TABLE

MR	PL	CP _U	CP _D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	J	H	Count Up
L	H	J	J	Count Down

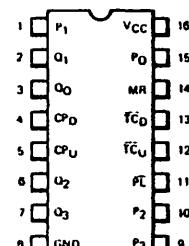
L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

J = LOW-to-HIGH Clock Transition

CONNECTION DIAGRAM
DIP (TOP VIEW)



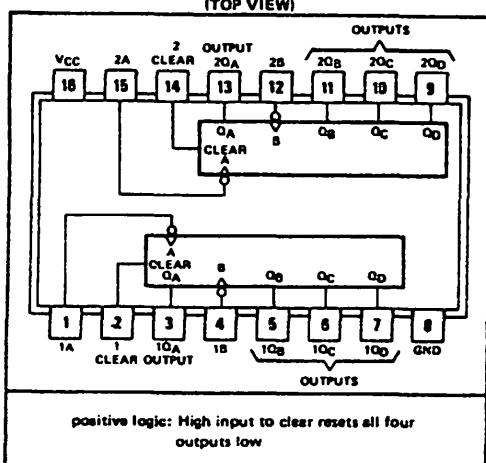
SN74193

SNS4390, SN54LS390...J OR W PACKAGE

SN74390, SN74LS390...J OR N PACKAGE

(TOP VIEW)

SN74390



'390, 'LS390
BCD COUNT SEQUENCE
(EACH COUNTER)
(See Note A)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

NOTES: A. Output Q_A is connected to Input B for BCD count.
B. Output Q_D is connected to Input A for bi-quinary count.
C. H = high level, L = low level.

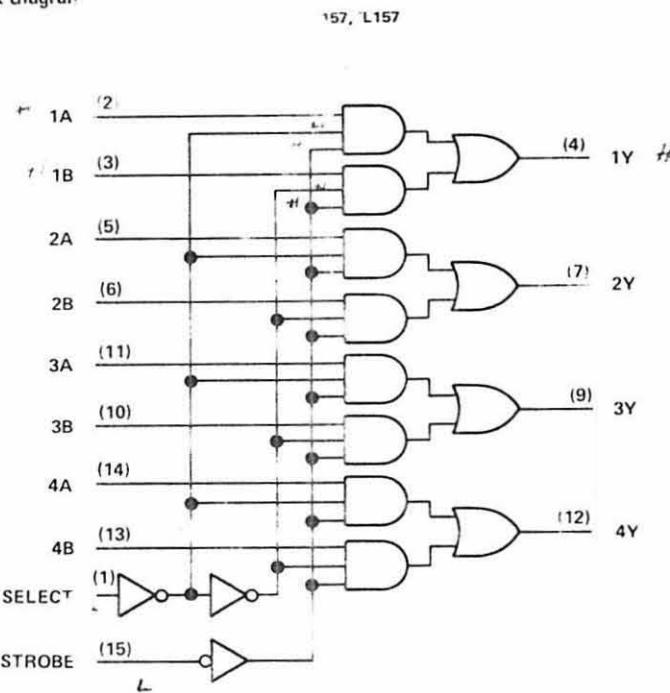
FUNCTION TABLES

'390, 'LS390
BI-QUINARY (5-2)
(EACH COUNTER)
(See Note B)

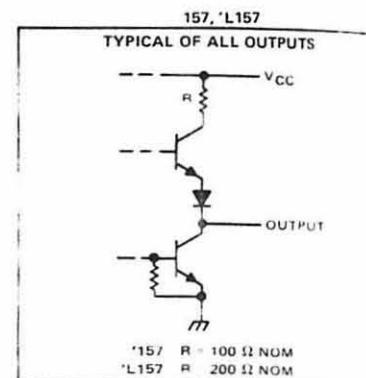
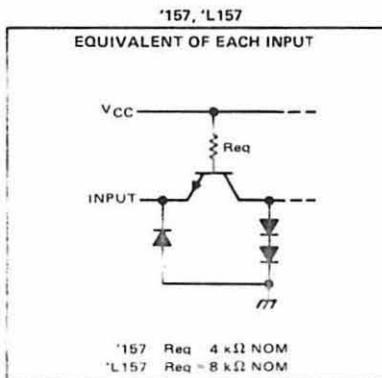
COUNT	OUTPUT			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

**TYPES SN54157, SN54L157, SN74157 SN74L157,
QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS**

functional block diagram



schematics of inputs and outputs



signetics

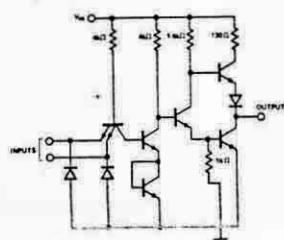
QUADRUPLE INPUT
POSITIVE AND GATES

**S5408
N7408**

S5408-A,F,W • N7408-A,F

DIGITAL 54/74 TTL SERIES

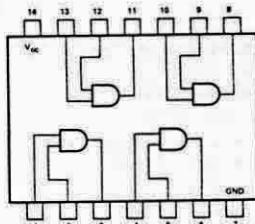
SCHEMATIC DIAGRAM



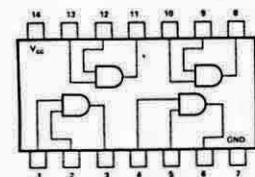
NOTE: Component values shown are nominal.

PACKAGINGS

W PACKAGE



A PACKAGE



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} : S5408 Circuits N7408 Circuits	4.5	5	5.5	V
Normalized Fan-Out from Output, N	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A : S5408 Circuits N7408 Circuits	-55	25	125	°C
	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	TEST CONDITIONS*			UNIT
		MIN	TYP**	MAX	
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 1 level at output	$V_{CC} = \text{MIN}$		2	V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 0 level at output	$V_{CC} = \text{MIN}$		0.8	V
$V_{out(1)}$	Logical 1 output voltage	$V_{CC} = \text{MIN}$, $I_{load} = 800\mu\text{A}$	$V_{in} = 2.0\text{V}$,	2.4 3.3	V
$V_{out(0)}$	Logical 0 output voltage	$V_{CC} = \text{MIN}$, $I_{sink} = 16\text{mA}$	$V_{in} = 0.8\text{V}$,	0.22 0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	$V_{CC} = \text{MAX}$	$V_{in} = 0.4\text{V}$	-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	$V_{CC} = \text{MAX}$, $V_{CC} = \text{MAX}$	$V_{in} = 2.4\text{V}$ $V_{in} = 5.5\text{V}$	40 1	μA mA
I_{OS}	Short circuit output current†	$V_{CC} = \text{MAX}$	$S5408$ $N7408$	-20 -18	-55 -55

SIGNETICS QUADRUPLE 2-INPUT POSITIVE AND GATES ■ S5408, N7408

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
I _{CC(1)} Logical 1 level supply current	V _{CC} = MAX, V _{in} = 5V		10	15	mA
I _{CC(0)} Logical 0 level supply current	V _{CC} = MAX, V _{in} = 0		18	26	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{pd0} Propagation delay time to logical 0 level	C _L = 15pF, R _L = 400Ω		12	19	ns
t _{pd1} Propagation delay time to logical 1 level	C _L = 15pF, R _L = 400Ω		17.5	27	ns

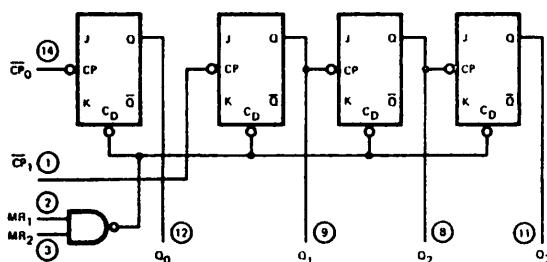
* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C

† Not more than one output should be shorted at a time.

LOGIC DIAGRAM

SN7493 - 4-BIT BINARY COUNTER

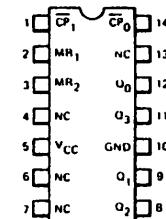


○ = Pin Numbers

V_{CC} = Pin 6

GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



NC = No Internal Connection

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

COUNT	OUTPUT			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	H
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Note: Output Q₀ connected to input CP₀

MONOSTABLE MULTIVIBRATORS

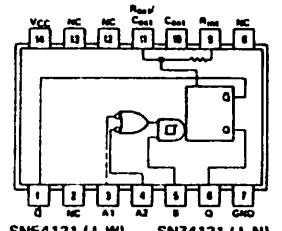
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FUNCTION TABLE

INPUTS		OUTPUTS	
A1	A2	B	Q
L	X	H	L H
X	L	H	L H
X	X	L	L H
H	H	X	L H
H	I	H	◻ □
I	H	H	◻ □
I	I	H	◻ □
L	X	I	◻ □
X	L	I	◻ □

See page 6-64

- NOTES:
- An external capacitor may be connected between C_{ext} (positive) and R_{ext}/C_{ext}.
 - To use the internal timing resistor, connect R_{int} to V_{CC}. For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open circuited.



SN54121 (J, W) SN74121 (J, N)
SN54L121 (J, T) SN74L121 (J, N)

'121 ... R_{int} = 2 kΩ NOM

'L121 ... R_{int} = 4 kΩ NOM

NC = No internal connection

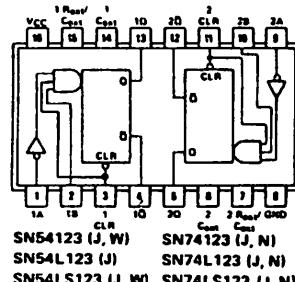
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

123

FUNCTION TABLE

INPUTS		OUTPUTS	
CLEAR	A	B	Q
L	X	X	L H
X	H	X	L H
X	X	L	L H
H	L	I	◻ □
H	I	H	◻ □
I	L	H	◻ □

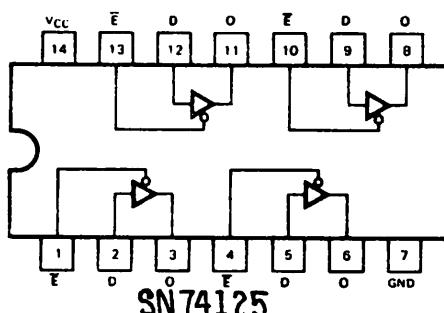
See page 6-76



SN54123 (J, W) SN74123 (J, N)

SN54L123 (J) SN74L123 (J, N)

SN54LS123 (J, W) SN74LS123 (J, N)

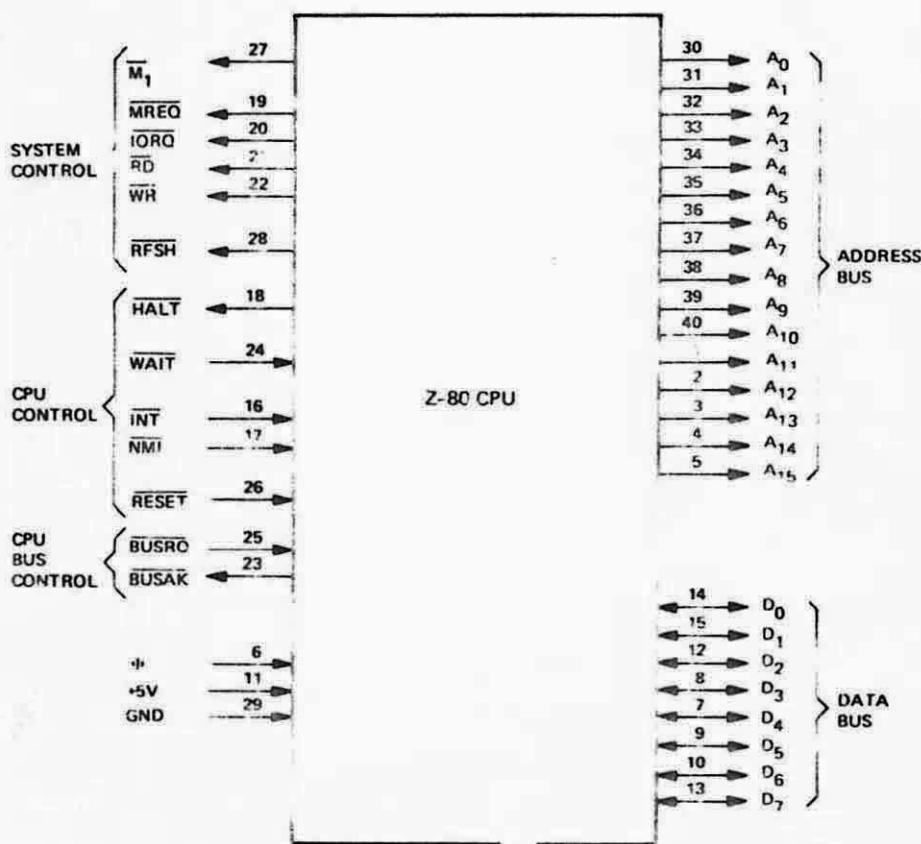
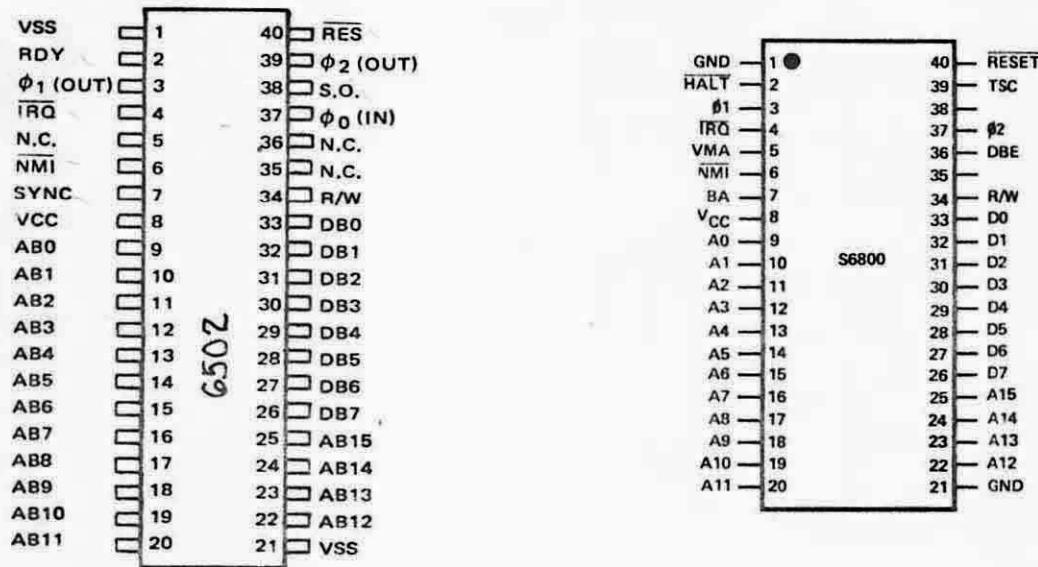


SN74125

SN74125 - QUAD TRI-STATE BUFFER

TTL

MICROPROCESSORS



Z-80 PIN CONFIGURATION