Improving the OSI Challenger C2

Part 2 continues with video, cassette and keyboard modifications.

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The model 540 video board is a video interface board with the following hardware features:

- 2K video RAM.
- A 2513 character generator or the optional CG-4 character generator.
- A programmable video display for a 32 × 32 or 64 × 64 character display.
- Normal or reversed video display.
- The analog portion of an audio cassette interface.
- Keyboard interface.

Video Display

The video display utilizes a crystal control clock, which feeds a divider chain to provide the horizontal and vertical sync pulses and the row and column addresses to access the display memory. The board typically operates with the display memory consistently feeding its data to the character generator and then to the display. The CPU, however, can access this memory so that it can be written into or read from just like any other memory location.

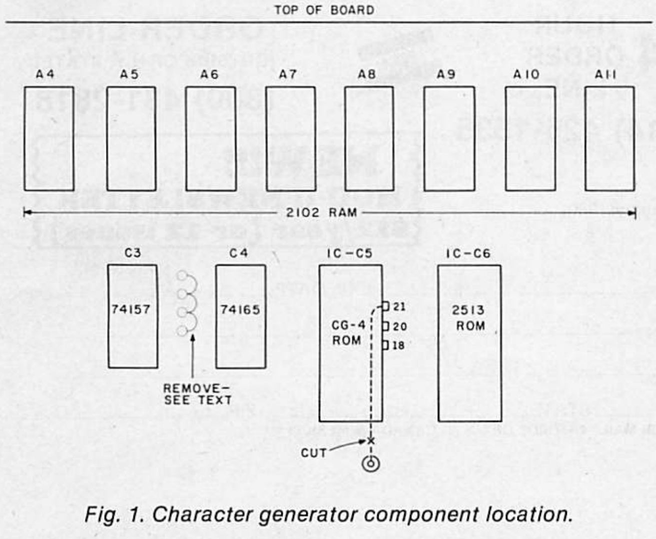

Fig. 1. Character generator component location.

Character Generator

The 540 board may come with a 2513 character generator ROM to provide 64 uppercase ASCII characters or OSI's CG-4 ROM that provides 256 numeric, graphic and gaming elements displayed in an 8 × 8 dot array.

You must make the following board modifications to convert from the 2513 ROM to the CG-4 ROM:

1. Remove the 2513 ROM, which is no longer needed and can be discarded.
2. At the spare 24-pin socket at C5, check for a ground on pin 20 and +5 V on pins 18 and 21 (see Fig. 1).
3. Cut the foil trace that runs on the component side of the board from pin 20 to a feed-through hole at the bottom of the socket.
4. Install a jumper between pin 20 and pin 21 of the socket.
5. Check for +5 V on pins 18, 20 and 21.
6. Locate four wire-wrap pins between the 74165 and 74157 IC, locations C3 and C4 (see Fig. 1).
7. Remove the jumpers that strap these pins together.
8. Install four 2102 RAMs in the spare memory sockets at locations A7, A8, A15 and A16.
9. Install the CG-4 ROM in the socket at location C5.
10. Run the Character Generator Test program (Listing 1). The generator should display 256 separate characters.

```
10 FOR CL = 1 TO 2048
20 POKE 53247 + CL, 32:NEXT CL
30 LN = 0:AS = 0
40 FOR SP = 1 TO 64 STEP 2
50 POKE 53695 + SP + LN, AS
60 AS = AS + 1:NEXT SP
70 LN = LN + 192
80 IF LN <1536 GO TO 40
```

Listing 1. Character Generator Test program.

You can also replace the character generator with a 2716 EPROM that has been user programmed to provide a completely different font. Either way, the video display will now provide more characters than the basic 64 uppercase of the 2513.

After the data leaves the character generator, it goes to an eight-bit parallel shift register and then through two in-

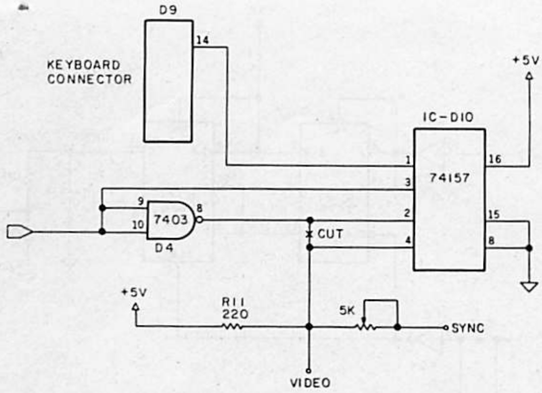

Fig. 2. Reverse video circuit.

verting buffers to the mixing circuit, where it is combined with the horizontal and vertical sync to produce the composite video signal.

Screen Size and Reverse Video

The 540 schematic notes indicate that the inverters may be bypassed for reverse video. Although this is a desirable feature, it would be better to be able to reverse the video signal under program control similar to the operation of changing the screen size.

A one-bit programmable latch is used to control the screen size. A 7474 IC (dual D flip-flop) is addressed and triggered to pass on the status of data bit 0 and 1. The status, a low or high, is latched by the flip-flop and used to activate a 74157 IC (1 of 2 data selector), which will then route one of two signals to other logic circuits.

In the case of the screen size change, one half of the 7474 uses the status of data bit 0 to select the clock signal directly and feed it to the dot clock and address counter chain or to select the clock signal divided by two and then feed it to the dot clock and address counter chain. If data bit 0 is low, then the screen size will be 32 × 32, which will provide a symmetrical dot array for graphics, plotting and video games. A high will give the standard 32 × 64 display.

The other half of the 7474 uses the status of data bit 1; however, the latched signal is not used to control any other logic circuit. I used this latched signal to control a new data selector that routes the video signal directly to the mixing circuit or bypasses one buffer and then routes the video signal to the mixing circuit (see Fig. 2).

Make the following modifications to implement the programmable reverse video:

1. Install a 16-pin IC socket at location D10, a prototype area (see Fig. 3).
2. Run four wires from IC socket D10, pins 1, 2, 3 and 4 to ICD9 socket, pin 14; ICD4, pins 8 and 10; and to R11 (see Figs. 2 and 3).
3. Jumper pins 8 and 15, ICD10 to the ground bus at the bottom of the IC.
4. Jumper pin 16, ICD10, to the +5 V bus at the top of the IC.
5. On the component side of the board, cut the foil trace from R11 to ICD4, pin 8. The trace is under the chip and appears at the top of the chip (see Fig. 3).
6. Check wiring, then install a 74157 in socket D10.
7. Turn on the computer. The video display should be the standard 32 × 64 display with white characters.

With the completion of this modification, you will have the ability to select four video display formats under program control (see Table 1). Although the video can now display both black and white characters, it cannot display both at the same time. In addition, you will have to adjust the video monitor controls to provide the sharpest characters in both the black and white display.

Audio Cassette Interface

	characters/line		character color	
Data	32	64	White	Black
0	X		X	
1		X	X	
2	X			X
3		X		X

Table 1. Screen options. Address DEXX hex (56900).

The May issue of *Kilobaud Microcomputing* contained an article ("High-Speed Cassette Interface," p. 42) describing the construction of a high-speed cassette interface. I used this information to modify the cassette interface.

The 540 board contains all of the components that make up the analog input and output portion of an audio cassette port. In conjunction with the 6850 ACIA on the 500 board, the interface is able to provide off-line data storage to an audio cassette.

A printer or data set will not work with the serial interface while the cassette transmit and receive leads are wired to the 540 board. Therefore, it is necessary to open these leads when you use the serial interface to operate a printer. I used a three-pole on-off switch to open the cassette transmit and receive leads and remove the ground from the $\overline{CTS}$ lead (see Fig. 4). The printer grounds the $\overline{CTS}$ lead when it is attached to the EIA connector and the power is on.

The audio cassette interface uses the Kansas City Standard format for converting the data bits to an audio signal that is recorded on the cassette. The Kansas City Standard is an FSK (frequency shift keying) system that keys a change in the binary value transmitted by a change in frequency. The 0s and 1s from the computer are converted to two different frequencies, 1200 Hz and 2400 Hz, which are then converted to a sine wave and recorded on an audio cassette. On playback, the receiving circuit detects the frequency shifts and converts them into 0s and 1s for input to the computer.

The cassette interface is normally operated at 300 baud. At this rate, a data zero is four full cycles of 1200 Hz, and a one is eight full cycles of 2400 Hz. If the interface were operated at 1200 baud, the cycles would be one-quarter of the 300 baud rate. A data zero is then one full cycle of 1200 Hz, and a one is four full cycles of 2400 Hz.

The transmitter circuit (Fig. 5) consists of a 7476 IC (dual JK flip-flop) wired to divide the clock by two or divide by four. To produce the 1200 Hz and 2400 Hz, the clock frequency must be

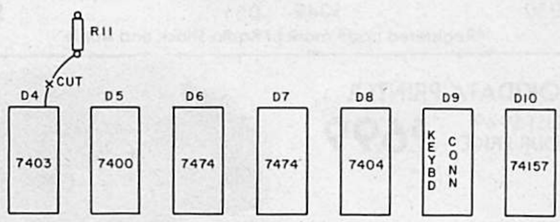

Fig. 3. Reverse video component location.

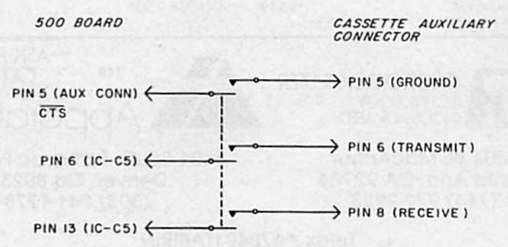

Fig. 4. Printer/cassette select switch.

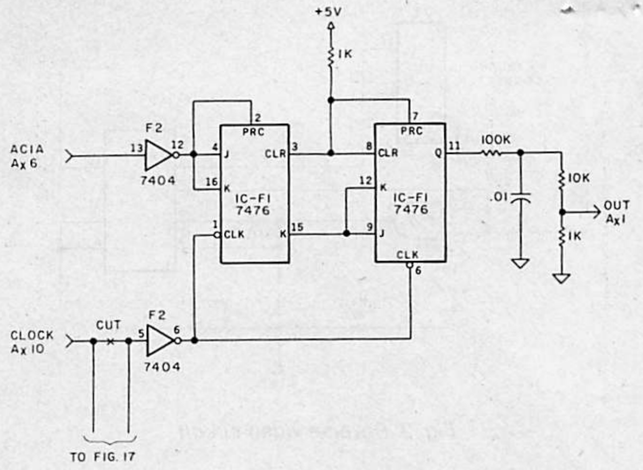

Fig. 5. Cassette transmit circuit.

4800 Hz, which is available from the 6850 clock circuit when it is operating at the 300 baud rate. However, when operating at the 1200 baud rate, the clock frequency increases to 19200 Hz.

For the transmit circuit to work at the 1200 baud rate, the 19200 Hz clock must be divided by four to produce 4800 Hz, which is needed to clock the JK flip-flop. A new 7474 IC (dual D flip-flop) is wired to divide the clock by four (see Fig. 6), while one-half of 74123 (dual monostable multivibrator) is wired to control the operation of the 7474.

Circuit Operation

At 1200 baud the 74123's clear lead is grounded through the baud rate selector switch (see Fig. 5, part 1). This inhibits triggering; the 74123 $\overline{Q}$ and 7474 clear pins go high; and the circuit divides normally. The 19200 Hz clock is divided by four and fed to the 7404 inverter (Fig. 5), where it is then converted to 2400 Hz or 1200 Hz by the operation of the 7476.

At 300 baud the 74123 clear lead is high. As the ACIA clock changes from high to low, the circuit triggers and makes the $\overline{Q}$ lead low, which then clears the 7474 IC. The overall effect is to pass the ACIA clock frequency through the 7474 without dividing it.

The 1200 Hz and 2400 Hz from the 7476 IC are then sent to a low-pass filter, which rounds off

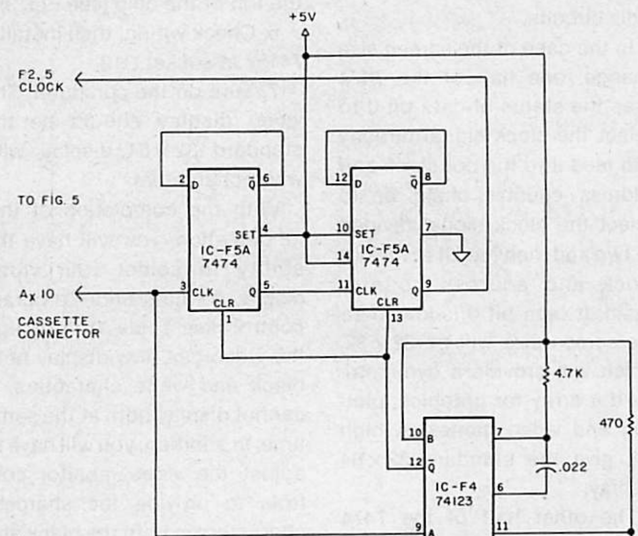

Fig. 6. Cassette 1200 baud modification circuit.

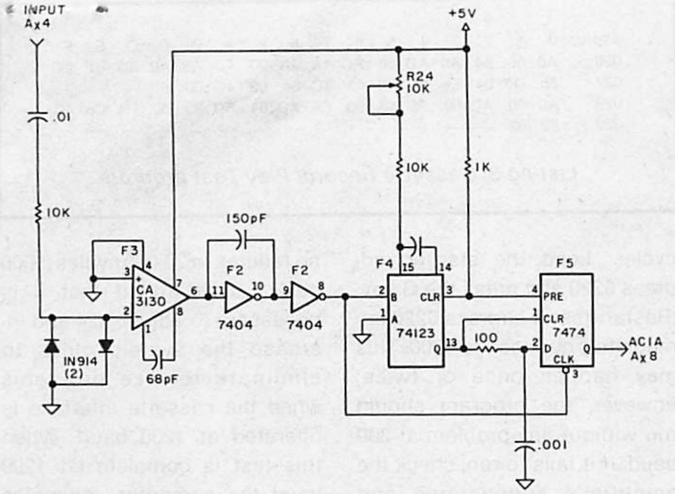

Fig. 7. Cassette receive circuit.

the square wave to provide a sine wave to the tape recorder (see Fig. 5).

The sine wave from the audio cassette is limited and converted to a square wave and then fed to one-half of a 74123 (monostable multivibrator) and one-half of a 7474 (D flip-flop). See the receive circuit in Fig. 7.

The 74123 is adjusted for a frequency between 1200 and 2400 Hz, which will constantly retrigger the 74123 and produce a constant high output, which will be clocked through the 7474 to produce a 1. 1200 Hz will clock through the circuit and produce a 0. The 0 and 1 are then sent to the 6850 chip.

Cassette record and play at 300 baud and 1200 baud is now possible with the following modification steps (see Fig. 8):

1. Install a 14-pin IC socket at location F5A.
2. Jumper pin 1 to 13, 2 to 6, 5 to 11 and 8 to 12 on the 7474.
3. Jumper pin 7 to ground.
4. Jumper pins 4, 10 and 14 to +5 V.
5. Install a 4.7k resistor between +5 V and pin 7 of the 74123 at location F4.
6. Install a .022 uF capacitor between pins 6 and 7, ICF4.
7. Install a 470Ω resistor between +5 V and pin 11, ICF4.
8. Jumper pin 10 of ICF4 to +5 V.
9. Jumper pins 9 and 12, ICF4, to pins 3 and 1, ICF5A.
10. Cut foil trace at pins 10 and 11 of the cassette auxiliary connector.
11. Run three wires from pin 11 and 10 of the connector and ICF2, pin 5, to ICF4, pin 11, and ICF5A, pins 3 and 9.
12. Run a wire from the auxiliary plug, pin 11, to the 1200 baud pin of the B part of the baud select switch (see Fig. 5, part 1).
13. Install a 7474 IC in socket.
14. Connect an amplifier to the cassette interface input/output jacks. Adjust the volume at the midpoint.
15. Connect a logic probe to pin 6 of the cassette auxiliary connector. It should be high.

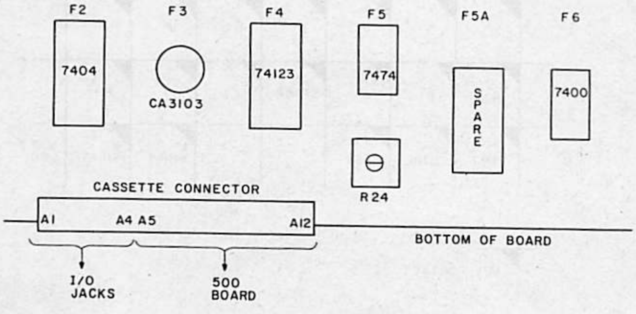

Fig. 8. Cassette component location.

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address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
022	A9	00	AA	A8	85	A0	85	A1	85	A2	85	A3	AD	00	FC	4A
023	4A	90	F9	A5	A0	8D	01	FC	AD	00	FC	4A	90	FA	AD	01
024	FC	C5	A0	D0	0F	E6	A0	D0	E3	E6	A2	D0	DF	E6	A3	D0
025	DB	4C	00	FF	85	A1	A9	4D	4C	46	FF	—	—	—	—	—

Listing 2. Cassette I/O Loop Test program.

address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
026	A0	00	84	A0	AD	00	FC	4A	4A	90	F9	A5	A0	8D	01	FC
027	88	D0	04	E6	A0	F0	03	4C	64	02	4C	00	FF	—	—	—
028	A0	00	AD	00	FC	4A	90	FA	AD	01	FC	99	00	D4	C8	4C
029	82	02	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Listing 3. Cassette Record/ Play Test program.

Connect a logic probe to pin 8 of the cassette connector. The pin should be high; if not, adjust R24 (see Fig. 8) until it goes high.

16. Ground pin 6 of the connector. Pin 8 should now be low; if not, adjust R24 until it goes low. Remove ground and check that pin 8 goes high.

17. Recheck that pin 8 is low when pin 6 is grounded and high when not grounded. This is the only adjustment at this time for the interface to operate.

18. Run the test program in Listings 2 and 3.

Listing 2 tests that the byte received is the same as the one transmitted. Listing 3 records the characters on a tape, which is then played back and displayed on the screen. There is no comparison made between transmit and receive data, except what is displayed on the screen.

Test Setup

Connect the amplifier or cassette to the input/output jacks and adjust the volume at the midpoint. Type in the machine-language program for the Cassette Loop test (Listing 2) and the Cassette Record/Play test (Listing 3). (Refer to the C2 or 500 board manuals for instructions on entering machine-language programs into the computer. The cassette interface should first be tested at 300 baud. If there are no problems, then test the 1200 baud operation.)

Listing 2 will check 256 characters continuously for 65,000 cycles. Load the starting address 0220 and press the G key. (Restart test if address 0220 immediately changes to 0000. This may happen once or twice; however, the program should run without any problem at 300 baud. If it fails to run, check the amplifier's connections and volume setting.)

When the program fails to compare the character received with that transmitted, it will bring up address 0000 on the screen. (Memory address 00A0 to 00A3 will load with the information needed to analyze the failure.)

Access address 00A0 for the character transmitted and 00A1 for the character received. (The information is in hexadecimal and must be converted to binary so that the bits can be compared.) Access address 00A3 and 00A2 to compute the number of cycles completed. (A3 is the high byte, and A2 is the low byte in hexadecimal.)

Rerun the test until there are no failures in 20,000 cycles (5000 hex). I have found that it is necessary to adjust R24 and increase the system clock to eliminate receive problems when the cassette interface is operated at 1200 baud. When this test is complete (at 1200 baud the computer completes 1420 cycles per hour), run the Record/Play test.

I was able to use my cassette recorder (Radio Shack CTR-39) connected normally. A blank cassette (no tape) is placed in the recorder and the Record/Play buttons are operated. The input signal is amplified and sent to the ear jack. During record, the volume control is inoperative; however, the amplified signal is more than adequate to drive the cassette interface.

To run Listing 3, operate Record/Play on cassette, load the starting address 0260 hex and press the G key. When the program is complete the C/W/M? will appear.

COLUMN

ROW \ BIT	7	6	5	4	3	2	1	0
7	1	2	3	4	5	6	7	
6	8	9	Ø	:	---	RUB OUT		
5	'	L	O	LF	CR			
4	W	E	R	T	Y	U	I	
3	S	D	F	G	H	J	K	
2	X	C	V	B	N	M	.	
1	Q	A	Z	SPACE	/	;	P	
0	REPT	CTRL	ESC			L SHIFT	R SHIFT	SHIFT LOC

KEY CONTACT

Table 2. Keyswitch matrix.

Access the machine monitor and load the address 0280 hex. Press the G key, and then operate Play on the cassette.

An ASCII character will be displayed 256 times on the screen before a new character is displayed. All 256 characters will be displayed before the program is completed. By observing the screen, you can detect any failures (a different character appears in place of the character being displayed).

These programs were run at 300 and 1200 baud. There were no errors at 300 baud. At 1200 baud there were many errors, which I eliminated after I increased the CPU clock to 1.58 MHz. After several months use at the 1200 baud rate, I have not had any problem; however, I do maintain a backup of all programs recorded at 300 baud.

542 Keyboard

The 542 polled keyboard uses 53 keyswitches and the microprocessor to provide the functions of a standard keyboard encoder chip. In normal operation, the CPU writes a byte of data, corresponding to a row of keys, to the keyboard address (DFXX hex). The CPU then reads a byte of data from the keyboard that corresponds to the column of the key closure.

When the CPU finds a key closure, it translates the row and column value to an ASCII code for use by the software seeking input from the keyboard (see Table 2). This polled keyboard has an advantage over a standard ASCII keyboard, which can also be used with the 540 board since it is simple to utilize the keys directly for some specific use.

Listing 4 shows a BASIC program that loads a row address and reads the column address so that complicated operations can be programmed as single keystrokes or multiple simultaneous keystrokes. The versatility of multiple, simultaneous keystrokes is not available when the keyboard is operating in the ASCII mode, since the software monitor provides roll-over protection.

With the polling feature, you can install any arrangement of switches to meet a specific need, including a quasi joystick.

Circuit Board Modification

In the upper corner of the keyboard, there is a prototype area that will accept two or three IC sockets. Follow these steps:

1. Install a 16-pin IC socket on the circuit board.
2. Wire the socket to the eight row address diodes and the eight column address pull-up resistors (see Fig. 9).
3. Use a 16-lead, double-ended DIP jumper cable to connect the keyboard to a specialized keyboard outside the case.

I have added two special keyboards, a hexadecimal keypad (Jameco) and a five-button quasi joystick. The hexadecimal keypad switches are wired to a 16-pin IC socket such that when connected to the main keyboard they will produce the same row and column address as the main keyboard (0 to 9, A to F and three additional keys).

The five-button keypad is wired to produce five column addresses with any one row address (see Fig. 10). With this ar-

```
POKE 530, 1          The control C must be
                     deactivated before checking
                     for a keystroke
POKE 57088, R*       select row
X = PEEK (57088)*    check column
```

*The decimal equivalent of the row or column bit is as follows:

on bit	7	6	5	4	3	2	1	0
decimal	128	64	32	16	8	4	2	1

Only one row bit is turned on at a time.
The column value is dependent on the number of keys pressed.

Listing 4. The BASIC program interpreting a keystroke.

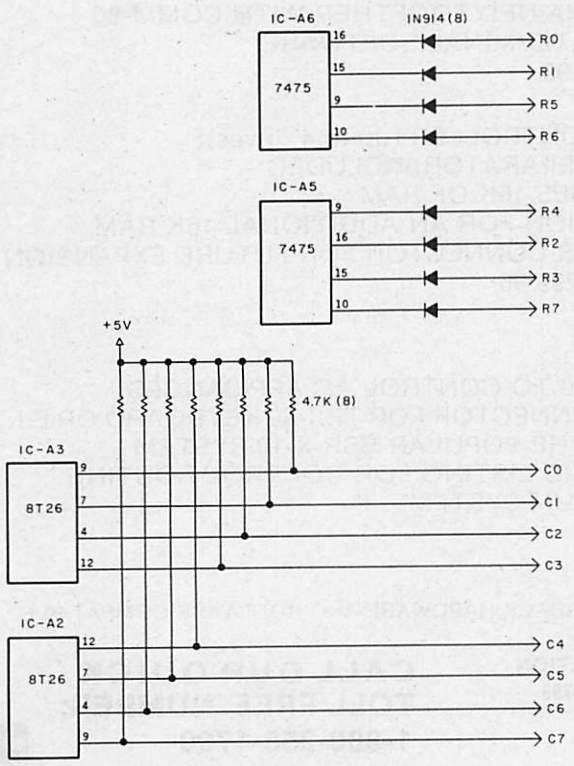

Fig. 9. Keyboard row and column components.

rangement it is possible to define four separate directions (N, S, E and W) with the single keys, and four alternate directions (NE, SE, SW and NW) with a multiple, simultaneous operation of a pair of keys.

You can incorporate the BASIC program in Listing 4 in a larger program that will select a subroutine based on the value of the column address.

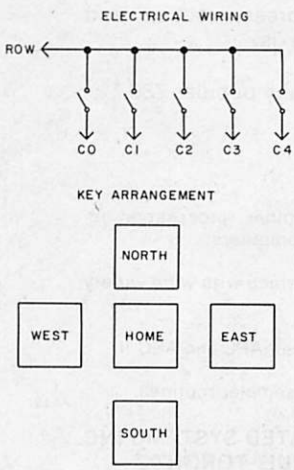

Fig. 10. Five-button joystick.

Conclusion

I completed the modifications over the course of one year, and had little time to develop much software. While there may be some additional room for hardware modifications, in the future I will be concentrating on software development and the study of the BASIC and monitor firmware. ■

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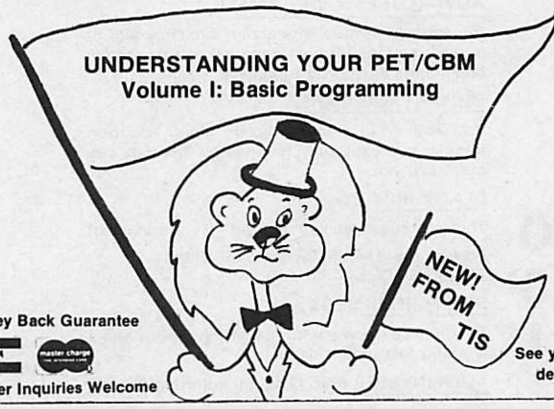

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