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Assignment 2

Chapter 4: Introduction to Computer Organization

**4.1 Basic Computer Organization**

A simple computer has three primary subsystems: The Central Processing Unit (CPU), the memory subsystem, and the Input/Output (I/O).

Bus: a set of wires, used to send information form one component to another, the data from system becomes the input for another system.

Three Buses:

Address bus: gets the address of data in the system, so the CPU outputs the address of a device on the bus. Therefore, the other systems can use them for instructions.

Data Bus: the bus that contains the data of a certain address in memory.

Control Bus: which consists of ‘n’ lines that can either, data is read into or written out of the CPU, whether the CPU is accessing memory or an I/O device, and whether the I/O device or memory is ready to transfer data.

I/O Bus: accesses all I/O devices.

Instructions Cycle: the procedure a microprocessor goes through to process an instruction. Fetch -> Decode -> Execute.

The computer uses a system clock to synchronize its operations. Helps with the READ and WRITE controls to get instruction code to put on the bus (read) and store the data (write).

**4.2 CPU Organization**

The CPU controls the computer. Has three sections: Register Section, which contain set of registers and a bus, the control unit that controls the CPU using signals, and the ALU (arithmetic/logic unit) performs most of the arithmetic and logical operation.

**4.3 Memory Subsystem Organization and Interfacing**

ROM: Read Only Memory, which are, programmed unit before they are added to the computer system. RAM: Random Access Memory (read/write memory)

ROM chips are different by how they are programmed.

Masked ROM, programmed with data as the chip is fabricated.

A Programmable ROM, which can be programmed by the user from any ROM programmer. An Erasable PROM can be programmed like a PROM but its contents can be erased and reprogrammed.

All ROMS have 2^n words with each having m data outputs, it has a chip enable and output enable.

RAM chips are different by how they are maintain data. External configuration is the same, each 2^n \* m chip has ‘n’ address inputs and ‘m’ bidirectional data pins. RAM chips has chip enable. Unless the chip enables are active, the chip’s outputs are tri-stated.

For chip organization of ROM/RAM; as the number of locations increases, the size of the address decoder needed in a linear organization becomes prohibitively large. The size of n to 2^n decoder is said to be O(2^n). Two or more chips can be combined to create memory with more bits per locations by connecting the addresses and controls of different chips. Chips can be combined to create more words.

For computers that are more complex: computers include small, high-speed cache memory. The cache serves as a location where data can be accessed quicker than its original address that is maintained through a cache control, which controls the flow of data. They also use Virtual Memory a hard disk as part of the computer’s memory, which minimizes the cost of memory. Since a byte of a hard disk costs less than a ROM.

**4.4 I/O Subsystem Organization and Interfacing**

Each memory location performs the same function; it stores a data value or an instruction for use by the CPU. Interfaces between the CPU and the I/O devices are very similar. Each I/O device also has a unique address. The enable logic must not enable the buffers unless it receives the correct address from the address bus. Load logic is the enable logic of the device interface. When the logic receives the correct address and the control signals, it asserts the LD signal of the register, causing it to read data form the system’s data bus.

When there are devices that used both input and output, it requires combined interfaces that is two interfaces.

One downfall of I/O devices is that they are much slower than CPU and memory. This cause I/O devices to have timing issues with the CPU. For this reason there is a READY signal in CPU alleviate this problem as well as interrupts so CPUs can do work while waiting for a slower device.

Direct Memory Access (DMA): is a method used to bypass the CPU in these transfers, thus performing them much more quickly.

**4.5 A Relatively Simple Computer**

Contains 16 address pins, it accesses the system data bus. It uses memory mapped I/O.

It has 8K of ROM and 8K of RAM. Note: 8K of memory has 2^13 internal memory locations. The RAM has two control inputs, RD and RW, which are controlled through the READ and WRITE signals.

**4.5 Real World Example: An 8085-based computer**

Address Latch Enable signal (ALE): set to 1 during the first clock cycle of a memory or I/O access, and 0 for the duration of the rest access.

Foldback: it reduces the logic needed to generate the enable signal.

Data Direction Register (DDR): which determines whether A or B are input or output ports. The CPU writes data to the DDRs to set the direction of the port.