



# Emulation of Aerospace Actuation Systems

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## Project Relevance

- ➔ Woodward, Inc. is validating an electrical drive alternative to replace current thrust reverser actuation systems
- ➔ Replacing hydraulically/pneumatically powered parts with electric drive systems can result in the following benefits:
  - ➔ Reduced weight
  - ➔ Reduced maintenance
  - ➔ Additional data analytics for real-time system prognostics
- ➔ A controller hardware in the loop (CHIL) platform allows for verification of these claims without incurring excessive research/dev costs

## Main Project Goals

- ☑ Create a modular CHIL system for use by current & future CSU project teams, specifically the EMTRAS project
- ☑ Determine analog & digital I/O requirements for the microcontroller and OPAL-RT interface
- ☑ Develop C code to run a closed-loop CHIL experiment on a real-time DC machine system model loaded onto the OPAL-RT
- ☑ Create a GUI in LabVIEW to view real-time outputs from the system under test

## Stretch Goals

- ☑ Construct a 3D printed enclosure to neatly organize the physical HIL architecture
- ☑ Document all design steps and experimental results in detailed report packages
- ☑ Include system requirements flow-through and design information using the principles of model-based systems engineering (MBSE)
- ☐ [IN WORK] Design a PI control loop to generate/validate stable outputs from the OPAL-RT, then verify through unit testing

## Budget

Item	Cost (with S/H)	Order Date
BNC-miniBNC Connector	(\$7.63)	9/21/2021
TI Microcontroller (x2) & Dev Board (x1)	(\$515.23)	2/18/2022
DB9 Connectors & Fasteners	(\$15.05)	4/1/2022
E-Days Materials	(\$61.77)	4/11/2022
Total Starting Budget	\$600.00	
Total Expenses	(\$599.68)	
Total Ending Budget	\$0.32	

## Physical HIL Architecture

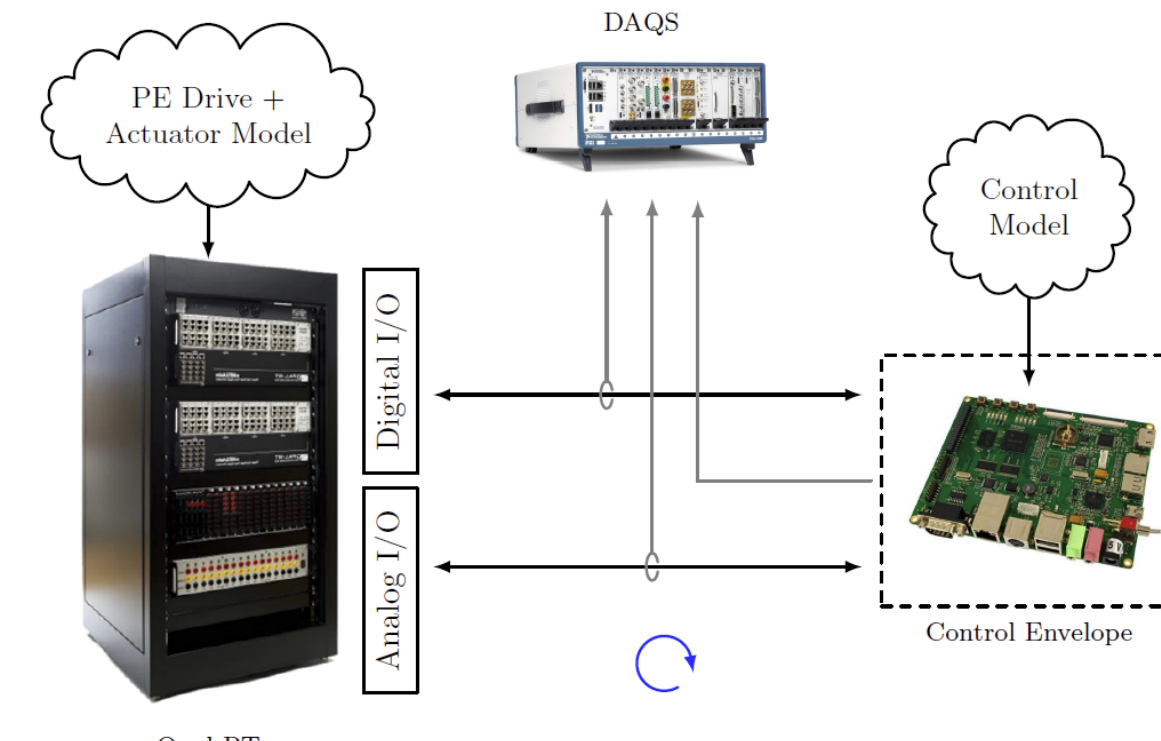


Fig. 1 - CHIL System Architecture

### Hardware Elements:

- ➔ TI TMS320F28379D Microcontroller & Dev Board
- ➔ OPAL-RT 5620
- ➔ NI cRIO Controller
- ➔ 3D Printed Microcontroller Enclosure
- ➔ DB9 Wire Harness

### Constraints:

OPAL 5600 RT Machine	TI TMS320F28379D
<ul style="list-style-type: none"><li>I/O: -30V to 30V</li><li>OPAL 5620 8 I/O Flat Carrier:<ul style="list-style-type: none"><li>output: +/- 12VDC @ 1.2A (mezzanine A/B)</li><li>output: +/- 18VDC @ 0.8A (mezzanine A/B)</li><li>input: +/- 12VDC @ 6A; +/- 5VDC @ 3A</li></ul></li><li>OPAL 5142 Digital I/O: 0-3 V</li><li>Onboard XILINX Spartan 3A FPGA: 3.3V (LVTTTL)</li><li>12 nodes maximum</li><li>Requires miniBNC connector</li></ul>	<ul style="list-style-type: none"><li>3.3V I/O design</li><li>-0.3V min to 4.6V max (0-3.3 V nominal operating range)</li><li>-20mA to 20mA</li><li>50 kHz synchronization rate</li><li>Requires code written in C (no object-oriented functionality)</li><li>Requires code to be written in the TI Code Composer Studio IDE</li></ul>

### Prototype Evolution:

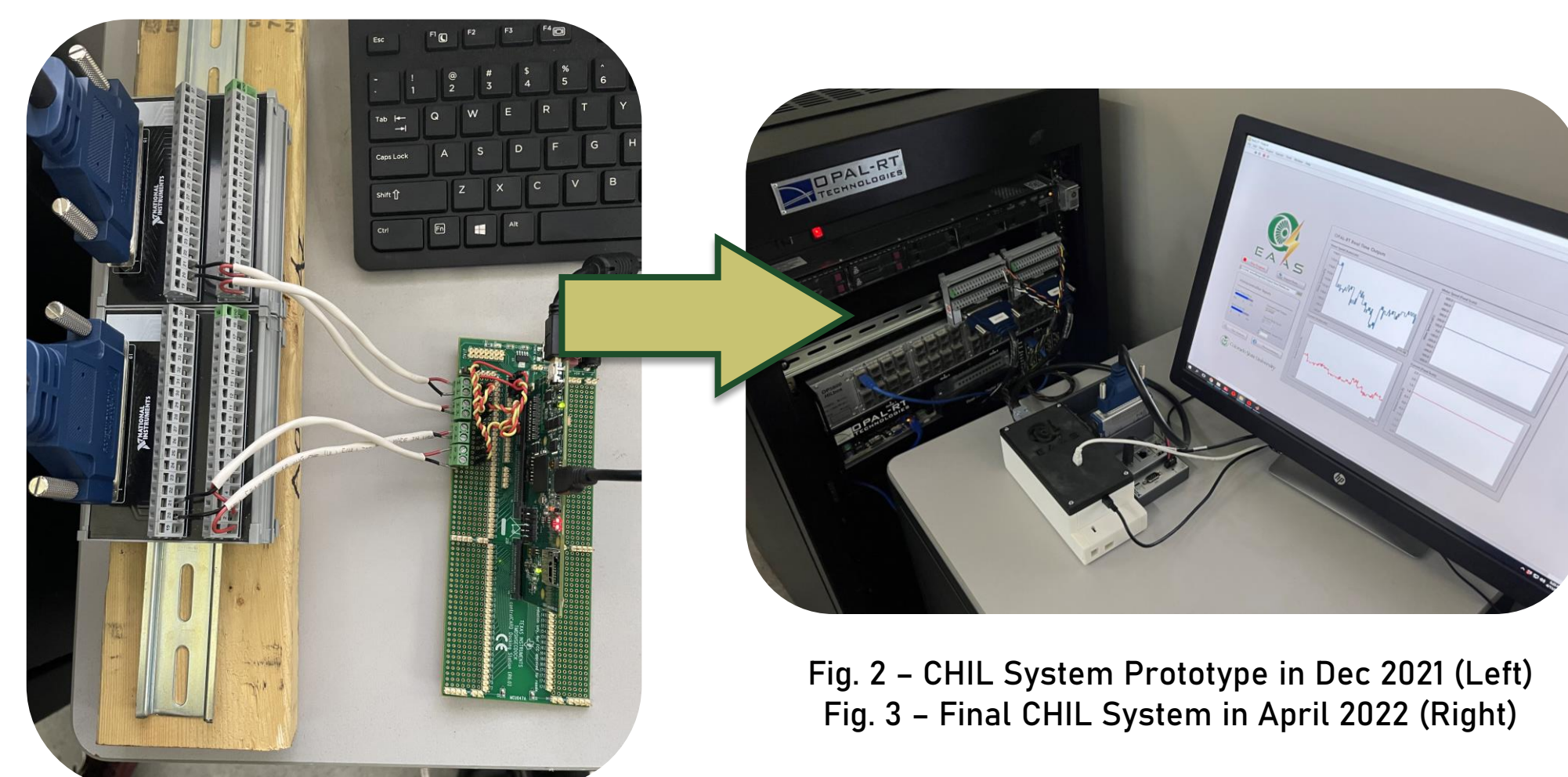


Fig. 2 - CHIL System Prototype in Dec 2021 (Left)  
Fig. 3 - Final CHIL System in April 2022 (Right)

## Required/Acquired Skills

- ➔ Embedded Systems/Control Algorithms in C
- ➔ MATLAB/Simulink
- ➔ HIL Construction and Interfacing
- ➔ LabVIEW GUI Design
- ➔ System Modeling Using MBSE Practices
- ➔ Defining/Testing GPIO Interfaces
- ➔ 3D Printing

## Software HIL Architecture

### Inputs to OPAL-RT (0-3 V)

- ➔ Duty Cycle [0 to 100% +/- 3%]
- ➔ Load Torque [-0.2 Nm - 0.2 Nm +/- 3%]

### Outputs from OPAL-RT (0-3.3 V @ 20 mA)

- ➔ Motor Speed [-600 to 600 rad/s +/- 3%]
- ➔ Armature Current [-2.5 to 2.5 A +/- 3%]

### Software Elements

- ➔  $\mu$ Controller Code, OPAL-RT Model, LabVIEW GUI

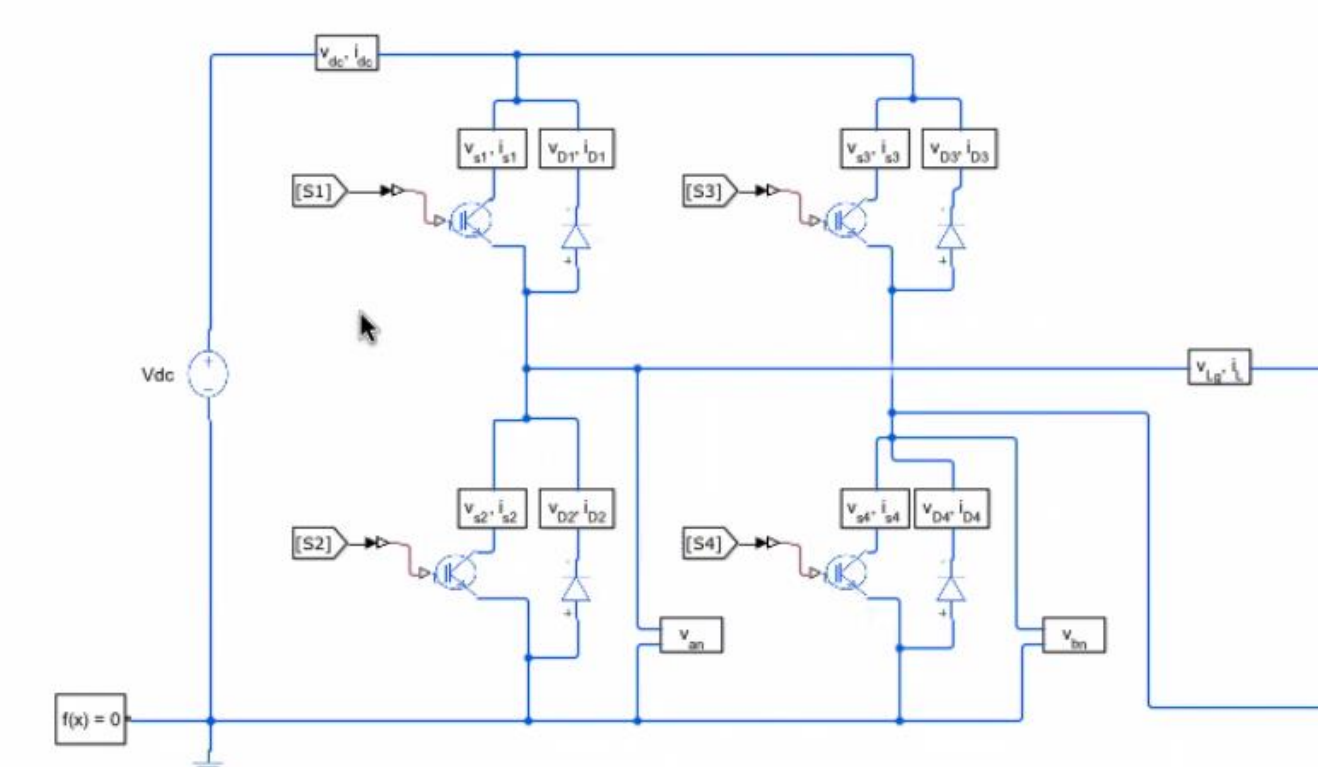
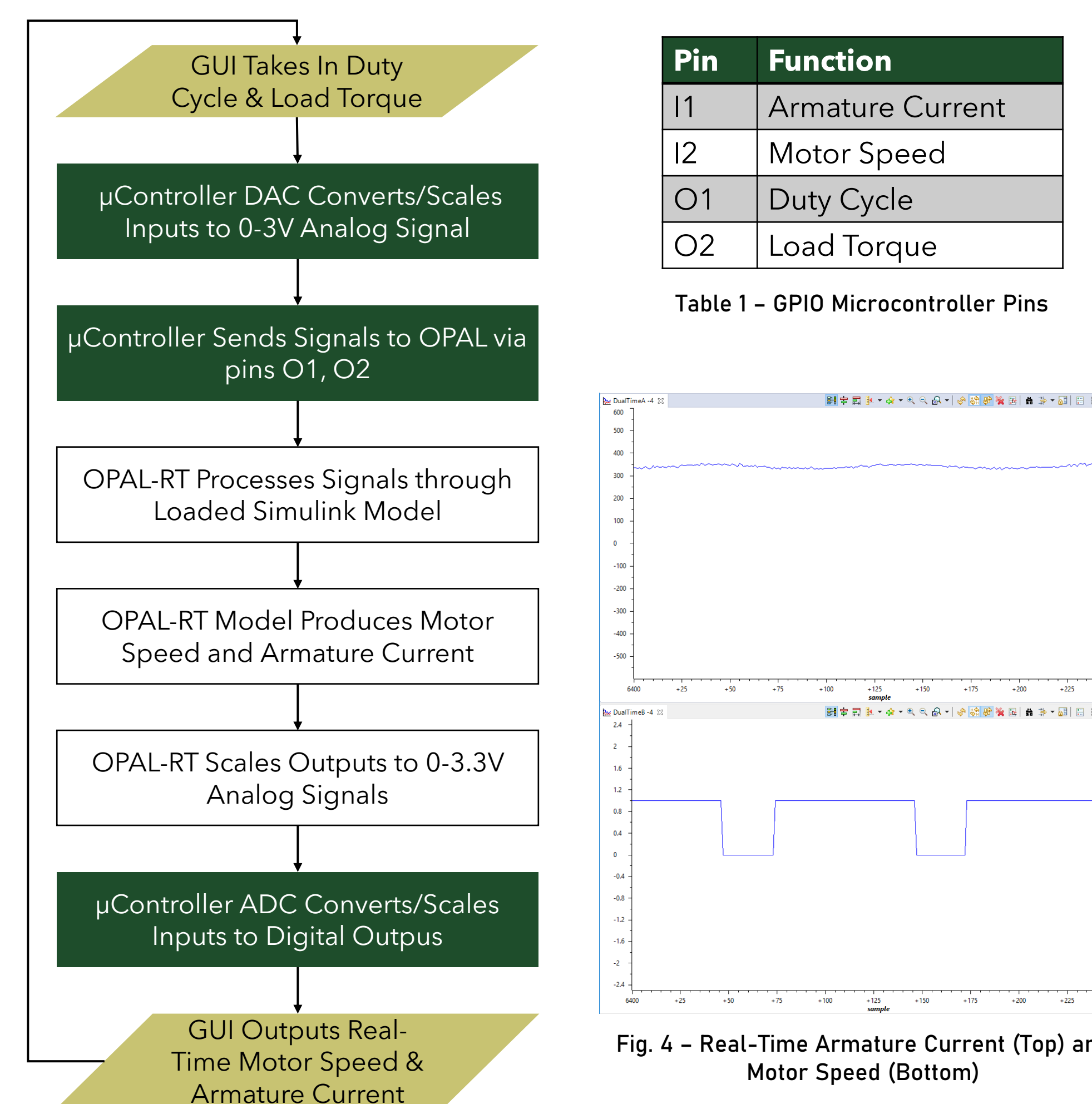


Fig. 5 - Simulink DC Machine Model

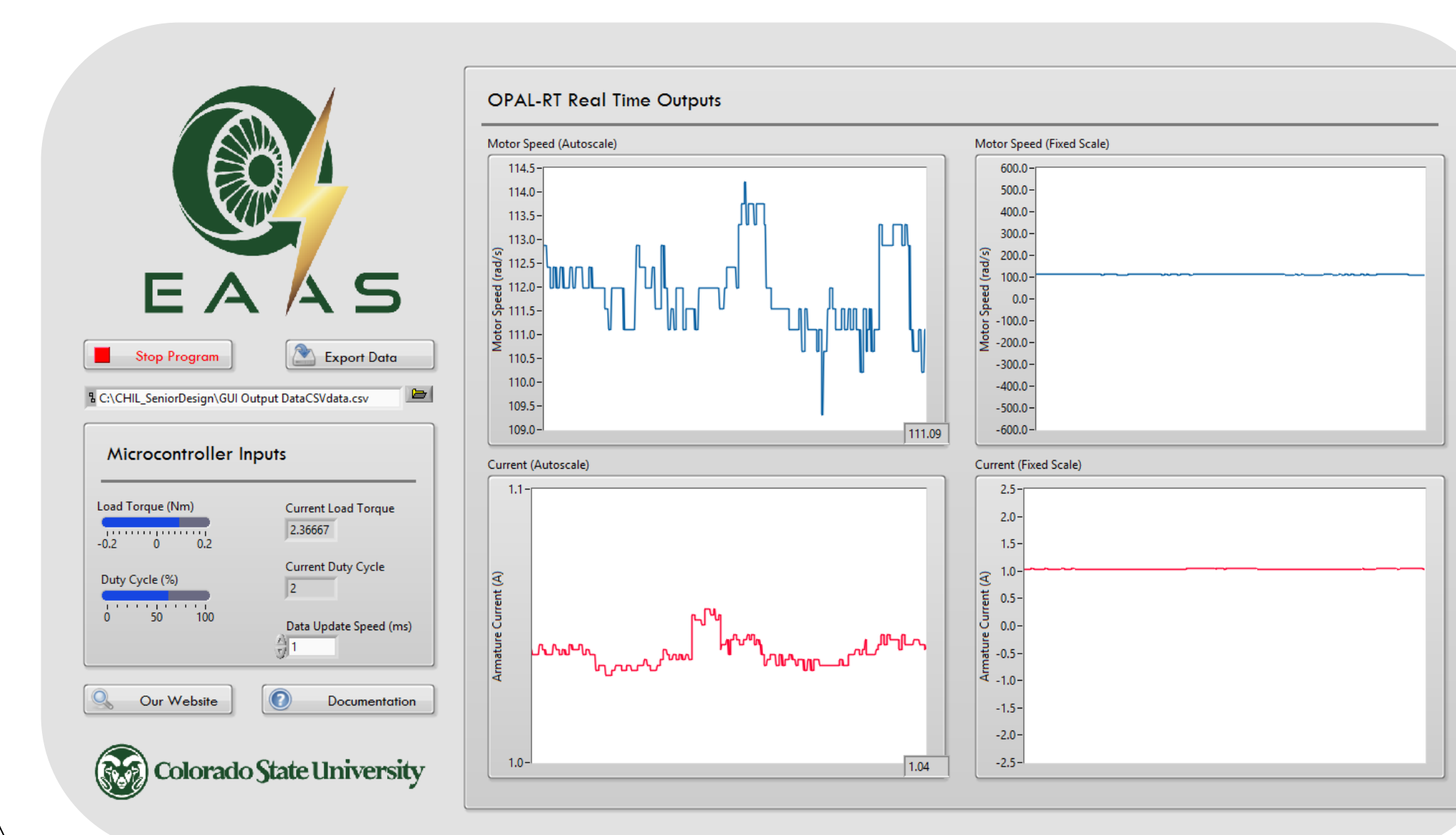


Fig. 6 - LabVIEW-Based CHIL GUI

## Model-Based Systems Engineering

- ➔ Team followed the MBSE process to create a verifiable and easily upgradable system
- ➔ Defined a set of 25 functional/non-functional requirements according to INCOSE standard
- ➔ Modeled various viewpoints of the system using Use Case Diagrams, Sequence Diagrams, & Internal Block Diagrams in Cameo Systems Modeler
- ➔ Used Cameo Systems Modeler as central repository of system design information, accelerating project completion

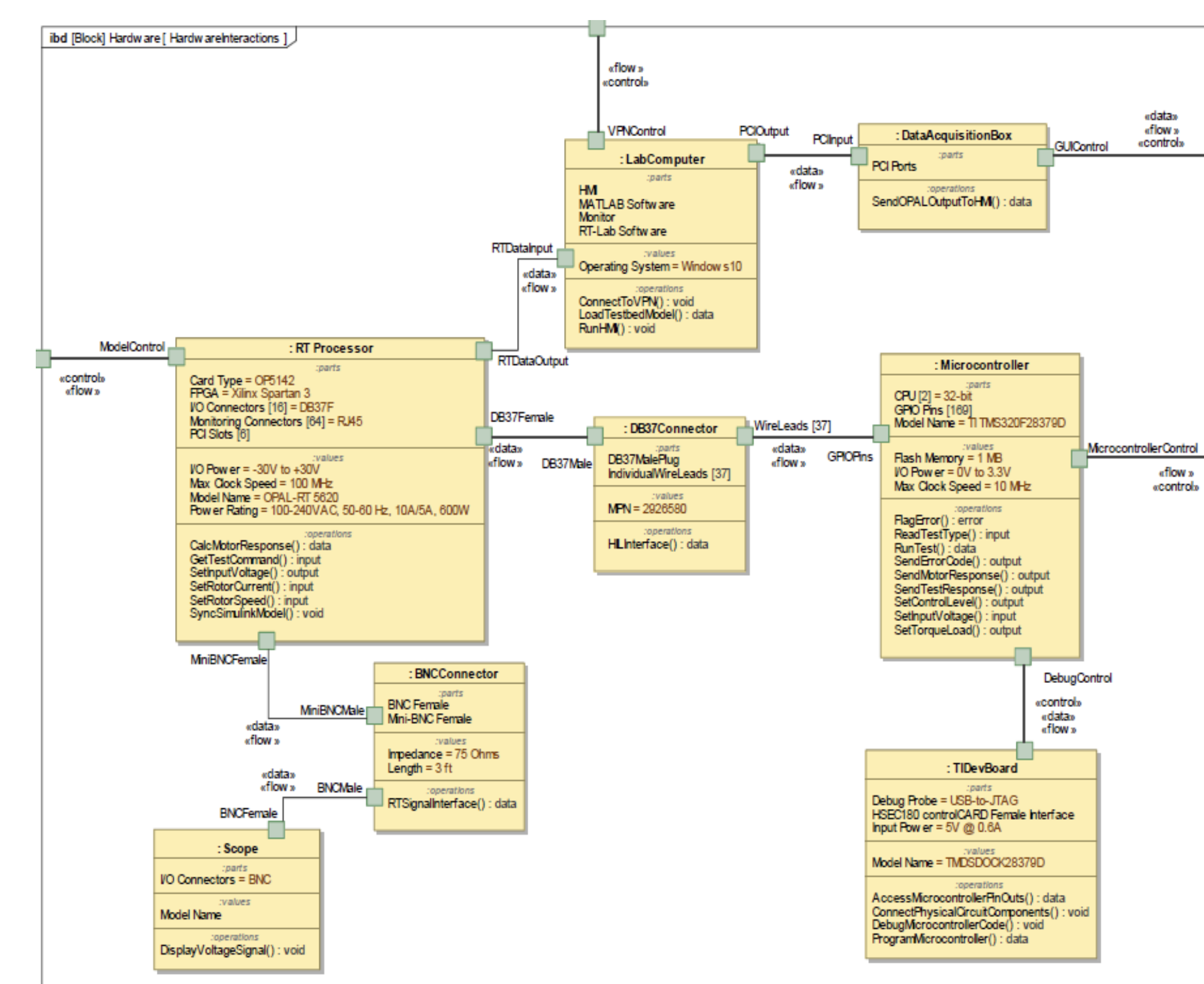


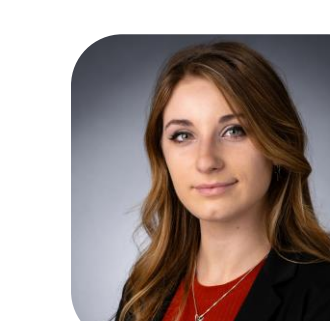
Fig. 7 - Physical Hardware Interface Diagram

## Documentation

- ➔ HTML Export of Code Commentary
- ➔ TI-OPAL Interface Definition
- ➔ Systems Cameo Model
- ➔ System Pinout Schematic
- ➔ Public GitHub Repository
- ➔ Team Website



## Team



**Kori Eliaz**  
B.S. Electrical Engineering  
Aerospace Concentration  
Team Role: Project Manager



**Jake Dorsett**  
B.S. Electrical Engineering  
Team Role: Hardware Lead



**Dylan Gaub**  
B.S. Electrical Engineering  
Minor in Computer Science  
Team Role: Software Lead

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