Project Plan | Emulation of Aerospace Actuation Systems

A Real-Time Controller Hardware-in-the-Loop Platform for Emulation of Aerospace Actuation Systems

Senior Design Students

Kori Eliaz | Electrical Engineering
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Jake Dorsett | Electrical Engineering

Additional Team Members

Ethan Schultz | Electrical Engineering, Undergraduate Team Member
Claudio Lima | Electrical Engineering, Graduate Team Member

Advisors

Project Advisor: Dr. James Cale
Lab Advisor: Chris Lute
EiR/Woodward Advisor: Matt Heath

Customers

Industry: Woodward, Inc.
Academia: CSU Systems Engineering Department

Summary

The Emulation of Aerospace Actuation Systems Project is an effort funded by Woodward, Inc. to validate an electrical drive alternative to replace the pneumatically/hydraulically operated Thrust Reverser Actuation Systems (TRAS) currently deployed on commercial and military aircraft. This project will interface a TI TMS320F28379D microcontroller with an OPAL-RT real-time processor to emulate several electrically driven aerospace actuation scenarios using a controller hardware-in-the-loop (CHIL) platform. Team members will program both the TI board and the OPAL-RT system in C to read/write synchronized digital and analog signals that reflect the behavior of real mechanical motors and drive systems located in a physical testbed at the Aerospace System Emulation and Test (ASET) Lab at the CSU Powerhouse. The team will also design a printed circuit board and wiring harness to facilitate seamless interaction between the TI board and the OPAL-RT system. Finally, the team will produce a detailed system model of the code and associated hardware using the principles of Model Based Systems Engineering in Cameo Systems Modeler. The overall product to Woodward, Inc. is a well-documented system model and thoroughly tested code package that can safely interface with the ASET testbed for the next phase of project validation.

Why is This Project Important?

The trend towards More Electric Aircraft (MEA) is expected to revolutionize the aerospace industry in the coming years, with promises of reduced weight, maintenance, and additional data analytics for real-time system prognostics compared to traditional drive systems. To verify these claims without incurring tremendous R&D costs to the customer, a CHIL platform allows for emulation of an expensive physical system using inexpensive software to test the behavior and benefits of an electromechanical TRAS.

Date	Comments	Version	Approved By
9/13/2021	Initial release	1.0	Jim Cale, Matt Heath

Problem Statement

The quest for more electric aircraft (MEA) is an industry-wide initiative to optimize aircraft performance, reduce operation and maintenance costs, and reduce the environmentally damaging effects of operating aircraft. Specifically, this concept prompts the redesign of all non-propulsive systems to use electric power rather than hydraulic or pneumatic techniques. Targeted pursuit of MEA technologies is a critical step towards improvements in aircraft fuel consumption, reliability, and carbon neutrality.

Current Thrust Reverser Actuation Systems (TRAS) employ mechanically focused solutions using hydraulic or pneumatic actuation to control an aircraft. Over the last two years, Woodward, Inc. and the CSU Systems Engineering Department have partnered to identify and validate an electric TRAS system at the ASET Lab. EM-TRAS systems are also currently in development at major aerospace contenders such as Honeywell Aerospace and Collins Aerospace; Woodward, Inc. has been at the forefront of mechanical TRAS systems for decades and is actively participating in the race to establish the most effective solution to implement this revolutionary concept.

The inherently large scope of any aerospace project in terms of cost and physical real-estate demands a solution that can validate control and analytics algorithms for electrical drive alternatives without having access to full-sized aircraft hardware. Through a partnership between Woodward, Inc. and the Systems Engineering Department at Colorado State University, a representative hardware testbed was designed and is now being constructed by members of the ASET Lab. The power-converter (voltage/current source) for this testbed employs a TI TMS320F28379D microcontroller. To complement the hardware testbed, there is a need to develop a platform to enable rapid firmware development for the power-converter by evaluating the hardware specific (I/O) functions of the microcontroller without endangering the physical testbed itself. By using controller-hardware-in-the-loop (CHIL) to emulate the physical system that would provide inputs to the microcontroller, team members can accomplish the following goals without risk to the physical testbed:

- Enact test failures and develop algorithms to mitigate and prevent these failures from occurring in real time
- Rapidly unit-test newly developed firmware
- Enable automated test sweeps to ensure that changes to the microcontroller code do not negatively impact code that was already validated

This project team will design the microcontroller code to interface with an OPAL-RT real time processor that is running a simplified model of a DC machine through a CHIL platform. Code will be written in C and will include various functions and unit tests that trigger specific failure modes in the model. These failure modes will be documented, and algorithms will be written to mitigate and prevent these failure modes from resulting in fatal errors to the overall system. By designing and rigorously testing this code on an internal model rather than on the physical testbed located in the ASET Lab, the team can ensure the longevity of the mechanical parts used to construct the testbed and can design solutions for the overall EM-TRAS system to operate nominally despite potential failure modes that may occur. These failure modes are addressed in a proprietary document and will be tracked accordingly during code development to ensure that all customer requirements are being met.

Objectives

Primary Objectives:

Note: These objectives are directly required by the customer for the successful completion of this project:

- Determine the analog and digital I/O requirements for the microcontroller and OPAL-RT
- Design, build, and test signal conditioning boards and wiring harnesses needed to interface the microcontroller and the OPAL-RT system as required

- Develop C code for running a closed-loop CHIL experiment, where the OPAL-RT executes a real-time DC machine system model
- Run the closed-loop CHIL experiment with set failure modes as described in the proprietary document and collect measurement information
- Document the design steps and experimental results in a test report to be delivered to the customer
- Include system requirements flow-through and design information on the CHIL platform in the existing Cameo repository for the testbed

Secondary Objectives:
Note: these objectives are not directly required by the customer, but are being pursued by the senior design team to increase readability and overall functionality of the end product:

- Design a Graphical User Interface (GUI) that abides by the ISA101 HMI Standard to represent the current state of the testbed during all tests as well as error codes that are flagged during these tests and the system's real-time response to mitigate these errors
- Create a script to parse through the microcontroller code and establish code coverage of all conditional branches to ensure that all code is being thoroughly tested and verified before official hand-off to the customer for interface with the physical testbed
- Run a documentation tool (e.g. Doxygen) on the finished code to extract an HTML report of all code documentation and increase readability/ease of understanding for the customer upon official hand-off at the end of the project period

Background Research

The key motivation of this senior design project is to provide the aerospace industry with more electric aircraft. More Electric Aircraft (MEA) is a concept in the aerospace industry that is driven by demands such as optimizing aircraft performance, decreasing operating and maintenance costs while also reducing fuel consumption and gas emissions (Yitao Liu et. al., 2018). This project is focused on electrifying secondary energy sources in aircraft, specifically, the currently hydraulic-driven thrust reversers on aircraft nacelle. Currently there are a few companies working on replacing the hydraulic driven thrust reversers with electric driven ones such as Honeywell and Collins Aerospace. While there are companies that have been working with similar goals, Woodward, Inc. has a long-standing position in the aerospace industry creating Thrust Reverser Actuation Systems dating back to the 1960s. With the expertise of Woodward, Inc. in combination with our senior design team, we aim to produce state of the art solutions to push the aerospace industry one step further towards fully electric aircraft.

This senior design project is a continuation project in collaboration with Woodward, Inc., with the goal of creating a testbed for validating an Electromechanical Thrust Reverser Actuation System (EM-TRAS). Previous work on this project yielded a physical testbed for emulating the EM-TRAS system, but before this testbed can be used to perform simulations, we will work on creating a validation system using a real time simulator and microcontroller to perform a Controller-Hardware-In-the-Loop (CHIL) experiment.

Final Design Info and Design Constraints

Final Design Info:
Note: The below items are intentionally positioned at a high level to protect the proprietary nature of this project.
The final product handed off to Woodward, Inc. and the ASET Lab shall include:

- Thoroughly documented and version-controlled code that cleanly executes test cases of customer-demanded situations commonly imposed on a TRAS system organized as independent functions with corresponding error codes and appropriate system responses. This code shall interface specifically with the basic DC machine model provided by Dr. Cale to demonstrate the effective

nature of a CHIL system using the OPAL-RT machine and TI microcontroller prescribed to the team and iterated in the Design Constraints table below.

- Well-defined system requirements and relevant system diagrams located in the pre-existing Cameo repository, including but not limited to:
    - Sequence diagram showing the timing relationships between the OPAL-RT and the TI microcontroller I/O signals
    - Use case diagrams showing the relationships between the hardware components themselves and the relationships between the hardware and the human user via a GUI
    - Activity diagrams simulating the behavior of the code to run and verify functional unit tests
- Interactive GUI designed in LabView to interface with the code running on the TI microcontroller that allows the user to fully understand what test case scenario is being run and what the system's real-time response is expected to be. This GUI shall currently reflect the behavior of the model on the OPAL-RT and shall also be designed to be compatible with the physical testbed
- Signal conditioning board presented as a PCB and an accompanying harness to interface between the OPAL-RT and TI microcontroller, as required

Design Constraints:

OPAL 5600 RT Machine:	TMS320F28379D Microcontroller:

• I/O: -30V to 30V
• OPAL 5620 8 I/O Flat Carrier:
  o output: +/- 12VDC @ 1.2A (mezzanine A/B)
  o output: +/- 18VDC @ 0.8A (mezzanine A/B)
  o input: +/- 12VDC @ 6A; +/- 5VDC @ 3A
• OPAL 5142 Digital I/O: 3.3V
• Onboard XILINX Spartan 3A FPGA: 3.3V (LVTTL)
• Limited documentation/support
• Number of cores determines the maximum number of nodes that can be modeled, in turn setting the maximum clock speed (to be determined)
	• 3.3V I/O design
	• -0.3V min to 4.6V max
	• -20mA to 20mA
	• 50 kHz synchronization rate
	• Requires code written in C (no object-oriented functionality)
	• Requires code to be written in the Code Composer Studio IDE provided by TI
	• Limited documentation

Budget Justification

The team was awarded $600 for the academic year ($200 per senior design team member). It is not expected that this team will require more than the allotted funds to complete the project considering that most of the proposed work is software-based and almost all hardware has already been acquired by the ASET Lab. The CSU Systems Engineering Department has already ordered and received five TI TMS320F28379D microcontrollers for redundancy and for ease of access by all members of the project team. The OPAL-RT machine has also been acquired by the ASET Lab. The team's project advisor has requested that the budget allows for the purchase of one more development board to be used with the TI microcontrollers so the graduate student on the team is available to support the project as needed.

Justifications for each component are provided in the table below. Expected purchase months are listed and will be updated more specifically along with the chosen vendor for each expense once the project reaches its development phase. Although it is unlikely that additional funds will be required, in the case that they are, an official proposal will be submitted to the Woodward, Inc. customer explaining how these funds are necessary to complete the assigned task. Kori will be responsible for drafting and pitching all funding proposals.

Expense	Fulfills Critical Path? (Y/N)	Amount + Shipping	Quantity	Status	Purchase Date	Justification
TI Dev Board	N	$200.00 + $50 S/H	1	To Be Ordered	Sep 2021	An additional Dev Board will allow for an additional graduate student on the project team to contribute to code implementation and verification, leading to more rapid troubleshooting and accelerated project completion. ***Note:*** *This is an optional purchase that will benefit the team but is not required to complete the project.*
PCB Fabrication	Y	$35.00 + $10 S/H	2	To Be Ordered	Oct 2021	PCB designed to interface between OPAL-RT and TI microcontroller required for validation testing of microcontroller code. Budgeting for a backup PCB in the case of redesign or manufacturer error.
Molex Crimping Tool	Y	$40.00 + $10 S/H	1	To Be Ordered	Oct 2021	Specific crimping tool required for the connectors purchased to construct the wiring harness to interface between the OPAL-RT to PCB and then from PCB to TI microcontroller. This will ensure that the wires in the harness are fastened properly into the connector and decreases likelihood for part failure.
Connectors/ Wires	Y	$100.00	1	To Be Ordered	Oct 2021	Various connectors and wires are required to construct the wiring harness to interface between the OPAL-RT and the PCB and then from the PCB to the TI microcontroller. These will be assessed in more detail once the project enters the hardware development phase.
E-Days Presentation Materials	Y	$50.00	1	To Be Ordered	Mar 2022	Posters, 3D printed pieces, and stickers/business cards will need to be produced for our E-Days Showcase in the Spring Semester.

Starting Balance	$600.00	Starting Balance	$600.00
Total Spent on Required Purchases ONLY	- $290.00	**Total Spent on ALL Purchases**	- $540.00
Total Remaining after Required Purchases ONLY	**$310.00**	**Total Remaining after ALL Purchases**	**$60.00**

FMEA Table

Note: The below failure modes are initial considerations. This list will be expanded once the project enters development phase.

Component	Purpose	Potential Failure Mode	Potential Failure Effect	SEV	Potential Causes	OCC	Current Process Controls	DET	RPN	Action Recommended
Executable Unit Tests	Tests are intended to simulate all possible cases of mechanical and electrical failure in EM-TRAS testbed and apply the appropriate mitigation response	Missing test case or thrown error code does not match test case	Inaccurate data, resulting in software needing to be revisited. If not addressed, could result in testbed mechanical damage, and large cost implications to customer	8	Improper or rushed programming and missing safety net	7	Test cases are mapped directly to customer requirements	10	560	The validation of project requirements to be tracked through a systems model in Cameo. Review code status with Woodward POC on a monthly basis to ensure consistency with evolving customer requirements
GUI	GUI is implemented to show the user which portions of the testbed are being tested, along with the system's response and potential failures	Properties of the GUI do not function properly	User is given inaccurate test results	6	Software is not properly integrated with GUI	3	GUI is to be reviewed alongside software reults to ensure it is representing accurate data	1	18	
Documentation	Provide the customer with a detailed explaination of the code and GUI functionality, specifically a detailed outline of all test cases and their corresponding mitigation plan	Error cases are not sufficiently documented	End user does not understand an error code, leading to confusion and frustration	4	Our team does not document our code well due to time constraints or lack of organization	3	Pair programming and HTML export of all documentation (Doxygen)	1	12	
Microcontroller Outputs	The microcontroller outputs serve as fixed voltage/current inputs to the testbed to simulate an error case and the appropriate mitigation response	The torque/power/ voltage limitations on hardware in the testbed are improperly defined in the microcontroller code	When connected to the physical testbed, hardware can be damaged	10	Spec sheets were read incorrectly and/or we did not consult a secondary source to verify their accuracy	3	Work will be done in person at the Powerhouse, so physical components of the testbed will be cross checked with the definitions in the microcontroller code	7	210	Host monthly design reviews with Woodward POC, and dedicate a portion of time specifically to review these specific parameters. Popup in the GUI warning of potential mechanical failure
Wiring Harness	The OPAL-RT needs to be connected to the TI Microcontroller to perform CHIL	TI board outputs are not properly connected to their appropriate input on OPAL-RT	OPAL-RT or TI board could be damaged	8	In producing the wiring harness, the connectors were not properly labeled	5	Wiring harness will be labeled with the locations of appropriate connections	1	40	

Risk Analysis Table

Note: The below risks are initial considerations. This list will be expanded once the project enters development phase.

#	Risk Event	Probability	Impact (hrs)	Score (hrs)	Effect	Risk Mitigation Plan	Responsible Person(s)
1	Miscalculation of voltage and current relationships between OPAL-RT and microcontroller	0.3	100	30	TI microcontroller or OPAL-RT are damaged as a result	Careful steps will be taken to ensure that correct relationships are established and verified with Chris Lute.	Jake
2	PCB does not function due to manufacturer error (improper plating)	0.25	30	7.5	Cannot use PCB and a new one needs to be ordered. Time delay and potential additional cost	PCBs will be purchased from a reliable vendor that has a positive relationship with the CSU Systems Engineering department.	Kori
3	Error cases are inadequately tested	0.75	100	75	The program does not successfully fulfill customer requirements	Create a script that tracks the percent of executed conditional branches run through. In doing so, obtaining 100% will ensure that all possible combinations have been tested	Jake, Dylan
4	Bad solder joints on PCB harness	0.2	10	2	PCB does not work, leading to additional time spent diagnosing issues	Assign soldering tasks to the most experienced team member	Dylan
5	Staff illness	0.1	18	1.8	Team is down in manpower and tasks take longer to complete	Non-sick team members make availability in their weekly schedule to cover time-sensitive tasks assigned to sick team member. Ensure project schedule and Trello are kept up to date with tasks/deadlines and time requirements	All
6	Unintentional disclosure of confidential components of the project	0.3	10	3	Proprietary information is given to the public and patent timeframes are tightened, severely affecting customer's timeline	Have all team members sign an NDA. Reiterate which portions of the project are proprietary at weekly meetings.	Kori
		Total Risk:	**119.3**				

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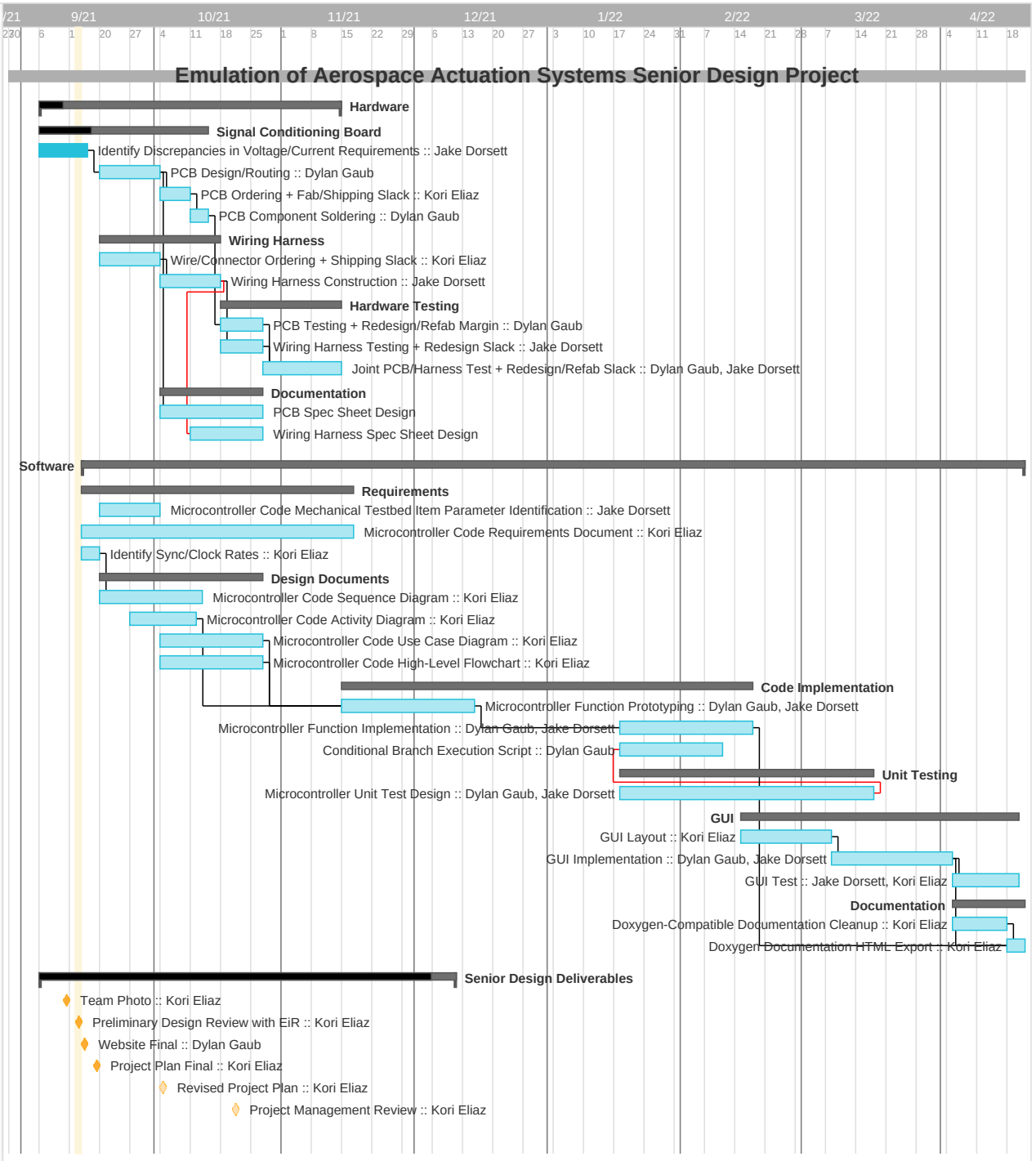
Emulation of Aerospace Actuatio...	start	end	19%
Hardware	**09/06/21**	**11/12/21**	**8%**
Signal Conditioning Board	**09/06/21**	**10/13/21**	**31%**
Identify Discrepancies in Voltage/Current...	09/06	09/15	100%
PCB Design/Routing	09/20	10/01	0%
PCB Ordering + Fab/Shipping Slack	10/04	10/08	0%
PCB Component Soldering	10/11	10/13	0%
Wiring Harness	**09/20/21**	**10/15/21**	**0%**
Wire/Connector Ordering + Shipping Sla...	09/20	10/01	0%
Wiring Harness Construction	10/04	10/15	0%
Hardware Testing	**10/18/21**	**11/12/21**	**0%**
PCB Testing + Redesign/Refab Margin	10/18	10/26	0%
Wiring Harness Testing + Redesign Slack	10/18	10/26	0%
Joint PCB/Harness Test + Redesign/Ref...	10/27	11/12	0%
Documentation	**10/04/21**	**10/26/21**	**0%**
PCB Spec Sheet Design	10/04	10/26	0%
Wiring Harness Spec Sheet Design	10/11	10/26	0%
Software	**09/15/21**	**04/20/22**	**0%**
Requirements	**09/15/21**	**11/16/21**	**0%**
Microcontroller Code Mechanical Testbe...	09/20	10/01	0%
Microcontroller Code Requirements Doc...	09/15	11/16	0%
Identify Sync/Clock Rates	09/15	09/17	0%
Design Documents	**09/20/21**	**10/26/21**	**0%**
Microcontroller Code Sequence Diagram	09/20	10/12	0%
Microcontroller Code Activity Diagram	09/27	10/11	0%
Microcontroller Code Use Case Diagram	10/04	10/26	0%
Microcontroller Code High-Level Flowcha...	10/04	10/26	0%
Code Implementation	**11/15/21**	**02/16/22**	**0%**
Microcontroller Function Prototyping	11/15	12/14	0%
Microcontroller Function Implementation	01/18	02/16	0%
Conditional Branch Execution Script	01/18	02/09	0%
Unit Testing	**01/18/22**	**03/16/22**	**0%**
Microcontroller Unit Test Design	01/18	03/16	0%
GUI	**02/15/22**	**04/19/22**	**0%**
GUI Layout	02/15	03/07	0%
GUI Implementation	03/08	04/04	0%
GUI Test	04/05	04/19	0%
Documentation	**04/05/22**	**04/20/22**	**0%**
Doxygen-Compatible Documentation Cl...	04/05	04/15	0%
Doxygen Documentation HTML Export	04/18	04/20	0%
Senior Design Deliverables	**09/06/21**	**12/09/21**	**94%**
Team Photo	09/10	09/10	100%
Preliminary Design Review with EiR	09/14	09/14	100%
Website Final	09/15	09/15	100%
Project Plan Final	09/17	09/17	100%
Revised Project Plan	10/04	10/04	0%
Project Management Review	10/20	10/20	0%



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DTVC Document	10/29	10/29	0%
Mid Project Review w/ EiR	12/03	12/03	0%
Oral Presentations	12/09	12/09	0%
Project Plan	**09/06/21**	**09/17/21**	**100%**
Project Plan Rough Draft	09/06	09/13	100%
Project Plan - Summary	09/11	09/13	100%
Project Plan - Why is This Project Import...	09/11	09/13	100%
Project Plan - Problem Statement	09/11	09/13	100%
Project Plan - Project Schedule	09/06	09/13	100%
Project Plan - Objectives	09/11	09/13	100%
Project Plan - Background Research/Mult...	09/06	09/13	100%
Project Plan - Final Design Info and Desi...	09/13	09/17	100%
Project Plan - FMEA Table	09/11	09/13	100%
Project Plan - Risk Analysis Table	09/11	09/13	100%
Project Plan - Budget Justification	09/11	09/13	100%
Website	**09/06/21**	**09/13/21**	**100%**
Website Rough Draft	09/06	09/13	100%
Website - Kori's Headshot, Resume, Lin...	09/06	09/07	100%
Website - Jake's Headshot, Resume, Lin...	09/06	09/06	100%
Website - Dylan's Headshot, Resume, Li...	09/06	09/07	100%
Website - Main Page	09/06	09/08	100%
Website - Timeline and Deliverables	09/06	09/13	100%
Website - Pictures and Demos	09/06	09/08	100%
Website - Documents	09/06	09/08	100%
Website - Acknowledgements	09/06	09/10	100%
Website - Required Graphics/Links	09/06	09/08	100%
Website - Formatting and Text Incorporat...	09/06	09/08	100%
Website - Update Abstract	09/12	09/13	100%
Administrative	**09/13/21**	**10/08/21**	**50%**
Proof Website with Dr. Cale	09/13	09/13	100%
Proof Project Plan with Dr. Cale	09/13	09/13	100%
Lab Walkthrough and Safety Briefing	09/13	09/13	100%
Cameo Model Weekly Update	09/17	09/17	0%
Website Biweekly Update	09/28	09/28	0%
FMEA/Risk Table Monthly Update	10/08	10/08	0%
Miscellaneous	**08/30/21**	**09/21/21**	**46%**