Dimitri Gerin

Software and Application Engineer

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Up-to-date version of CV is available at
https://dgerin.github.io/cv

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Dimitri Gerin

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(Personal github) dgerin

As a Software Engineer, I have been working on a wide range of projects, for different companies. I always try to work on the most possible innovative projects, that's why I have mostly been working for startup companines. Because I like to interact with hardware, I always try to stick with the low level aspects of each project, from the design of rtl blocks to the software side, even if I decided to fully switch to software for the last few years. I implemented different algorithms, on different kind of architectures like well known Xilins FPGA's, but more recently on the emergent Processing In Memory (PIM) devices, developed by UPMEM. Over the years, I developed a deep understanding of theses different algorithm, architectures and systems. I'm also a crypto-enthusiastic person. I'm fascinated by the blockchain technology in general, and even I am not actively working in this field, I always try to keep informed about the evolution of the main technologies like bitcoin and ethereum.

parrallel programming	●●●●	performances optimization	●●●●	Linux device driver	●●●○	Deep Learning	●●○○	RTL Design	●●●○	Quantization	●●●○
C	●●●●	C++	●●●●	Python	●●●●	VHDL	●●●●				
PIM (Processing in Memory)	●●●●	Linux Kernel	●●●○	x86	●●●○	PCI express	●●●○	DDR Memory	●●●●	Xilinx FPGA	●●●●
PyTorch	●●●●	Tensorflow	●●●○	LLVM	●○○○						
linux perf	●●●●	qemu	●●●○	intel vtune	●●●○	docker	●●○○	vivado	●●●○		

Professional Experience

2021 - 2023

UPMEM, Paris/Grenoble

Software and Application Engineer

One part of my job is to develop applications on UPMEM PIM devices to demonstrate the interest of PIM technology in term of performance and energy efficiency. I also work on the development, maintenance and support of the UPMEM PIM SDK, which is a set of tools and libraries to develop applications on UPMEM PIM devices. I am also working on the improvement of the UPMEM PIM device driver, which is a Linux kernel module used to communicate with PIM devices.

PIM | Linux Device Driver | Parallel Programming | PCI express | Performance Optimization | Deep Learning

Noticable Applications/Projects

genomic compression

Implementation of a a novel genomique technique of DNA comprehension, based on blool filter, in colaboration with INRIA/IRISA.

SparseP

https://github.com/upmem/SparseP/tree/upmem_internal

Obtimization of original SparseP implementation from ETH Zurich. SparseP is a PIM implementation of Sparse Matrix/Vector multiplication (https://arxiv.org/abs/2201.05072)

PIM Embedding

https://github.com/upmem/PIM-Embedding-Lookup/tree/multicol

PIM implementation of Pytorch EmbeddingBag

2018 - 2021

VSORA, Meudon-La-Forêt

Software Engineer

I mainly focussed on the specification and the implementation of the VSORA Deep Learning Inference library, a library that implements various DL Layers on VSORA DSP Architecture. I also ported various Deep Learning models on VSORA DSP Architecture, and developed a Quantization Aware retraining flow to improve models precision with Low-Precision quantization. One other part of my job was to maintain the release and CI pipeline.

DeepLearning C++ SystemC

2017 - 2018

THALES, Gennevilliers

FPGA Engineer

As subcontractor, I participaped to the development and validation of the physical layer of FO3D, a new military waveform developed by Thales. I focussed myself on the design of the FPGA part of the TX and RX chains. For this, I developed different RTL blocks that implements signal processing functions.

FPGA Telecom Signal Processing

Involved Projects

FO3D

FPGA Implementation of the physical layer of the FO3D waveform

2014 - 2017

SIMPULSE, Palaiseau

FPGA / Embedded System Engineer

I participated to the development of the FPGA platform. I developed different RTL blocks for different purposes like telecom signal processing functions, device interfaces and CPU co-processors.

RTL Design FPGA Telecom SoC HW/SW Codesign

Noticable Projects

European Project

In colaboration with Nokia Bell Labs, implementing an OpenAIR LTE If4p5 Interface, into FPGA, with Simpulse DSP IP

2014

CEA LETI, Grenoble

Intern

Research in MIMO algorithm for advanced (5G,LTE-Advance).

Matlab OFDM 5G

2013

UNLV, Las Vegas

Intern

Participating to developpment of an interactive motion based traffic simulator.

C++

Education

2012 - 2014

PHELMA, Grenoble-INP (ex ENSERG), Grenoble

Engineer's Degree in signal processing, electrical engineering and computer science

Signal Processing Electrical Engineering Computer Science

2008 - 2010

CNAM, Paris

Technology degree (DUT GEII), Graduated as Valedictorian

Electrical Engineering

2005 - 2008

ETPLM, Grenoble

High school degree (BAC STI GE), with hounours (mention très bien)

Certifications

2021

Machine Learning (Coursera/Standford, Andrew Ng)

Logistic Regression | Neural Networks | Recommenders

2022

Solana Blockchain Developer Bootcamp with Rust + JavaScript (Udemy)

SmartContract | Rust | Javascript | Solana

2018

Xilinix FPGA Certification (Xilinx Training Programm)

FPGA | Vivado | VHDL