DOM-Cal XML Users' Guide
Version 7.4

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1 Introduction

This document describes the result XML file produced by the DOM-resident calibration software DOM-Cal. The intent is to allow a user to develop a reader which will calibrate DOM waveforms, allowing transformation of both raw and pedestal-subtracted waveforms into physical units such as voltage, time, and charge.

This document does not describe the means of calibration. More information about the calibration methods is available in the DOM-Cal Users' Guide, available as part of the dom-cal project.

2 XML File Description

The XML elements are presented below in the order in which they appear in the output file.

- <domcal version=*version*>
  The root element of the XML file contains the version of DOM-Cal which produced it as an attribute. The version is a string of the format *N.N.N*, with each field denoting major, minor, and patch versions respectively. This version matches the release tag of the software.
  - <date>
    The date of the calibration, in DD-MM-YYYY format.
  - <time>
    The time of the calibration, in HH:MM:SS format. Note that the date/time are in GMT.
  - <domid>
    The DOM mainboard ID (hexadecimal).
  - <temperature format="Kelvin">
    The DOM temperature at calibration time, measured in K by the mainboard temperature sensor. This is 10-12K above the ambient temperature, unless the DOM has just been powered on. Note that in general, the calibration is only valid around this temperature.
  - <dac channel=*channel*>
    All mainboard DAC settings (0-15) are recorded. **IMPORTANT:** in general, the calibration should only be considered valid for these DAC settings! In particular, the ATWD operational settings in DACs 1-3 and 5-7 must match any data to which this calibration is applied. The sampling speed in DACs 0 and 4 can be adjusted, however.
  - <adc channel=*channel*>
    All mainboard ADC values (0-23) are recorded.
  - <frontEndImpedance format="Ohms">
    The front-end impedance used for the calibration. The same value must be used in any charge calculations which depend on DOM-Cal results. See section 3 for more information.

– <discriminator id="spe">

The front-end SPE discriminator calibration. This calibration translates the SPE discriminator DAC setting (DAC 9) to the amplified charge (after the PMT) corresponding to that trigger level.

* <fit model="linear">
  - <param name="slope">
  - <param name="intercept">
  - <regression-coeff>

  A linear fit element describing the calibration results. There are a large number of these in the DOM-Cal output, all of this form. The fit element contains three sub-elements: the slope and intercept of the fit, along with the R^2 coefficient, all in floating-point format.
  This fit provides the following relation:

$$\text{charge trigger level (pC)} = m \cdot \text{DAC}[9] + b \ . \tag{1}$$

  Because this trigger level is relative to a given baseline determined by the FE (front end) bias voltage DAC (DAC 7), this calibration is only valid for a given setting of the bias voltage (recorded in the appropriate <dac> element).
  See the <pmtDiscCal> result for a refinement of this calibration.

– <discriminator id="mpe">

The front-end MPE discriminator calibration. This calibration translates the MPE discriminator DAC setting (DAC 8) to the amplified charge (after the PMT) corresponding to that trigger level.
Like the SPE discriminator calibration, a linear fit element describes the results, providing the following relation:

$$\text{charge trigger level (pC)} = m \cdot \text{DAC}[8] + b \ . \tag{2}$$

Because this trigger level is relative to a given baseline determined by the FE (front end) bias voltage DAC (DAC 7), this calibration is only valid for a given setting of the bias voltage (recorded in the appropriate <dac> element).

– <atwd id=*id* channel=*channel* bin=*bin*>

A series of 768 linear fits which calibrate the ATWDs. The attributes indicate the id (ATWD 0 or 1), the channel (0, 1, or 2), and the waveform bin (0-127) for which the fit it valid. The linear fit provides transformation from ATWD counts to voltage (Volts, after channel amplification):

$$\text{V}(\text{id}, \text{channel}, \text{bin}) = m \cdot \text{counts}(\text{id}, \text{channel}, \text{bin}) + b \ . \tag{3}$$

For example, to reconstruct a single waveform in ATWD 1, channel 0, the first step is to use the 128 fits with $id = 1$ and $channel = 0$ to reconstruct the voltage for each bin. **IMPORTANT:** the fits for each bin automatically calibrate out the pedestal pattern of the ATWD. The calibration should not be applied as described to pedestal-subtracted data. See section 3 for more information. Also

note that the bin number corresponds to the sample in the raw time-reversed ATWD waveform, so bin 127 is the earliest sample in time, and bin 0 is the latest.

Also note that there is currently no calibration available (or planned) for the y-axis of the analog multiplexer channels. The time axis can be treated just like any other ATWD channel.

– <fadc_baseline>

The FADC baseline calibration records the linear response of the FADC baseline (in ADC ticks) to the FADC reference DAC setting, DAC 10. There is also a smaller dependence of the FADC baseline on the front-end bias voltage, DAC 7, so this relationship should be considered valid for the DAC 7 value recorded above in the appropriate <dac> element.

$$\text{FADC baseline (ticks)} = m \cdot \text{DAC}[10] + b \ . \tag{4}$$

– <fadc_gain>

The FADC gain calibration element.

* <gain error=*error*>

  The gain element contains the FADC gain, including the intrinsic gain of the FADC as well as the channel amplifiers, as a floating-point number. The error reported as an attribute is the 1σ error on this mean gain measurement. Note that unlike the gain of the ATWD channels, this calibration element has units (V/tick).

– <fadc_delta_t>

The FADC time offset calibration.

* <delta_t error=*error*>

  The delta_t element contains the FADC time offset, in ns, from ATWD waveform start. The number reported is negative, as the FADC waveform starts earlier in time than the ATWD waveform. The error reported as an attribute is the 1σ error on this mean delta_t measurement. This calibration is valid only for the DOMApp FPGA (used in pDAQ), not the STF FPGA (used in testDAQ).

– <atwd_delta_t*id* = *id* >

The ATWD time offset calibration.

* <delta_t error=*error*>

  The delta_t element contains the ATWD time offset, in ns, resulting from slightly different delays in ATWD digitization start. The ATWD used in the transit time calibration will have an offset of zero, while the other delta_t element provides a small (a few nanoseconds) correction for the other ATWD. See section 3 for more information. The error reported as an attribute is the 1σ error on this mean delta_t measurement.

– <amplifier channel=*channel*>

The amplifier gain calibrations for the three ATWD signal channels (0, 1, and 2). The calibrations

are valid both for ATWD 0 and ATWD 1. The reconstructed waveforms from the ATWD bin fits need to be divided by the channel gain to get the PMT output voltage.

  * <gain error=*error*>
    The gain element contains the channel gain as a floating-point number. The gain is negative to reconstruct the waveform as positive-going. The error reported as an attribute is the 1σ error on this mean gain measurement.

- <atwdfreq atwd=*atwd*>
  The ATWD time calibrations for ATWD 0 and 1. This can be used to translate the ATWD waveform x-axis into time. Unlike other ATWD calibrations, the relation between DAC setting and sampling speed is not quite linear, but is nicely described quadratically with the following fit element:

  * <fit model="quadratic">
    · <param name="c0">
    · <param name="c1">
    · <param name="c2">
    · <regression-coeff>

  The c_n fit parameters correspond to the best-fit coefficients of the nth order term. Thus, the fits relate the sampling speed DAC setting (DAC 0 for ATWD 0, DAC 4 for ATWD 1) to a sampling speed frequency as follows:

$$\text{sampling speed (MHz)} = c_0 + c_1 \cdot \text{DAC}[0,4] + c_2 \cdot \text{DAC}[0,4]^2 \ . \tag{5}$$

  This can obviously be inverted to get the time per sample for the waveform. Remember that the last sample in the raw waveform is the first sample in time.

- <baseline voltage="0">
  The first of a number of baseline measurements at various high voltage settings, which record the remnant baseline (<1 mV) after waveforms are transformed to voltage and the bias level subtracted. Ideally, this would be zero, but the baseline has been found to be very sensitive to the internal state of the DOM. DOM-Cal precisely determines the baseline in order to obtain accurate amplifier gain and charge measurements. Whether the user decides to use these baselines or determines them dynamically on a waveform-to-waveform basis is an open question. Note that these baselines are amplified voltages for the given channel, so they should be subtracted before dividing out the channel gain.

  * <base atwd=*atwd* channel=*channel* value=*value*>
    The *value* attribute records the baseline offset, in Volts, of a waveform in the given ATWD and channel. From the parent element one can determine that these baselines were measured with the high voltage off.

These baseline measurements have been obtained using the testDAQ ("stf") FPGA. For baseline measurements which are more applicable to data taken with the DAQ ("domapp") FPGA, see the <daq_baseline> calibration element.

– <daq_baseline>
A series of residual baseline measurements for each ATWD, channel, and bin obtained using the DAQ ("domapp") FPGA. The baseline values (in Volts) are given as follows:

  * <waveform atwd="*atwd*" channel="*channel*" bin="*bin*">*value*</waveform>

These baselines are amplified channel voltages, so they should be subtracted off before dividing out the channel gain. These baseline waveforms are obtained with the DOM in its nominal data-taking state and should more closely record residual baseline shifts in DAQ data than the <baseline> calibrations.

– <pmtTransitTime num_pts=*points*>
Contains a linear fit element giving the total transit time of the DOM (PMT transit time plus the delay board), as a function of high voltage. In particular, the fit provides the following relation:

$$\text{transit time (ns)} = m/\sqrt{V} + b \ . \tag{6}$$

Note the $1/\sqrt{V}$ dependence, where V is the high voltage, in Volts. This calibration can be used to adjust the waveform leading-edge times back to the time of light reaching the DOM.

The attribute num_pts indicates the number of high voltages used in the linear fit (a minimum of two).

– <hvGainCal>
A calibration of the gain of the PMT versus high voltage. A linear fit element provides the following log-log relation:

$$\log_{10} gain = m \cdot \log_{10} V + b \ . \tag{7}$$

– <pmtDiscCal numPts=*points*>
Contains a linear fit with the result of the SPE discriminator calibration. This calibration translates the SPE discriminator DAC setting (DAC 9) to the amplified charge (after the PMT) corresponding to that trigger level:

$$\text{charge trigger level (pC)} = m \cdot \text{DAC[9]} + b \ . \tag{8}$$

The attribute numPts indicates the number of discriminator settings used in the linear fit. If present, this calibration should be used in preference to the <discriminator> calibration, as it is more accurate for SPEs and sub-SPE pulses.

Because the discriminator level is relative to a given baseline determined by the FE (front end) bias voltage DAC (DAC 7), this calibration is only valid for a given setting of the bias voltage (recorded in the appropriate <dac> element).

- <baseline voltage=*voltage*>
  A sequence of baseline measurements as previously described. These baseline measurements are at non-zero high voltage settings, one for each of the voltages used for the HV gain calibration.
  Following the baseline measurements are charge histograms taken at various high voltages:
- <histo voltage=*voltage* convergent=*true/false* pv=*PV ratio* noiseRate=*rate* isFilled=*true/false*>

  The charge histogram recorded during the HV gain calibration at a given voltage. The attributes of this element are: the high voltage; whether the gain calibration was successful / convergent and used for the linear fit; the peak-to-valley ratio for convergent charge histograms; the noise rate at which the histogram was collected, in Hz; and whether the histogram data itself follows.
  The fit parameters to the histogram are always reported, even if the fit was not convergent (in which case the last iteration is recorded):
  - <param name="exponential amplitude">
  - <param name="exponential width">
  - <param name="gaussian amplitude">
  - <param name="gaussian mean">
  - <param name="gaussian width">

  As implied above, the charge histogram is fit to a functional form of $A\ e^{-Bq}\ +\ C\ e^{-E(q-D)^2}$, where q is the amplified charge in pC.
  If the *isFilled* attribute is true, the raw histogram data follows:
  - <histogram bins=*number of bins*>
    - <bin num=*bin* charge=*charge* count=*count*>
      The bin data *count* for a given bin *bin* is given along with the left edge charge value of that bin, in pC.

  The charge histograms are the final elements in the XML file. Because iterative HV/gain calibrations are possible, multiple charge histograms may be present for a given voltage.

3 Calibration Usage

This section gives a very basic description of how to use the calibration results to transform raw ATWD and FADC waveforms into voltage and time. More elaborate techniques in waveform reconstruction or feature extraction can follow but are not covered here.

3.1 ATWD Waveform Calibration

3.1.1 Raw Waveforms

To transform raw ATWD waveforms (testDAQ data, or DAQ data that has not been pedestal-subtracted) into voltage:

1. Use the linear fit for each waveform bin (slope m and intercept b for the appropriate ATWD, channel, and bin) from the <atwd> calibration to convert the ATWD counts into amplified Volts.

2. Subtract the bias voltage. From the bias DAC value (DAC 7), determine the front-end bias voltage from this relation:

$$\mathrm{V_{bias}(Volts)} = \mathrm{DAC[7]} \cdot 5.0/4096.0 \ . \tag{9}$$

3. Subtract any remnant baseline. For testDAQ data, an approximate value for the operating voltage can be retrieved from the <baseline> calibration, or the baseline can be determined from the waveform itself. For DAQ data, the <daq_baseline> waveform should be subtracted out at this point. Note that the latter is a function of the ATWD bin as well. So, to this point we have:

$$\mathrm{V(id, ch, bin)} = m(\mathrm{id, ch, bin}) \cdot \mathrm{wf(id, ch, bin)} + b(\mathrm{id, ch, bin}) - \mathrm{V_{bias}} - \mathrm{baseline(id, ch, bin)} \ . \tag{10}$$

4. Divide by the channel gain for the appropriate channel from the <amplifier> calibration.

3.1.2 Pedestal-Subtracted Waveforms

The procedure above is applicable to non-pedestal-subtracted waveforms. In DAQ data that has been compressed, the ATWD pedestal may have already been subtracted by the DOM, but a constant offset remains to allow the waveform to remain positive. This offset is currently the average of the pedestal waveform for that ATWD channel.

To transform pedestal-subtracted waveforms (with offset added) into voltage:

1. Reconstruct the baseline (the pedestal average) for this ATWD and channel:

$$\overline{p}(\mathrm{id, ch}) = \lfloor \ \frac{1}{N_{bin}} \ \sum_{bin} \left(\frac{\mathrm{V_{bias}} + \mathrm{daq\_baseline(id, ch, bin)} - b(\mathrm{id, ch, bin})}{m(\mathrm{id, ch, bin})} \right) \rfloor \tag{11}$$

   where m and b are the linear fit parameters from the <atwd> calibrations, and $\lfloor \ \rfloor$ is the floor operation (*i.e.* rounding in truncate mode).

2. Subtract this baseline from the waveform, and then use the slope from the linear fit from the <atwd> calibration to convert the ATWD counts into amplified Volts:

$$\mathrm{V(id, ch, bin)} = \mathrm{m(id, ch, bin)} \cdot (\mathrm{wf(id, ch, bin)} - \overline{p}(\mathrm{id, ch})) \ . \tag{12}$$

3. Subtract any remnant baseline, if necessary.

4. Divide by the channel gain for the appropriate channel.

3.1.3 Integrated Charge

To find the integrated charge of an ATWD waveform one must also:

1. Determine the sampling frequency of the ATWD used with the <atwdfreq> calibration in the result file.

2. Convert the summed voltages V_i into amplified charge. The front-end impedance Z (in Ohms) to use is found in the <frontEndImpedance> element.

$$\text{charge (pC)} = 10^{12} \cdot \frac{1}{Z\ (\Omega)} \cdot \frac{1}{\text{freq (Hz)}} \cdot \sum_i V_i \ . \tag{13}$$

3. Divide by the gain of the PMT for the operating high voltage using the linear log-log relationship in the <hvGainCal> calibration.

3.1.4 Time Calibration

To translate a leading edge time (or some other feature time) within an ATWD waveform to a photon hit time at the PMT:

1. Determine the bin position (interpolate if you like) of the feature.

2. Convert the bin offset within the waveform (recall sample 127 is the first sample) into a time T_{offset} using the <atwdfreq> sampling speed calibration for the appropriate ATWD.

3. Add the feature offset time to the ATWD trigger time T_{launch} (GPS time in nanoseconds).

4. Subtract the transit time T_{transit} for the given operating voltage, determined from the <pmtTransitTime> calibrated relationship.

5. Subtract the ATWD offset Δ_{ATWD} correction, from the the <atwd_delta_t> calibration. The ATWD offset is positive if the launch time for this ATWD is later than the ATWD used in the transit time calibration – it can be viewed as a correction to the transit time.

To summarize, the PMT hit time T_{hit} can be computed as follows:

$$\begin{aligned} T_{\text{hit}}\ \text{(ns)} &= T_{\text{launch}} + T_{\text{offset}} - (T_{\text{transit}} + \Delta_{\text{ATWD}}) \\ &= T_{\text{launch}} + \frac{\text{bin} \cdot 10^3}{\text{ATWD freq. (MHz)}} - \left(\frac{m_{\text{TT}}}{\sqrt{V}} + b_{\text{TT}} + \Delta_{\text{ATWD}} \right) \ . \end{aligned} \tag{14}$$

3.2 FADC Waveform Calibration

To calibrate an FADC waveform into voltage:

1. Subtract the baseline, using the value obtained from the <fadc_baseline> calibration at the operating DAC 10 level.

2. Convert the baseline-subtracted waveform into volts, using the (V/tick) constant G in the <fadc> calibration:

$$\mathrm{V_i\ (Volts)} = G \cdot (\mathrm{FADC}_i - \mathrm{baseline})\ . \tag{15}$$

To find the PMT hit time corresponding to a feature within an FADC waveform:

1. Determine the FADC sample position of the feature, interpolating if you like.
2. Determine the offset T_{offset} in ns from the FADC launch, using the FADC sampling frequency of 40.0 MHz.
3. Add this offset to the ATWD waveform start time T_{ATWD} (the launch time, corrected for waveform transit time and ATWD Δ_{ATWD} offset – see previous subsection), and add the FADC inherent time offset Δ_{FADC} from the <fadc_delta_t> calibration:

$$\begin{aligned} \text{FADC time (ns)} &= T_{\mathrm{offset}} + T_{\mathrm{ATWD}} + \Delta_{\mathrm{FADC}} \\ &= \frac{\mathrm{bin} \cdot 10^3}{40.0\ \mathrm{MHz}} + T_{\mathrm{launch}} - (T_{\mathrm{transit}} + \Delta_{\mathrm{ATWD}}) + \Delta_{\mathrm{FADC}}\ . \end{aligned} \tag{16}$$

   In the calibration results, one will note that Δ_{FADC} is negative, expressing the fact that the FADC digitization window starts before that of the ATWD.

3.3 Discriminator Setting

To find the discriminator DAC setting corresponding to some number N_{PE} of photoelectrons (PEs):

1. Determine the operating gain of the PMT at the given HV using the <hvGainCal> log-log fit:

$$g = 10^{m \cdot \log_{10}(\mathrm{HV})\ +\ b}\ . \tag{17}$$

2. Determine the SPE discriminator DAC setting for the desired charge by inverting the <pmtDiscCal> linear fit:

$$\mathrm{DAC[9]} = \frac{1}{m}(g \cdot N_{PE} \cdot e \cdot 10^{12} - b) \tag{18}$$

   where e is the charge of the electron, in Coulombs.

Please feel free to contact the authors if you have any questions about the use of these calibration results.

4 Changes

This section records changes in the XML file format since the first draft of this document (starting with DOM-Cal version 5.11).

- 7.4

  Added <pmtDiscCal> calibration, which refines the SPE discriminator calibration by using actual PMT pulses. If present, this calibration should be used in preference to the SPE <discriminator> calibration.

- 7.3
  Fixed sign of <atwd_delta_t> usage. Added more detail to hit time calculations for both ATWD and FADC.

- 7.2
  Added <atwd_delta_t> element to record offset between ATWD digitization start times. Switched <fadc_delta_t> calibration to use the "domapp" FPGA, increasing the offset by one clock cycle (25 ns).
  New: <atwd_delta_t> calibration records the ATWD digitization start offset relative to the transit time calibration. Both ATWD and FADC delta_t calibrations use the "domapp" FPGA.
  Old: No ATWD offset was available. The FADC time offset calibration used the "stf" FPGA, which has a delay once clock cycle smaller than the "domapp" FPGA.

- 7.0
  Added <daq_baseline> element to record residual baseline waveforms from the "domapp" FPGA.
  New: <daq_baseline> waveforms record the residual baseline for each ATWD, channel, and bin.
  Old: Only testDAQ "stf" baselines were available via the <baseline> elements.

  Client/server architecture changed substantially, in that the DOM doesn't write calibration results to the flash filesystem. Instead, the XML is generated on the DOM side and then sent to the surface Java client.

- 6.3
  Added front-end impedance element.
  New: <frontEndImpedance> records the impedance used in the calibration.
  Old: No impedance information recorded.

  Multiple charge histograms per voltage are now possible, if the option to iterate the HV/gain calibration was chosen at runtime. Also, all baseline measurements come before charge histograms.
  New: <baseline> and <histo> elements separated; may be more than one <histo> per voltage.
  Old: <baseline> and <histo> elements always came in pairs.

- 6.2
  Added time of calibration (GMT).
  New: <time> HH:MM:SS </time>
  Old: No time information recorded.

No change to date format *specification*, but note that code before this version actually used the American MM-DD-YYYY format, instead of DD-MM-YYYY.
New: <date> DD-MM-YYYY </date>
Old: <date> MM-DD-YYYY </date>

Added patch version number.

- 6.1
  Added MPE discriminator calibration. There are now two <discriminator> elements, one with id="spe" (the previous SPE discriminator calibration), and the new MPE discriminator calibration with id="mpe".
  New: <discriminator id="spe"> and <discriminator id="mpe"> record linear fits for SPE and MPE discriminator calibrations.
  Old: <discriminator> calibration recorded only the the linear fit for the SPE discriminator calibration.

- 6.0
  Changed nominal value of front-end impedance based on measurements from LBNL. Charge integration code must use this new value starting with this version of DOM-Cal calibration results.
  New: Nominal FE impedance is 43 Ω.
  Old: Nominal FE impedance was 50 Ω.

  Added FADC calibration. Baseline (in FADC ticks) as a function of FADC front-end bias (DAC 10) is calibrated with a linear fit. The gain of the FADC, including intrinsic gain and amplifiers is recorded along with the error of this mean gain value. The units on this gain value are V/tick and should multiply the FADC value, unlike the ATWD channel gain calibrations.
  New: <fadc_baseline> linear fit records baseline as a function of DAC setting. <fadc_gain> records gain value and error.
  Old: FADC placeholder elements, <fadc parname="pedestal" value="0">, and <fadc parname="gain" value="1">.

  Added FADC time offset calibration. Time offset in ns from ATWD waveform start is recorded, along with an error on this mean value. Value is negative, reflecting the fact that FADC waveform starts earlier in time than the ATWD waveform.
  New: <fadc_delta_t> records delta_t value and error.
  Old: N/A

  Added discriminator calibration. SPE discriminator trigger level (amplified charge, in pC) as a function of SPE discriminator DAC setting is recorded as a linear fit.

New: <discriminator> linear fit records calibration.
Old: N/A

Removed pulser calibration. Pulser charge replaces discriminator level as primary uncalibrated input.
New: N/A
Old: <pulser> linear fit recorded pulser amplitude as a function of pulser DAC setting.

- 5.14

Changes to <atwdfreq> calibration element. Fit model is now quadratic instead of linear, and value resulting from the fit no longer needs to be multiplied by the clock frequency.
New: <fit model="quadratic">, with three fit coefficients and R^2.
Frequency in MHz given by this relation:

$$\text{sampling speed (MHz)} = c_0 + c_1 \cdot \text{DAC}[0,4] + c_2 \cdot \text{DAC}[0,4]^2 \ . \tag{19}$$

Old: <fit model="linear">, with two fit coefficients and R^2.
Frequency in MHz given by this relation:

$$\text{sampling speed (MHz)} = 20.0 \ (m \cdot \text{DAC}[0,4] + b \ ). \tag{20}$$

- 5.13

Added attribute "num_pts" to pmtTransitTime to indicate how many high voltage points were used for the linear fit (minimum of 2).
New: <pmtTransitTime num_pts="9">
Old: <pmtTransitTime>