

Sistema

Memoria

```
graph TD; Memoria[Memoria] --- Bus; Bus --- CPU1[CPU]; Bus --- CPU2[CPU]; Bus --- CPU3[CPU]; Bus --- CPU4[CPU];
```

The diagram illustrates a system architecture. At the top, a light green rounded rectangle labeled 'Memoria' is connected by a vertical line to a horizontal bus. From this bus, four vertical lines extend downwards to four separate light blue squares, each labeled 'CPU'. The entire diagram is set against a light blue background with a dashed black border.

CPU

CPU

CPU

CPU