EVALUATION KIT AVAILABLE

MAX32550

DeepCover Secure Cortex-M3 Flash Microcontroller

General Description

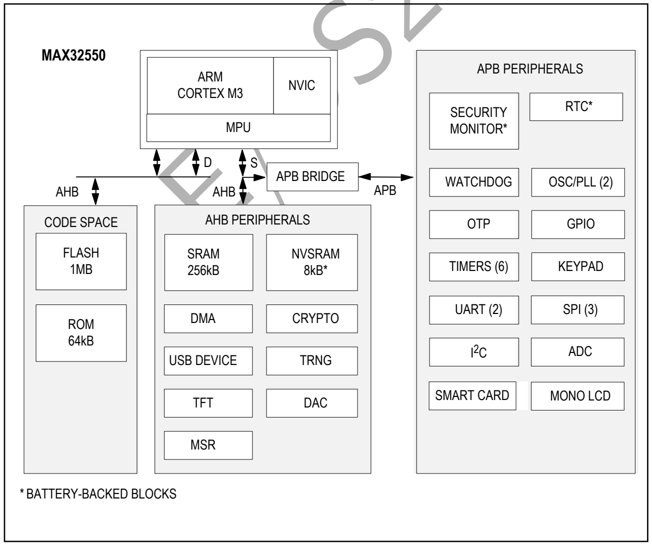
DeepCover® embedded security solutions cloak sensitive data under multiple layers of advanced physical security to provide the most secure key storage possible.

The DeepCover Secure microcontroller (MAX32550) provides an interoperable, secure, and cost-effective solution to build new generations of trusted devices such as mobile chip and pin pads. The MAX32550 is based on a Cortex M3 processor with 1MB of embedded flash, 256KB of system RAM, 8KB of battery-backed AES self-encrypted NVSRAM. It includes all the essential functions of mobile POS terminal including a cryptographic engine, a true random number generator, battery-backed RTC, environmental and tamper detection circuitry, a magnetic stripe reader, a smart card controller with embedded transceiver to directly support 1.8V, 3.3V, and 5V cards, and an integrated secure keypad controller. It also provides a seamless interface to TFT displays and includes a vast array of peripherals, SPIs, UARTs, DMA, ADC, and DAC that add flexibility to control and differentiate the system design.

Applications

- PCI Mobile Payment Terminals (mPOS)
- ATM Keyboards
- EMV Card Reader

Functional Diagram



Benefits and Features

- ARM® Cortex® M3 Processor Core Allows for Easy Integration into Applications
  - 108MHz Core Operating Frequency Through PLL
  - 1MB Dual-Bank Flash Memory with Cache
  - 256KB System SRAM
  - 8KB AES Self-Encrypted NVSRAM
- Security Features Facilitate System-Level Protection
  - Secure Boot Loader with Public Key Authentication
  - AES, DES and SHA Hardware Accelerators
  - Modulo Arithmetic Hardware Accelerator (MAA) Supporting RSA, DSA, and ECDSA
  - 8-Line Secure Keypad Controller
  - Hardware True Random-Number Generator
  - Die Shield with Dynamic Fault Detection
  - 6 External Tamper Sensors with Independent Random Dynamic Patterns
  - 256-Bit Flip-Flop-Based Battery-Backup AES Key Storage
  - Temperature and Voltage Tamper Monitor
  - Real-Time Clock
- Integrated Peripherals Reduce External Component Count
  - Triple-Track Magnetic Stripe Head Interface
  - One ISO 7816 Smart Card Interface with Integrated Transceiver (1.8V, 3V, and 5V)
  - USB 2.0 Device with Internal Transceiver and Dedicated PLL
  - 3 SPI Ports, 2 UART Ports, and 1 I^2C Controller
  - 6 Timers, 4 with PWM Capability
  - Up to 70 General-Purpose I/O Pins
  - 2-Channel, 10-Bit ADC and 1-Channel, 8-Bit DAC
  - Color/Monochrome LCD TFT Controller
  - 4-Channel DMA Controller
- Power Management Optimizes Battery Life and Reduces Active Power Consumption
  - Single 3.3V Supply Operation*
  - Integrated Battery-Backup Switch
  - Clock Gating Function
  - Low-Current Battery-Backup Operation

**5V smart card support requires external 5.0V supply.*

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Absolute Maximum Ratings

(All voltages with respect to GND.)

V_{DD}, V_{DDA}	-0.5V to +3.6V
SC_VDDA	-0.5V to +5.5V
Any Lead	-0.5V to V_{DD} + 0.5V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Continuous Power Dissipation (T_A = +85°C)	1231mW
Soldering Temperature	See IPC/JEDEC J-STD-020A

Package Thermal Characteristics (Note 1)

CSBGA

Junction-to-Ambient Thermal Resistance (θ_{JA})	32.5°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8.8°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage	V_{DD}, V_{DDA}		3.0	3.3	3.6	V
	V_{SC_VDDA}	1.8/3V cards	3.2	3.3	5.5	V
		1.8/3/5V cards	5.15	5.25	5.5	V
Battery Supply Voltage	V_{BAT}		2.3		3.6	V
Main Battery Supply Voltage	V_{MAIN}		0		3.6	V
Main Battery Supply Switching Threshold	V_{MAIN_SWITCH}		2.3	2.5	2.7	V
Power-Fail Reset Voltage	V_{RST}		2.8		3.0	V
Power-Fail Warning Voltage	V_{PFW}			V_{RST} + 0.05		V
Supply Current (Note 2)	I_{DD1}	f_{SYS} = 108MHz T_A = +25°C		60	80	mA
Idle Mode Current (Note 3)	I_{IDLE}	T_A = +25°C		9.4		mA
		T_A = +85°C		10.5		mA
Standby Mode Current (Note 4)	I_{STBY}	T_A = +25°C		550		µA
		T_A = +85°C		1220		µA
Battery Back Mode Current (Note 5)	I_{BAT}	T_A = +25°C		3.9		µA
		T_A = +85°C		4.4		µA
Main Battery Back Mode Current (Note 6)	I_{MAIN}	T_A = +25°C		7		µA
Battery Leakage Current (Note 7)	I_{BAT2}	T_A = +25°C			100	nA
EXTERNAL CRYSTAL OSCILLATOR						
External Oscillator/Crystal Frequency (Note 8)	f_{HFXIN}			12		MHz
Crystal Oscillator Startup Time	t_{HFSU}			8192		cycles

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL OSCILLATOR						
Oscillator Frequency	f_{OSC}		84	96	108	MHz
NANOPOWER RING						
Nanopower Ring Frequency	f_{NANO}		4.2	8.0	14	kHz
Digital I/O (Note 9)						
Input High Voltage (All Pins Except External Sensors)	V_{IH}		0.7 x V_{DD}		V_{DD}	V
Input Hysteresis (All Pins Except External Sensors)	V_{IHYS}			0.3		V
Input Low Voltage (All Pins Except External Sensors)	V_{IL1}		GND		0.3 x V_{DD}	V
Output Low Voltage (Standard Port Pins)	V_{OL2}	I_{OL} = 2mA			0.4	V
Output High Voltage (Standard Port Pins)	V_{OH2}	I_{OH} = -2mA	V_{DD} -0.4			V
Output Low Voltage (High-Drive Port Pins)	V_{OL4}	I_{OL} = 4mA			0.4	V
Output High Voltage (High-Drive Port Pins)	V_{OH4}	I_{OH} = -4mA	V_{DD} -0.4			V
Input Leakage Current	I_L	Internal pullup disabled	-1		+1	µA
Input Capacitance (HFXIN)	C_{HFXIN}			8		pF
Input Capacitance (32KIN)	C_{32KIN}			6		pF
Input Capacitance (All Port Pins)	C_{IN}			5		pF
Input Pullup Resistance (All Port Pins and RSTIN)	R_{PU}		50	100	150	kΩ
Input Pulldown Resistance (All Port Pins)	R_{PD}		50	100	150	kΩ
USB						
USB Supply Voltage	V_{USB}			V_{DD}		V
Input High Voltage D+, D-	V_{IH_USB}	(Note 10)	2.0			V
Input Low Voltage D+, D-	V_{IL_USB}	(Note 10)			0.8	V
Output Low Voltage D+, D-	V_{OL_USB}	RL = 1.5 kΩ from DP to V_{USB} and IOL = 4mA (Note 10)	GND		0.3	V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage D+, D-	V_{OH_USB}	RL = 15 kΩ from DP and DM to GND and IOH = 4mA (Note 10)	2.8		V_{DD}	V
Transition Time (Rise/Fall) D+, D- (Note 11)	t_{RF}	CL = 50pF (Note 10)	4		20	nS
D+, D- Pin Capacitance	C_{IN_USB}	Pin to GND		8		pF
Differential Input Sensitivity for D+, D-	V_{DI}	FSD+ to FSD- (Note 10)	0.2			V
Common-Mode Voltage Range	V_{CM}	Includes VDI range (Note 10)	0.8		2.5	V
Single-Ended Receiver Threshold	V_{SE}	(Note 10)	0.8		2.0	V
Single-Ended Receiver Hysteresis	V_{SEH}			200		mV
Differential Output Signal Cross-Point Voltage	V_{CRS}	GBD	1.3		2.0	V
Internal Pullup Resistor	R_{PU_USB}	Idle (Note 10)	0.9		1.575	kΩ
		Receiving (Note 10)	1.425		3.090	kΩ
Driver Output Resistance	R_{DRV}		28		44	Ω
ENVIRONMENTAL SENSORS						
V_{DD} Overvoltage Threshold	V_{DD_OV}		3.6		3.8	V
V_{BAT} Undervoltage Threshold	V_{BAT_UV}		2.1		2.3	V
V_{BAT} Over Voltage Threshold	V_{BAT_OV}		3.6		3.8	V
High-Temperature Threshold	T_{HTR}	GBD	110	120	130	°C
Low-Temperature Threshold	T_{LTR1}	GBD	-70	-60	-50	°C
	T_{LTR2}	GBD	-44	-37	-30	°C
10-BIT ADC						
Resolution				10		Bits
ADC Clock Frequency	f_{ACLK}		0.1		3.375	MHz
AN0–AN1 Input Voltage Range	V_{AN}		GND		V_{DDA}	V
Analog Input Capacitance	C_{AIN}			1		pF
Integral Nonlinearity	INL	(Note 12)			±2	LSB
Differential Nonlinearity	DNL	(Note 12)			±1	LSB
Offset Error	V_{OS}	(Note 12)			±4	LSB
ADC Active Current	I_{ADC}	ACLK = 3.375MHz, internal reference on		260		µA
ADC Setup Time	t_{ADC_SU}			30		µs
ADC Output Latency	t_{ADC}			1025		TACLK
ADC Settling Time	t_{ADC_SETTLE}	Due to channel or reference change		48 14		FACLK µs
ADC Throughput	F_{ADC}				3.375	ksps

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
10-BIT ADC REFERENCE						
Internal Reference Voltage	V_{IREF}			1.22	±5%	V
External Reference Voltage	V_{EXTREF}				V_{DDA}	V
Internal Reference Setup Time	t_{IREF_SU}			30		μs
8-BIT DAC						
Resolution	DAC_R	Guaranteed monotonic		8		Bits
Differential Nonlinearity	DNL	Code 07 to F9h (Note 10)		±0.2		LSB
Integral Nonlinearity	INL	Code 07 to F9h (Note 10)		±0.4		LSB
Offset Error	E_O	(Note 10)		±2		LSB
Gain Error	E_G	(Note 10)		±2		LSB
Power up Time	T_{PU}			200		μs
Full-Scale Voltage	V_{DACOUT}			2.0		V
SMART CARD						
Active SC_VDDA Current 5V Cards	I_{DD_SC5}	Regulator on, SC_VDDA = 5.25V, f_{SC_CLK} = 5MHz (Note 10)		I_{LOAD} + 2.5mA	I_{LOAD} + 3.5mA	mA
Active SC_VDDA Current 3V Cards	I_{DD_SC33}	Regulator on, SC_VDDA = 3.3V, f_{SC_CLK} = 5MHz (Note 10)		I_{LOAD} + 1.5mA	I_{LOAD} + 2.5mA	mA
Active SC_VDDA Current 1.8V Cards	I_{DD_SC18}	Regulator on, SC_VDDA = 3.3V, f_{SC_CLK} = 5MHz (Note 10)		I_{LOAD} + 1mA	I_{LOAD} + 1.5mA	mA
Inactive Mode Current	I_{DD_SCIDLE}	Card inactive, regulator off		1		μA
SMART CARD—SC_VCC						
Output Low Voltage—Card-Inactive Mode	V_{SC_VCC1}	ISC_VCC = 1mA (Note 10)	0		0.3	V
Output Current—Card-Inactive Mode	I_{SC_VCC1}	SC_VCC = 0V (Note 10)	0		-1	mA
Slew Rate—Card-Active Mode	$\lvert V_{SC\_VCCR} \rvert$	Up/down, C < 300nF		0.10		V/μs
Output Low Voltage—Card Active Mode	V_{SC_VCC2}	5V supply selected, ISC_VCC < -60mA (Note 10)	4.60	5	5.25	V
		3V supply selected, ISC_VCC < -55mA (Note 10)	2.78	3	3.22	
		1.8V supply selected, ISC_VCC < -40mA (Note 10)	1.66	1.8	1.94	
Output Current—Card Active Mode	I_{SC_VCC2}	5V supply selected, SC_VCC = 0V–5.25V (Note 10)			-60	mA
		3V supply selected, SC_VCC = 0V–3.3V (Note 10)			-55	
		1.8V supply selected, SC_VCC = 0V–1.8V (Note 10)			-40	

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Shutdown Current Threshold	$I_{SC\_VCC\_SD}$			152		mA
SMART CARD—SC_DETECT						
Input Low Voltage	V_{ILSC_DETECT}	(Note 10)			0.3 x V_{DD}	V
Input High Voltage	V_{IHSC_DETECT}	(Note 10)	0.7 x V_{DD}			V
Input Low Current	I_{ILSC_DETECT}	V_{SC_DETECT} = 0V (Note 10)	-5	-3	0	μA
Input High Current	I_{IHSC_DETECT}	V_{SC_DETECT} = V_{DD} (Note 10)	-1		+1	μA
SMART CARD—SC_CLK						
Output Low Voltage—Card Inactive Mode	V_{OLSC_CLK}	I_{OLSC_CLK} = 1mA (Note 10)	0		0.3	V
Output Current—Card-Inactive Mode	I_{OLSC_CLK}	V_{OL_SCCLK} = 0V (Note 10)		±15		μA
Output Low Voltage—Card-Active Mode	V_{OL1SC_CLK}	I_{OLSC_CLK} = 200μA (Note 10)	0		0.2 x V_{SC_VCC}	V
Output High Voltage—Card-Active Mode	V_{OHSC_CLK}	I_{OLSC_CLK} = -200μA (Note 10)	0.7 x V_{SC_VCC}		V_{SC_VCC}	V
Rise Time—Card-Active Mode	t_{RSC_CLK}	C_L = 30pF, f_{SC_CLK} = 5MHz 10%–90%, GBD			8% of f_{SC_CLK}	ns
Fall Time—Card-Active Mode	t_{FSC_CLK}	C_L = 30pF, f_{SC_CLK} = 5MHz 10%–90%, GBD			8% of f_{SC_CLK}	ns
Current Limitation—Card-Active Mode	$I_{SC\_CLK\_LIM}$	(Note 10)	-55		+55	mA
Clock Frequency—Card Active Mode	f_{SC_CLK}	Operational (Note 10)	1		4.8	MHz
SMART CARD—SC_RST						
Output Low Voltage—Card Inactive Mode	V_{OLSC_RST}	I_{OLSC_RST} = 1mA (Note 10)	0		0.3	V
Output Current—Card-Inactive Mode	I_{OLSC_RST}	V_{OLSC_RST} = 0V (Note 10)		±15		μA
Output Low Voltage—Card-Active Mode	V_{OL1SC_RST}	I_{OLSC_RST} = 150μA (Note 10)	0		0.12 x V_{SC_VCC}	V
Output High Voltage—Card-Active Mode	V_{OHSC_RST}	I_{OHRST} = -200μA (Note 10)	0.8 x V_{SC_VCC}		V_{SC_VCC}	V
Fall Time—Card-Active Mode	T_{FSC_RST}	C_L = 30pF, 90% to 10%, GBD			0.1	μs
Rise Time—Card-Active Mode	T_{RCS_RST}	C_L = 30 pF, 10% to 90%, GBD			0.1	μs
Current Limitation—Card-Active Mode	I_{SC_RST}(LIMIT)	(Note 10)	-10		+10	mA

Electrical Characteristics (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SMART CARD—SC_C4, SC_C8						
Output Low Voltage—Card Inactive Mode	V_{OLSC_C48}	I_{OLSC_C48} = 1mA (Note 10)	0		0.3	V
Output Current—Card-Inactive Mode	I_{OLSC_C48}	V_{OLSC_C48} = 0V (Note 10)		±15		µA
Internal Pullup Resistor—Card Inactive Mode	R_{PUPSC_C48}	Between C4 or C8 and SC_VCC (Note 10)	9		14.5	kΩ
Output Low Voltage—Card-Active Mode	V_{OL1SC_C48}	I_{OLSC_C48} = 1mA (Note 10)	0		0.4	V
Output High Voltage—Card-Active Mode	V_{OHSC_C48}	I_{OHSC_C48} ≤ -20µA (Note 10)	0.8 x V_{SC_VCC}		V_{SC_VCC}	V
		I_{OHSC_C48} ≤ -40µA (3V/5V) (Note 10)	0.75 x V_{SC_VCC}		V_{SC_VCC}	
Current Limitation—Card-Active Mode	$I_{SC\_C48(LIMIT)}$	(Note 10)	-15		+15	mA
Output Rise/Fall Time—Card-Active Mode	t_{RFSC_C48}	C_L = 30 pF f_{MAX_C48} = 1MHz, GBD			0.8	µs
Input Low Voltage—Card-Active Mode	V_{ILSC_C48}	(Note 10)	-0.3		0.15 x V_{SC_VCC}	V
Input Low Current—Card Active Mode	I_{ILSC_C48}	V_{ILSC_C48} = 0V (Note 10)	-850			µA
Input High Current—Card Active Mode	I_{IHSC_C48}	V_{IHSC_C48} = V_{SC_VCC} (Note 10)			20	µA
Input High Voltage—Card Active Mode	V_{IHSC_C48}	(Note 10)	0.7 V_{SC_VCC}		V_{SC_VCC}	V
SMART CARD—SC_IO						
Output Low Voltage—Card Inactive Mode	V_{OLSC_IO}	I_{OLSC_IO} = 1mA (Note 10)	0		0.15 x V_{SCVCC}	V
Output Current—Card-Inactive Mode	I_{OLSC_IO}	V_{OLSC_IO} = 0V (Note 10)		±15		µA
Internal Pullup Resistor—Card Inactive Mode	R_{PUPSC_IO}	To SC_V_{CC} (Note 10)	9		14.5	kΩ
Output Low Voltage—Card-Active Mode	V_{OL1SC_IO}	I_{OLSC_IO} = 1mA (Note 10)	0		0.15 x V_{SCVCC}	V
Output High Voltage—Card-Active Mode	V_{OHSC_IO}	I_{OHSC_IO} ≤ -20µA (Note 10)	0.8 x V_{SCVCC}		V_{SCVCC}	V
Output High Voltage—Card Active Mode	V_{OHSC_IO}	I_{OHSC_IO} ≤ -40µA (3V/5V) (Note 10)	0.75 x V_{SCVCC}		V_{SCVCC}	V

Electrical Characteristics (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Limitation—Card-Active Mode	I_{SC_IO}(LIMIT)	(Note 10)	-15		+15	mA
Output Rise/Fall Time—Card-Active Mode	T_{RFSC_IO}	C_L = 30 pF, GBD			0.8	µs
Input Low Voltage—Card-Active Mode	V_{ILSC_IO}	(Note 10)	-0.3		0.15 x V_{SCVCC}	V
Input Low Current—Card Active Mode	I_{ILSC_IO}	V_{ILSC_IO} = 0V (Note 10)	-850			µA
Input High Current—Card Active Mode	I_{IHSC_IO}	V_{IHSC_IO} = V_{SC_VCC} (Note 10)			20	µA
Input High Voltage—Card Active Mode	V_{IHSC_IO}	(Note 10)	0.7 x V_{SCVCC}		V_{SCVCC}	V
SMART CARD TIMING						
Activation Time	t_{ACT}			160		µs
Deactivation Time	t_{DEACT}			80		µs
SC_DETECT Debounce Time	t_{DBSC_DETECT}			8		ms

Note 2: Measured on the V_{DD} pin and the part not in reset. All inputs are connected to GND or V_{DD}. Outputs do not source/sink any current. Part is executing code from internal RAM.

Note 3: Measured on the V_{DD} pin and the part not in reset. All inputs are connected to GND or V_{DD}. Outputs do not source/sink any current.

(Footnotes)

Note 4: Measured on the V_{DD} pin and the part not in reset. All inputs are connected to GND or V_{DD}. Outputs do not source/sink any current.

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Note 5: Measured on the V_{BAT} pin. V_{MAIN} = 0V, V_{BAT} = 3.3V, and V_{DD} = 0V. All inputs connected to GND. Outputs do not source/sink any current. RTC, die shield, temperature sensors, voltage sensors, and external sensors are enabled. External sensor pairs are tied together with 0Ω resistors. The external sensor clock is 2kHz.

Note 6: Measured on the V_{MAIN} pin. V_{MAIN} = 3.3V, V_{BAT} = 3.3V and V_{DD} = 0V. All inputs connected to GND. Outputs do not source/sink any current. RTC, die shield, temperature sensors, voltage sensors, and external sensors are enabled. External sensor pairs are tied together with 0Ω resistors. The external sensor clock is 2kHz.

Note 7: Measured on the V_{BAT} pin. V_{MAIN} = 2.8V, V_{BAT} = 3.6V and V_{DD} = 0V. All inputs connected to GND. Outputs do not source/sink any current.

Note 8: External oscillator duty cycle should be between 45% and 55%.

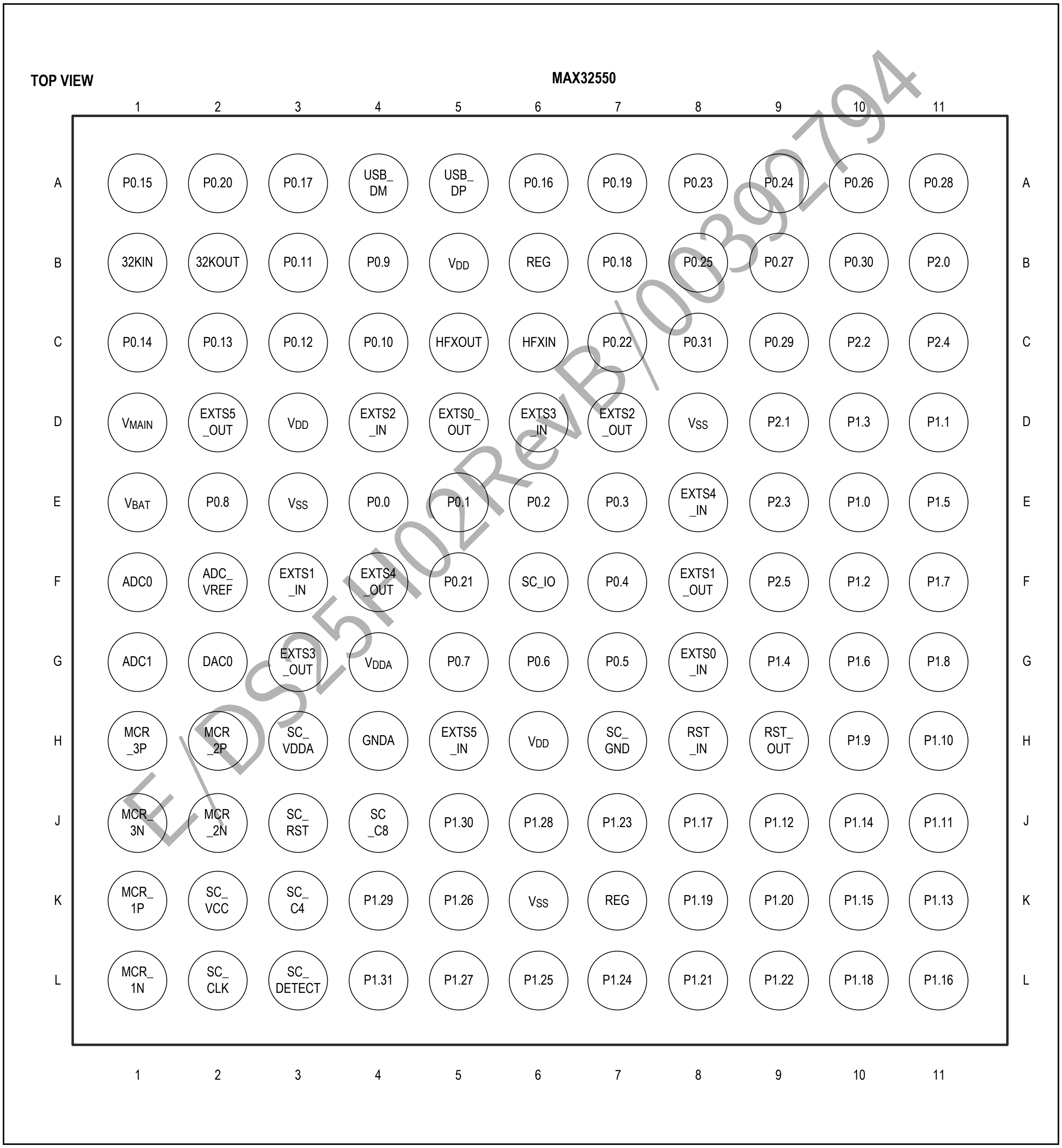
Note 9: The maximum total current, I_{OH} (max) and I_{OL} (max), for all listed outputs combined should not exceed 100mA to satisfy the maximum specified voltage drop.

Note 10: Production tested at T_A = +85°C.

Note 11: As per USB 2.0 specification, rise and fall time transitions must also be matched to within ±10%.

Note 12: Production tested at T_A = +25°C.

Pin Configuration



	1	2	3	4	5	6	7	8	9	10	11
A	P0.15	P0.20	P0.17	USB_DM	USB_DP	P0.16	P0.19	P0.23	P0.24	P0.26	P0.28
B	32KIN	32KOUT	P0.11	P0.9	V_{DD}	REG	P0.18	P0.25	P0.27	P0.30	P2.0
C	P0.14	P0.13	P0.12	P0.10	HFXOUT	HFXIN	P0.22	P0.31	P0.29	P2.2	P2.4
D	V_{MAIN}	EXTS5_OUT	V_{DD}	EXTS2_IN	EXTS0_OUT	EXTS3_IN	EXTS2_OUT	V_{SS}	P2.1	P1.3	P1.1
E	V_{BAT}	P0.8	V_{SS}	P0.0	P0.1	P0.2	P0.3	EXTS4_IN	P2.3	P1.0	P1.5
F	ADC0	ADC_VREF	EXTS1_IN	EXTS4_OUT	P0.21	SC_IO	P0.4	EXTS1_OUT	P2.5	P1.2	P1.7
G	ADC1	DAC0	EXTS3_OUT	V_{DDA}	P0.7	P0.6	P0.5	EXTS0_IN	P1.4	P1.6	P1.8
H	MCR_3P	MCR_2P	SC_VDDA	GNDA	EXTS5_IN	V_{DD}	SC_GND	RST_IN	RST_OUT	P1.9	P1.10
J	MCR_3N	MCR_2N	SC_RST	SC_C8	P1.30	P1.28	P1.23	P1.17	P1.12	P1.14	P1.11
K	MCR_1P	SC_VCC	SC_C4	P1.29	P1.26	V_{SS}	REG	P1.19	P1.20	P1.15	P1.13
L	MCR_1N	SC_CLK	SC_DETECT	P1.31	P1.27	P1.25	P1.24	P1.21	P1.22	P1.18	P1.16

Pin Description

BALL	GPIO PORT NUMBER	PRIMARY FUNCTION	SECONDARY FUNCTION	FUNCTION
E4	P0.0	KBD0	—	Keyboard I/O
E5	P0.1	KBD1	—	Keyboard I/O
E6	P0.2	KBD2	—	Keyboard I/O
E7	P0.3	KBD3	—	Keyboard I/O
F7	P0.4	KBD4	—	Keyboard I/O
G7	P0.5	KBD5	—	Keyboard I/O
G6	P0.6	KBD6	—	Keyboard I/O
G5	P0.7	KBD7	—	Keyboard I/O
E2	P0.8	RXD0	—	UART0 Data Input
B4	P0.9	TXD0	—	UART0 Data Output
C4	P0.10	RTS0	SC_C4_BYP	UART0 Request to Send/Smart Card C4 Bypass
B3	P0.11	CTS0	SC_C8_BYP	UART0 Clear to Send/Smart Card C8 Bypass
C3	P0.12	RXD1	—	UART1 Data Input
C2	P0.13	TXD1	—	UART1 Data Output
C1	P0.14	RTS1	—	UART1 Request to Send
A1	P0.15	CTS1	—	UART1 Clear to Send
A6	P0.16	MISO0	—	SPI0 Master In, Slave Out
A3	P0.17	MOSI0	—	SPI0 Master Out, Slave In
B7	P0.18	SCLK0	—	SPI0 Clock
A7	P0.19	SSEL0_0	—	SPI0 Slave Select 0
A2	P0.20	SSEL0_1	—	SPI0 Slave Select 1
F5	P0.21	SSEL0_2	SC_IO_BYP	SPI0 Slave Select 2/Smart Card I/O Bypass
C7	P0.22	SSEL0_3	SC_RST_BYP	SPI0 Slave Select 3/Smart Card Reset Bypass
A8	P0.23	SDA	—	I^2C Data
A9	P0.24	SCL	—	I^2C Clock
B8	P0.25	MISO1	—	SPI1 Master In, Slave Out
A10	P0.26	MOSI1	—	SPI1 Master Out, Slave In
B9	P0.27	SCLK1	—	SPI1 Clock
A11	P0.28	SSEL1_0	—	SPI1 Slave Select 0
C9	P0.29	SSEL1_1	—	SPI1 Slave Select 1
B10	P0.30	SSEL1_2	TCLK2	SPI1 Slave Select 2/Timer 2 CLK I/O
C8	P0.31	SSEL1_3	TCLK3	SPI1 Slave Select 3/Timer 3 CLK I/O
E10	P1.0	TCLK0	SC_DETECT_BYP	Timer 0 CLK I/O/Smart Card Detect Bypass
D11	P1.1	TCLK1	SC_CLK_BYP	Timer 1 CLK I/O/Smart Card CLK Bypass

Pin Description (continued)

BALL	GPIO PORT NUMBER	PRIMARY FUNCTION	SECONDARY FUNCTION	FUNCTION
F10	P1.2	LCD_DATA0	LCD_CLK	Mono LCD Data 0/LCD Clock
D10	P1.3	LCD_DATA1	LCD_HSYNC	Mono LCD Data 1/LCD Horizontal Sync
G9	P1.4	LCD_DATA2	LCD_VSYNC	Mono LCD Data 2/LCD Vertical Sync
E11	P1.5	LCD_DATA3	LCD_VDEN	Mono LCD Data 3/LCD Video Data Enable
G10	P1.6	LCD_DATA4	LCD_GREEN0	Mono LCD Data 4/LCD Green Value 0
F11	P1.7	LCD_DATA5	LCD_GREEN1	Mono LCD Data 5/LCD Green Value 1
G11	P1.8	LCD_DATA6	LCD_GREEN2	Mono LCD Data 6/LCD Green Value 2
H10	P1.9	LCD_DATA7	LCD_GREEN3	Mono LCD Data 7/LCD Green Value 3
H11	P1.10	LCD_EN	LCD_GREEN4	Mono LCD Enable/LCD Green Value 4
J11	P1.11	LCD_RS	LCD_GREEN5	Mono LCD Command/Data Select/LCD Green Value 5
J9	P1.12	LCD_RW	LCD_GREEN6	Mono LCD RW/LCD Green Value 6
K11	P1.13	MISO2	LCD_GREEN7	LCD Green Value 7/SPI2 Master In, Slave Out
J10	P1.14	—	LCD_BLUE0	LCD Blue Value 0
K10	P1.15	—	LCD_BLUE1	LCD Blue Value 1
L11	P1.16	—	LCD_BLUE2	LCD Blue Value 2
J8	P1.17	—	LCD_BLUE3	LCD Blue Value 3
L10	P1.18	—	LCD_BLUE4	LCD Blue Value 4
K8	P1.19	SSEL2_2	LCD_BLUE5	LCD Blue Value 5/SPI2 Slave Select 2
K9	P1.20	SSEL2_0	LCD_BLUE6	LCD Blue Value 6/SPI2 Slave Select 0
L8	P1.21	MOSI2	LCD_BLUE7	LCD Blue Value 7/SPI2 Master Out, Slave In
L9	P1.22	—	LCD_RED0	LCD Red Value 0
J7	P1.23	—	LCD_RED1	LCD Red Value 1
L7	P1.24	—	LCD_RED2	LCD Red Value 2
L6	P1.25	—	LCD_RED3	LCD Red Value 3
K5	P1.26	—	LCD_RED4	LCD Red Value 4
L5	P1.27	SSEL2_3	LCD_RED5	LCD Red Value 5/SPI2 Slave Select 3
J6	P1.28	SSEL2_1	LCD_RED6	LCD Red Value 6/SPI2 Slave Select 1
K4	P1.29	SCLK2	LCD_RED7	LCD Red Value 7/SPI2 Clock
J5	P1.30	—	LCD_PWREN	LCD Power Enable
L4	P1.31	—	LCD_LEND	LCD Line End
G8	—	EXTS0_IN	—	External Sensor 0 Input
D5	—	EXTS0_OUT	—	External Sensor 0 Output
F3	—	EXTS1_IN	—	External Sensor 1 Input
F8	—	EXTS1_OUT	—	External Sensor 1 Output
D4	—	EXTS2_IN	—	External Sensor 2 Input
D7	—	EXTS2_OUT	—	External Sensor 2 Output

Pin Description (continued)

BALL	GPIO PORT NUMBER	PRIMARY FUNCTION	SECONDARY FUNCTION	FUNCTION
D6	—	EXTS3_IN	—	External Sensor 3 Input
G3	—	EXTS3_OUT	—	External Sensor 3 Output
E8	—	EXTS4_IN	—	External Sensor 4 Input
F4	—	EXTS4_OUT	—	External Sensor 4 Output
H5	—	EXTS5_IN	—	External Sensor 5 Input
D2	—	EXTS5_OUT	—	External Sensor 5 Output
A4	—	USB_DM	—	USB D-
A5	—	USB_DP	—	USB D+
B11	P2.0	V_{BUS_DET}	—	USB V_{BUS} Detect
H8	—	RSTIN	—	System Reset Input
H9	—	RSTOUT	—	System Reset Output
C6	—	HFXIN	—	High-Frequency Crystal Clock Input
C5	—	HFXOUT	—	High-Frequency Crystal Clock Output
B1	—	32KIN	—	32K RTC Crystal Input
B2	—	32KOUT	—	32K RTC Crystal Output
D9	P2.1	TDI	—	JTAG Test Data Input
C10	P2.2	TDO	—	JTAG Test Data Output
E9	P2.3	TMS	—	JTAG Test Mode Select
C11	P2.4	TCK	—	JTAG Test Clock
F9	P2.5	JTRST	—	JTAG Reset
B5, D3, H6	—	V_{DD}	—	Digital Supply Voltage
B6,K7	—	REG	—	Regulator Capacitor
E1	—	V_{BAT}	—	Battery Backup Power Supply
D1	—	V_{MAIN}	—	Main Battery Supply for Battery Backup mode
D8, E3, K6	—	V_{SS}	—	Core and I/O Power Supply Ground
H4	—	GNDA	—	Analog Ground
G4	—	V_{DDA}	—	Analog 3.3V Power Supply
H3	—	SC_VDDA	—	Smart Card PHY Power Supply
L3	—	SC_DETECT	—	Smart Card Detect
K2	—	SC_VCC	—	V_{CC} (1.8V/3V/5V) Output to Smart Card
H7	—	SC_GND	—	V_{SS} Output to Smart Card
F6	—	SC_IO	—	Smart Card I/O
J3	—	SC_RST	—	Smart Card Reset
K3	—	SC_C4	—	Smart Card C4

Pin Description (continued)

BALL	GPIO PORT NUMBER	PRIMARY FUNCTION	SECONDARY FUNCTION	FUNCTION
J4	—	SC_C8	—	Smart Card C8
L2	—	SC_CLK	—	Smart Card CLK
K1	—	MCR_1P	—	Magnetic Stripe Reader Track 1, Positive Input
L1	—	MCR_1N	—	Magnetic Stripe Reader Track 1, Negative Input
H2	—	MCR_2P	—	Magnetic Stripe Reader Track 2, Positive Input
J2	—	MCR_2N	—	Magnetic Stripe Reader Track 2, Negative Input
H1	—	MCR_3P	—	Magnetic Stripe Reader Track 3, Positive Input
J1	—	MCR_3N	—	Magnetic Stripe Reader Track 3, Negative Input
F1	—	ADC0	—	ADC Channel 0
G1	—	ADC1	—	ADC Channel 1
F2	—	ADC_VREF	—	ADC Voltage Reference
G2	—	DAC0	—	DAC Output Pin

Detailed Description

The MAX32550 is built around the ARM Cortex-M3 core, an enhanced 32-bit RISC CPU with memory protection unit (MPU). It also provides separate instruction and data AMBA AHB, interfaces connected to a multilayer AHB Matrix. The Cortex-M3 processor implements the ARMv7-M architecture instruction set. The ARMv7-M instruction set supports Thumb and Thumb-2 instructions sets as well as 1-cycle 32-bit hardware multiply operations.

Refer to the Cortex-M3 Technical Reference Manual for more details on operation of these features. This data sheet is an introduction to the primary features of the MAX32550. Detailed descriptions of the device's features can be found in the user guides and errata sheets for this product.

Memory Map

The MAX32550 memory map is contiguous from 0000 0000h to FFFF FFFFh with regions defined for different memory types. Each memory/peripheral type is entirely contained within its defined region.

The MAX32550 internal memory region contains the program and data memories for the CPU.

Internal Flash

The MAX32550 embeds 1MB of flash memory that is split in two banks of 512KB. Each bank can be reconfigured to be used upon reset through a secure selection mechanism. Furthermore the device simplifies remote firmware upgrades by ensuring that only a valid firmware is used upon boot.

The flash also features a dedicated flash acceleration engine to avoid latencies when executing code at the maximum operating frequencies.

Internal SRAM and NVSRAM

The internal system SRAM is 256KB of zero wait-state memory that is split into two banks of 128KB. Each of them is a dedicated AHB slave on the matrix, thus maximizing the on-chip bandwidth and allowing parallel data transfers.

The device also includes 8KB of battery-backed nonvolatile SRAM. This memory is provided for both secure data storage where data is automatically AES encrypted/decrypted upon access and plain data such as transaction logs where security is not a primary concern, but data endurance is. The amount of space reserved for secure and plain data is user configurable.

Data stored in the secure partition is automatically encrypted by a dedicated hardware AES-256 engine and using a random key that has been generated upon user request. This random key is stored in a dedicated 256-bit flip-flop-based secure nonvolatile key register that is automatically wiped upon triggering by one of the intrusions and environmental sensors, both internal and external. The key itself can only be read by the dedicated AES-256 engine and is not mapped on the AHB/APB buses, making it unreadable from any other system peripherals including CPU and JTAG. The block also provides a way to override the self-generated AES key with a user supplied AES-256 key.

Internal ROM and Bootloader

Upon assertion and deassertion of system reset, the Cortex-M3 is reset and begins program execution of internal ROM code at address 0x00000000. A secure bootloader is implemented to provide trusted boot, secure flash upload, flash integrity verification upon reboot, and flash bank selection.

A built-in public key authentication scheme allows secure firmware updates from both UART and USB interfaces.

The secure bootloader is configured to use parameters stored in OTP and/or NVSRAM.

Internal OTP

The internal OTP memory resides on the APB bus. A special controller is designed to read and write the bits in the OTP. The OTP offers 4KB of user storage.

AMBA AHB Bus

The MAX32550 implements a five-layer 32-bit AHB bus matrix. Arbitration between these peripherals is managed by a fixed burst arbitration scheme, wherein each master has a fixed priority.

Interrupt Controller

The MAX32550 includes the ARM nested vector interrupt controller(NVIC), providing high speed, deterministic response, interrupt masking, and multiple interrupt sources.

Features of the interrupt controller include:

- IRQ generation for each interrupt source (programmable)
- Unique vectors for each interrupt channel
- Programmable priority for each channel (8 priority levels)
- Support for nesting and preemption by higher priority interrupts
- Support for NMI (nonmaskable interrupts)

Mono LCD Controller

The LCD interface allows an external LCD to be accessed directly over the APB. This interface has the following features:

- Directly compatible with popular monochrome LCDs, text, and graphic modes
- Supports interfaces of 4-/8-bit data and 3 control
- Read and writes to external LCD-module-supported register operations
- Programmable read and write cycle times

Color LCD Controller

The color LCD controller is provided to make seamless connection to an LCD display such as active matrix TFT panels with up to 24-bit bus interface, single panel color STN panels with 8-bit bus interface, and single panel monochrome STN panels with 4-bit or 8-bit interface.

The panel resolution is programmable and the LCD controller supports a number of color modes from 1bpp to 24bpp depending on the supplied LCD panel and available frame buffer memory.

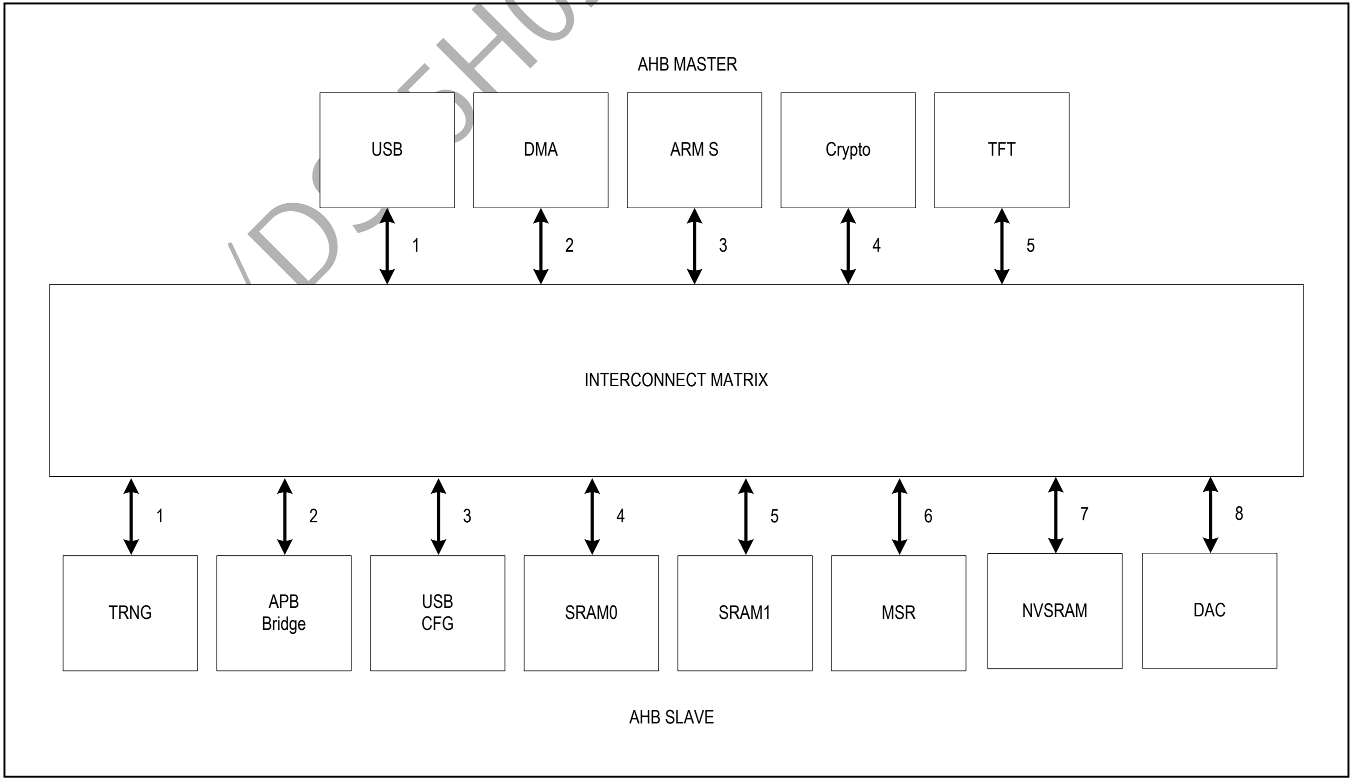


Figure 1. Buspriority

Furthermore, the controller provides the following functionality:

- Horizontal front and back porch
- Horizontal synchronization pulse width
- Number of pixels per line
- Vertical front and back porch
- Vertical synchronization pulse width
- Number of lines per panel
- Signal polarity, active high or low (LCDCLK, VSYNC, HSYNC, VDEN, LEND)
- Panel clock frequency
- Bits per pixel
- Display Type STN mono/color or TFT
- Little endian, big endian, or WinCE mode
- Interrupt generation

USB

The MAX32550 provides one USB full-speed device interface with a dedicated transceiver.

The USB device ports allows seamless connection to external USB hosts and provides a flexible endpoint management for addressing most USB classes including composite devices.

- Complies with USB specification rev. 2.0
- Supports 12Mbps and 1.5Mbps data transmission
- Integrated USB transceiver
- Programmable USB RAM for flexible endpoint configuration
- Dedicated DMA channel

DMA Controller

The DMA controller allows automatic one-way data transfer between two entities. These entities can be either memories or peripherals. The transfers are done without using CPU resources. The following transfer modes are supported:

- 4-channel
- Peripheral-to-memory
- Memory-to-peripheral
- Memory-to-memory

All DMA transactions consist of an AHB burst read into the DMA FIFO followed immediately by an AHB burst write from the FIFO.

Cryptographic Accelerator

The hardware cryptographic accelerator block is used to assist the computationally intensive operations of several common algorithms. Supported algorithms include:

- AES-128, 192, and 256 (FIPS 197)
- DES and 3DES (NIST SP800-67)
- SHA-1, 224, 256, 384, and 512 (FIPS 180-3)
- Modulo arithmetic hardware accelerator (MAA) with support up to 2048-bit DSA and ECDSA, 4096-bit (CRT) RSA

The cryptographic accelerator is configured through an APB register interface. Some of its features include:

- Integrated DMA with read ahead and write buffers for high throughput
- Support for NIST approved block modes (SP800-38A)
- Parallel calculation of block cipher and hash functions

Triple-Track Magnetic Stripe Head Interface

The magnetic stripe decoders embed a complete high-performance solution for reading and decoding 3-track magnetic stripe cards. It includes three parallel ADCs to process track data as well as filtering and decoding logic.

SPI

The Serial Peripheral Interface (SPI) is a synchronous interface allowing several SPI-compatible devices to be interconnected. SPI-compatible devices include EEPROMs, printer controllers, and contactless smart card controllers. The MAX32550 implements three independent SPI controllers for maximum flexibility. Each of the SPI controllers supports the follow features:

- Full-duplex, synchronous communication of 8-/6-bit characters
- 4-wire interface plus 3 additional slave selects
- Data transfers rates up to one-fourth the PCLK frequency
- Master mode of operation
- Dedicated baud rate generator
- 8 x 16 transmit and receive FIFOs
- Transmit and receive DMA support
- Maximum baud rate: 25 Mbps

I2C

The I2C host port is compliant with the Philips I2C standard. The I2C port is a half duplex serial port that uses two lines (data and clock) for data transmission. The MAX32550 chip provides two dedicated open-drain I/Os for the I2C bus. The I2C port can be set up as a master only. Standard 100kHz and fast 400kHz transmit modes are supported.

- I2C bus specification version 2.1 compliant (100kHz and 400kHz)
- Programmable for both normal (100kHz) and fast bus data rates (400kHz)
- Programmable for using normal addressing
- Clock synchronization and bus arbitration
- Supports arbitration in a multimaster environment
- Fully programmable slave response address
- 2 FIFOs (Rx and Tx)
- Supports I2C bus hold for slow host service
- Transfer status interrupts and flags

Smart Card Interface

The MAX32550 smart card controller embeds both the digital core and analog transceiver of the Smart Card interface. The built-in transceiver is responsible of voltage translation according to the EMV or ISO7816-1 standard and can support 1.8V and 3V cards with internal power supply and 5V cards with external 5V power supply. A bypass mode is available to use an external transceiver. The dedicated card detection input can be used to wake-up the device when in standby mode.

The ISO-7816 UART supports the following features:

- ISO/IEC 7816 standards supported
- Supports both synchronous and asynchronous cards
- 11-bit elementary time unit (ETU) counter
- 9-bit guard time counter
- 32-bit general-purpose waiting time counter
- Auto character repetition on error signal detection in transmit mode
- Auto error signal generation on parity error detection in receive mode
- Manual mode to directly drive the card IOs
- 8-level FIFO

Random Number Generator

Random numbers are the cornerstone of many security systems providing values that cannot be predicted by attackers. They prevent from replay attacks or key search approaches. The best quality random numbers come from true random number generators (TRNG) that base their source of randomness on a physical unpredictable phenomenon.

The TRNG embedded in the MAX32550 chip is designed to efficiently generate a 128-bit true random number in 128 system clock cycles. For example, only four consecutive read accesses (32-bit access) are needed to obtain a 128-bit AES random key ready for encryption. The TRNG passes NIST 800-22 and DIEHARD test suites.

Real-Time Clock (RTC)

The device includes a binary real-time clock (RTC) that keeps the time of day in absolute seconds with 1/256s resolution. The RTC operates from the V_{BAT} supply that allows it to optionally keep running even when the main digital supply (V_{CORE}) for the device is powered down. The RTC's time base is the external 32.768kHz crystal.

The MAX32550 includes a battery backup switch to automatically and safely switch between different power sources while maintaining nonvolatile SRAM content. Many mobile pin pad implementations cut the main power supply from the secure microcontroller when in stop mode. The internal battery backup switch has two dedicated input pins, V_{BAT} that connects to a traditional non-rechargeable lithium battery, and another called V_{MAIN} that connects to the main rechargeable battery through an external low drop voltage regulator. Tamper detection applies to whatever input pin is currently selected by the internal battery switch. The switch gives the priority over to the V_{MAIN} so the system drains as much current as possible from the main rechargeable battery before switching to the hard-to-replace lithium battery. It allows the end devices to be stored on shelves for long periods of time and without the fear of losing NVSRAM content because of exhausted lithium battery.

It is also possible to connect V_{MAIN} to V_{DD} to switch to the lithium battery as soon as the power is removed from the MAX32550.

The 32-bit second counter can count up to approximately 136 years and be translated to calendar format by application software. A time-of-day alarm and independent sub-second alarm can cause an interrupt or wake the device from standby mode. The independent subsecond alarm runs from the same RTC and allows the application to support interrupts with a minimum interval of approximately 3.9ms. This creates an additional timer that can be used to measure long periods of time without performance degradation.

Traditionally, long time periods have been measured using multiple interrupts from shorter interrupt intervals. Each timer interrupt required servicing, with each accompanying interruption slowing system operation. By using the RTC subsecond timer as a long-period timer, only one interrupt is needed, eliminating the performance hit associated with using a shorter timer. The device also includes a trimming feature with 1ppm resolution and can correct up to ±127ppm.

Timers/Counters/PWM

There are six 32-bit reloadable timers with four associated output pins that can be used for timing, event counting, or generation of pulse-width modulated (PWM) signals. The timers' features include:

- 32-bit reload counter
- Programmable prescaler with prescale values from 1 to 4096
- Hi-drive (8mA) PWM output generation (timer 0–3 only)
- Capture, compare and capture/compare capability
- External input pin for timer input, clock gating, or capture signal (timer 0–3 only)
- Timer output pin (timer 0–3 only)
- Timer interrupt

UART

A UART or universal asynchronous receiver-transmitter is a piece of computer hardware that translates between

parallel bits of data and serial bits. The MAX32550 embeds two UARTs. The UARTs contain a shift register that is used to convert data from a serial to a parallel form and supports the following functions:

- 8-byte FIFO
- Programmable baud rate generator up to 6Mbps
- 5, 6, 7, or 8 data bits
- 1, 1.5, or 2 stop bits
- Odd, even, or no parity
- Interrupt generation
- Supports Rx, Tx, CTS, and RTS signals

Security Monitor

The behavior of the system is constantly monitored by a range of internal and external sensors.

Internal Sensors

The internal sensors include environmental sensors such as die shield sensor, programmable temperature sensor, and battery-backed voltage sensor. Furthermore, there are core sensors monitoring internal core voltages on all rails.

Depending of the triggering source, the device might only reset or the encryption keys might be instantly wiped followed by a destructive NMI.

External Tamper Sensors

The device provides six external dynamic tamper sensors. Each external tamper sensor uses two pins (EXTS_IN, EXTS_OUT) that provide a random, changing pattern generated by an internal, true random entropy source. The two pins of an external tamper sensor can be connected to a mesh or user-defined, normally-closed tamper switch. Any mismatch on the EXTS_IN pin of a sensor pair triggers a destructive NMI after a user-configurable number of mismatches has been detected. Each pair of sensor pins generates a unique signal and can be independently enabled.

Destructive NMI (DNMI)

A DNMI is caused by triggering a tamper response or environmental out of range condition. This causes the part to instantly wipe the NVSRAM AES master key as well as other sensitive registers. In the meantime, the device triggers a nonmaskable interrupt (NMI) to allow a flexible and early answer to attack once the sensitive data is cleared (i.e., data logging). The NMI handler is user defined and stored in flash (default), but can also be re-located in SRAM. Maxim provides hardware hooks and code examples for easily erasing the flash, SRAM, and NVSRAM content by the destructive NMI routine.

Secure Keypad

The MAX32550 includes 8 I/Os that can be used by the secure keyboard controller. They are connected to a key matrix without the need for additional external components.

The keyboard controller supports the following features:

- 4 x 4 or 3 x 5 matrix
- Management of up to 16 keys
- Randomized spread-spectrum key scanning
- Debouncing feature
- Four key registers

- Push-and-release key detection features
- One-time readable key registers
- Secure scanning features
- GPIO mode
- Integrated pullup

Additional GPIO pins are available for nonsecure key scanning.

Power Management

The Power Management Unit (PMU) controls system clocking and power management. The configuration of the PMU is performed through the PMU registers.

Upon a hard reset, the PMU drives the main oscillator clock onto the system clock. All digital clock domains are enabled and most analog circuits are powered down. Various power-down modes are available for optimum system performance configuration:

- Active
- Idle with wake-up from GPIO, USB, and RTC
- Standby
- Battery backup with RTC alarm wakeup to power manager chip

Additionally, the power management unit can help reduce power consumption even further by offering the following features:

- Integrated oscillator with configurable PLL and flexible prescaler options
- Configurable dynamic CPU clock switching for frequency stepping upon system load
- Independent CPU and peripherals clock domains for slowing down CPU when performance is less required
- Individual clock gating where each peripheral's clock can be enabled and disabled on demand
- On-chip, low-frequency RC oscillator for running the CPU at ultra-low speed while maintaining some background activity

GPIO

A total of up to 70 GPIO pins are available on the device. The GPIO module enables direct I/O control of the GPIO pins. Most pins are shared with a peripheral function and can be used as GPIO when the function is unused. Though this multiplexing between peripheral and GPIO functions is usually static, it can also be done dynamically.

The primary features of the GPIO module are:

- Up to 70 GPIO pins
- Configured as input, output, or I/O
- Generate interrupt
- Interrupt generated on level or edges
- Up to four independent interrupts
- Wake the power management unit on rising/falling edge

System Reset

The MAX32550 provides following types of Reset operations:

- Hard reset
- System reset
- Peripheral reset

Hard reset: A hard reset is caused by the reset input pin, an internal power-on reset, watchdog timeout, or a tamper reset from the security module. A hard reset resets all digital modules of the device. The hard reset is asserted asynchronously by any of its sources. The hard reset is released synchronously to the CLKXI oscillator input after all reset sources have been inactive for 16 clock cycles.

System reset: A system reset is caused by a hard reset or a soft reset. A system reset resets all modules except the power management unit (PMU) and watchdog timer. A system reset is driven out onto the RSTOUT pin.

Peripheral reset: A peripheral reset is caused by a system reset or an individual peripheral reset. These signals reset APB peripherals, with the exception of the CPU, PMU, watchdog timer, and GPIO, secure access, or the external memory controller.

10-Bit ADC

The ADC is a 10-bit analog-to-digital-converter. The following features are supported:

- Two channels
- Single-shot mode
- Conversion rate 6K samples/s
- Power-down mode performing minimal power dissipation
- Programmable threshold interrupts—each channel has a high and low reading register. If any ADC reading on that channel falls outside those thresholds, and interrupt is triggered if enabled.

The ADC can operate from an external or internal voltage reference. The accuracy of conversions depends greatly on the quality of the V_{REF} voltage supplied. V_{REF} can be tied to the Analog V_{DD} for the ADC. Care should be taken to filter noise to achieve the best performance.

8-Bit DAC

The DAC is an 8-bit single-channel digital-to-analog converter. The following features are supported:

- Output sample rate control
- Data flow control interrupts- FIFO almost empty, FIFO underflow, data pattern done
- Interpolation filter to enhance dynamic performance, supporting 1:2, 1:4, and 1:8 interpolation

Watchdog Timer

A watchdog timer is used to trigger a system reset if the application fails due to a hang and does not reload the counter at regular intervals. The purpose of the watchdog is to bring the system back from a nonoperational state to normal operation. The watchdog timer can also be used as followed:

- Internal system reset on timer overflow
- Interrupt generation (IRQ) in timeout

Input clock watched by the MAX32550 security mechanisms. The watchdog supports eight (8) programmable time delay periods with prescale values from 4 to 4096. For system clock running at 108MHz, a maximum timeout delay of 37.96µs is supported.

JTAG Port

The JTAG interface is used for code loading, ICE debug activities and for control of Boundary Scan activities. The ordering information section contains unique part numbers for devices with the JTAG interface enabled or disabled. Devices with the JTAG interface enabled are used during application development and debugging. Devices with the JTAG interface disabled prevent access to the debugging interface and should be used in mass production. For more Information, refer to the Secure ROM User Guide.

Additional Documentation

Designers must have the following documents to fully use all the features of this device. This data sheet contains pin descriptions, feature overviews, and electrical specifications. Errata sheets contain deviations from published specifications. User guides contain detailed descriptions of device features and peripherals from a programming perspective.

- This MAX32550 data sheet, which contains electrical/timing specifications, package information, and pin descriptions.
- The MAX32550 revision-specific errata sheet.
- The MAX32550 User Guide, which contains detailed information and programming guidelines for core features and peripherals.

Development and Technical Support

Technical support is available at **https://support.maximintegrated.com/micro**.

Ordering Information

PART	PIN-PACKAGE	ICE
MAX32550-LNS+	121 CSBGA (8mm x 8mm, 0.65mm pitch)	No
MAX32550-LNJ+	121 CSBGA (8mm x 8mm, 0.65mm pitch)	Yes

+Denotes a lead(Pb)-free/RoHS-compliant package.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
121 CSBGA	X12188+2C	**21-0680**	**90-0451**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/14	Initial release	—
1	12/14	Revised *General Description* and *Benefits and Features* section and updated battery back mode current specs	1, 2

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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