# HN613128P, HN613128FP

### 16384-word×8-bit Mask Programmable Read Only Memory

The HN613128P/FP is a mask-programmable, byte-organized memory designed for use in bus-organized systems. To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation. The active level of the CS, OE<sub>0</sub>, OE<sub>1</sub> input and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a power-down mode.

#### FEATURES

- Fully Static Operation
- Automatic Power Down
- Single +5-Volt Power Supply
- Three-State Data Output for OR-Ties
- Mask Programmable Chip Select, Output Enable
- TTL Compatible
- Maximum Access Time; 250ns
- Low Power Standby and Low Power Operation;

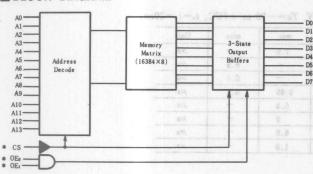
Standby:

5μW (typ.)

Operation: 50mW (typ.)

Pin Compatible with EPROM

#### ■ BLOCK DIAGRAM



#### \* Active level defined by the user.

#### **MADSOLUTE MAXIMUM RATINGS**

Item	Symbol	Value	Unit
Supply Voltage*	Vcc	-0.3 to $+7.0$	V
Input Voltage*	Vin	-0.3 to $+7.0$	V
Operating Temperature Range	Topr	-20 to +75	.C
Storage Temperature Range	Tets	-55 to +125	°C
Storage Temperature Range (under bias)	Thias	-20 to +85	°C

<sup>\*</sup> With respect to Vss.

#### ■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage *	Vcc	4.5	5.0	5.5	V
	VIL	-0.3	-	0.8	V
Input Voltage*	VIH	2.2	-	Vcc	V
Operating Temperature	Topr	-20	-	75	°C

<sup>\*</sup> With respect to Vss.

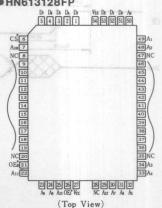
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### PIN ARRANGEMENT



#### ●HN613128FP



#### **ELECTRICAL CHARACTERISTICS** ( $V_{cc}=5.0V\pm10\%$ , $V_{ss}=0V$ , $T_a=-20$ to $+75^{\circ}$ C)

Item   Item	Symbol	Test Condition	min	typ	max	Unit
Input High-level Voltage	VIH	and the world and an analysis of the and	2.2	Se Folk	Vcc	V
Input Low-level Voltage	VIL	- He o a second annual manager of the second second second	-0.3	1 - 1	0.8	V
Output High-level Voltage	Von	$I_{OH} = -205\mu\text{A}$	2.4	1-11	1100.00	V
Output Low-level Voltage	Vol	$I_{OL}=3.2\mathrm{mA}$	articum?	Et Tuesto	0.4	V
Input Leakage Current	Iin	V <sub>m</sub> = 0 to 5.5 V	ie-iin <u>o</u> i	1-12/11	2.5	μA
Output High-level Leakage Current	ILOH	$V_{out} = 2.4 \text{V}, \text{CS} = 0.8 \text{V}, \overline{\text{CS}} = 2.2 \text{V}$	GINE <u>L</u> n	ALTER DA	10	μA
Output Low-level Leakage Current	ILOL	$V_{out} = 0.4 \text{V, CS} = 0.8 \text{V, } \overline{\text{CS}} = 2.2 \text{V}$	(D)(D)	ugai a	10	μΑ
Supply Current (Active/Standby)	Icc/ I.	$V_{cc} = 5.5 \text{V}, I_{DOUT} = 0 \text{ m A } /\overline{\text{CS}} \ge V_{cc} - 0.2 \text{V,CS} \le 0.2 \text{V}$	माक्ष क्या	10/1	25/30	mA/µA
Input Capacitance	Cin	$V_{in} = 0 \text{ V}, f = 1.0 \text{ MHz}, Ta = 25^{\circ}\text{C}$	RG 940	31/45 1	10	pF
Output Capacitance	Cout	$V_{in} = 0 \text{ V}, f = 1.0 \text{ MHz}, Ta = 25^{\circ}\text{C}$	-	-	15	pF

<sup>\*</sup> Steady state current

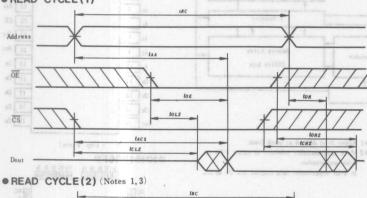
#### ■ RECOMMENDED AC OPERATING CONDITIONS (READ SEQUENCE)

 $(V_{cc}=5.0V\pm10\%, V_{ss}=0V, T_a=-20 \text{ to } +75^{\circ}\text{C}, \text{All timing with } t_r=t_f=20 \text{ ns})$ 

	6 1 1	HN61	3128P	ension.	
Item	Symbol	min	max	Unit ylongus se voc. V.d. elgania A	
Read Cycle Time	trc	250	CANTHER TO DOS	ns notigenerate tawog wo.	
Address Access Time	taa	_	250	ns (.qy) Wyd ydbnafa	
Chip Select Access Time	tacs	- 1	250	ns sidheqmon JTI	
Chip Selection to Output in Low Z	tcLZ	10	_	ns Marry 21, C.C. termin areas A	. 0
Output Enable to Output Valid	toE	_	100	ns	
Output Enable to Output in Low Z	toLz	10		ns DAGADAIG NOOL	
Chip deselection to Output in High Z	tcHZ	0	100	ns	
Chip Disable to Output in High Z	toнz	0	100	ns	
Output Hold from Address Change	tон	10		ns	

#### **TIMING WAVEFORM**

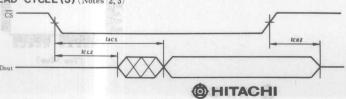
#### • READ CYCLE (1)



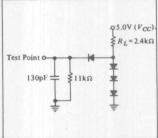
### • READ CYCLE (3) (Notes 2, 3)

Address

Dout



#### AC TEST LOAD



Notes) 1.  $t_r = t_f = 20 \text{ ns}$ .

- C<sub>L</sub> includes jig capacitance.
  All diodes are 1S2074<sup>®</sup>.

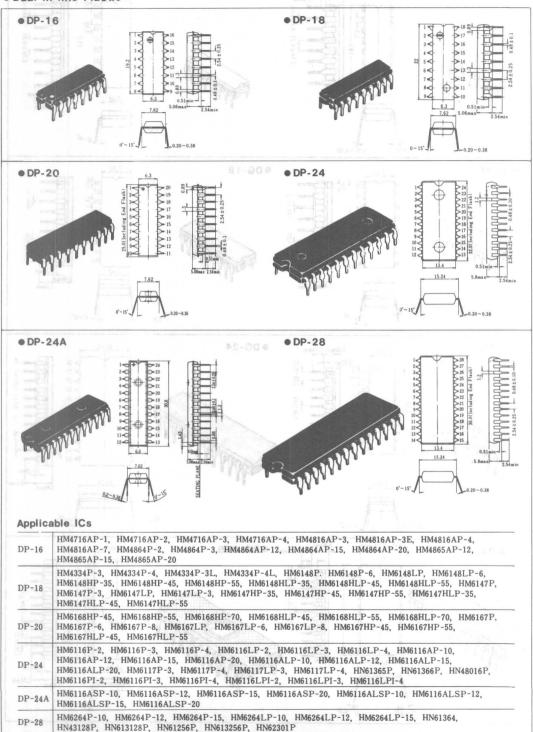
#### NOTES:

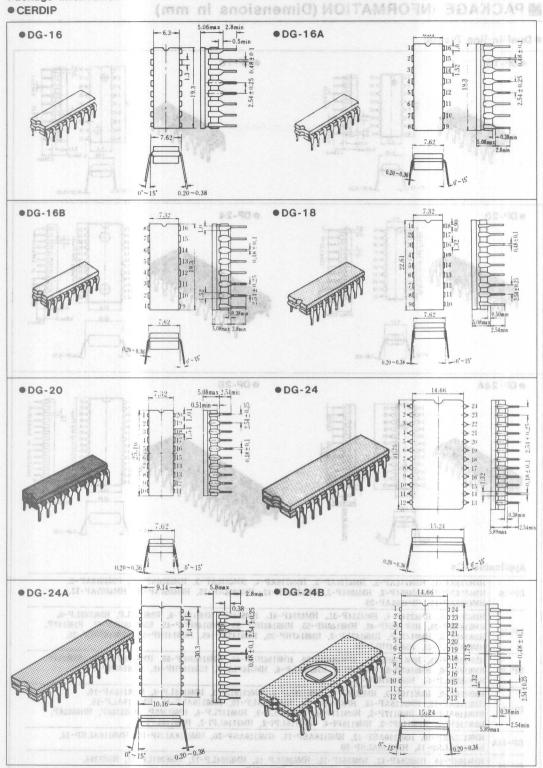
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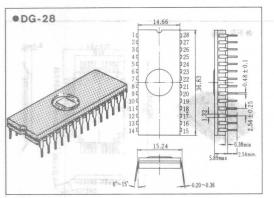
- 1. Device is continuously selected.
- 2. Address Valid prior to or coincident with CS transition low.
- 3.  $\overline{OE} = VIL$ .

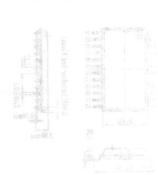
### ■ PACKAGE INFORMATION (Dimensions in mm)

#### Dual-in-line Plastic



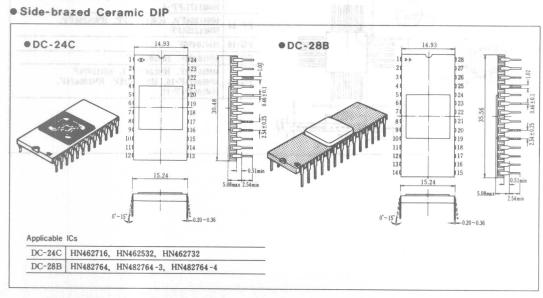




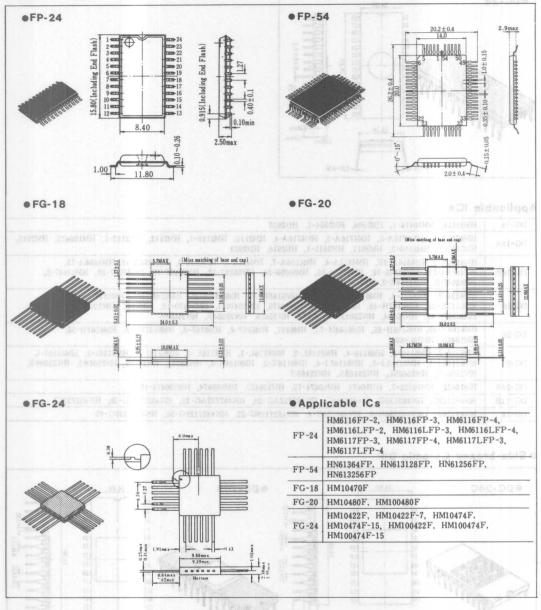


#### Applicable ICs

DG-16	HM10414, HM10414-1, HM2504, HM2504-1, HD2912
DG-16A	HM4716A-1, HM4716A-2, HM4716A-3, HM4716A-4, HM2110, HM2110-1, HM2112, HM2112-1, HM100415, HM2510-1, HM2510-2, HM2511, HM2511-1, HD2916, HD2923
DG-16B	HM4816A-3, HM4816A-3E, HM4816A-4, HM4816A-7, HM4864-2, HM4864-3, HM4864A-12, HM4864A-15, HM4864A-20, HM50256-12, HM50256-15, HM50256-20, HM50257-12, HM50257-15, HM50257-20, HM4864I-2, HM4864I-3, HM4864K-2, HM4864K-3
DG-18	HM4334-3, HM4334-4, HM6148, HM6148-6, HM6148H-35, HM6148H-45, HM6148H-55, HM6147, HM6147-3, HM6147H-35, HM6147H-45, HM6147H-55, HM10470, HM10470-1, HM10470-15, HM2142, HM100470, HM100470-15, HN25044, HN25045, HN25084, HN25085, HN25084S, HN25085S
DG-20	HM6168H-45, HM6168H-55, HM6168H-70, HM6167, HM6167-6, HM6167-8, HM6167H-45, HM6167H-55, HM10480, HM100480
DG-24	HM6116-2, HM6116-3, HM6116-4, HM6116L-2, HM6116L-3, HM6116L-4, HM6116I-2, HM6116I-3, HM6116I-4, HM6116LI-2, HM6116LI-3, HM6116LI-4, HM6116K-3, HM6116K-4, HN25088, HN25089, HN25089S, HN25089L, HN25089L, HN25169S
DG-24A	HM10422, HM10422-7, HM10474, HM10474-15, HM100422, HM100474, HM100474-15
DG-24B	HN462716G, HN462532G, HN462732G, HN482732AG-20, HN482732AG-25, HN482732AG-30, HN462732GI
DG-28	HN482764G, HN482764G-3, HN482764G-4, HN4827128G-25, HN4827128G-30, HN4827128G-45



#### • Flat Packages



#### • Leadless Chip Carrier

