**Laboratory 02.1.- “Equivalence Checking with Yosys vs Conformal”**

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# Objective

Compare FPGA implementation from Vivado and Yosys, using sequential equivalence checking.

# Material

1. PC
2. SEDA tool, FPV App
3. Vivado Formal Equivalence Checking Libraries

# Practical development

* **Description:** Cadence Conformal tool can perform gate-to-gate and RTL-to-RTL equivalence checking of Vivado's synthesized netlists in pre/post synthesis and post place-and-route mode, using xeclibs. For example, the following module can be formally verified (equivalence checking) with conformal as follows:
* Define a simple counter such as the following one, synthesize it with Vivado, and Yosys. Write a post synthesis Verilog netlist (write\_verilog ...).



* Rename your files in a way that you can identify, such as top\_vivado\_syn.v and top\_yosys\_syn.v.
* Create two files, golden.vc and revised.vc. The former will call the Vivado synthesized design, with the xeclibs for LEC. The latter, will do the same, but using Yosys netlist instead:

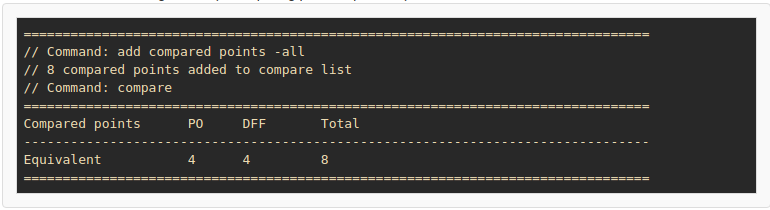




* Create a **dofile** conformal script, to setup a LEC project using golden.vc as golden, and revised.vc as revised model:



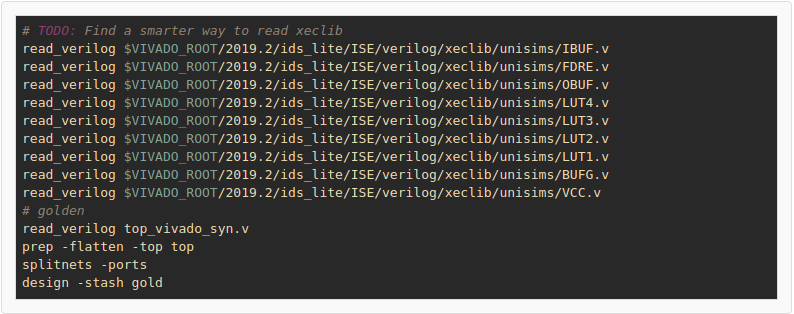
* Lastly, call conformal with the **dofile** script, and watch the results: **$CONFORMAL\_ROOT/bin/lec -d dofile -L**
* You should see something as this (4 comparing points equivalent):



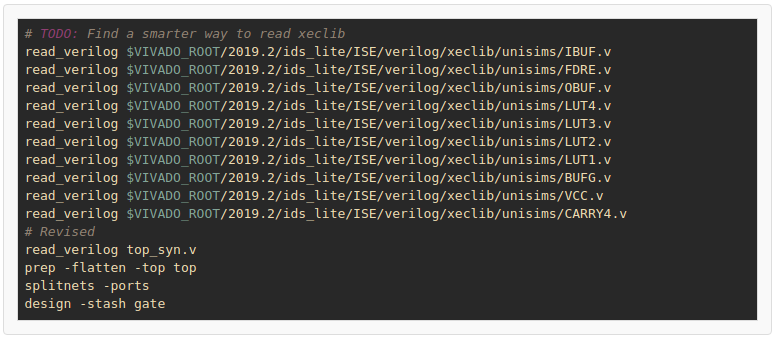
## Yosys

The xeclibs can be used in exactly the same way as with Conformal, to do gate-to-gate equivalence checking between netlists. The process is similar until the point of getting both post synthesis Verilog files. After this step, the setup script of Yosys needs to:

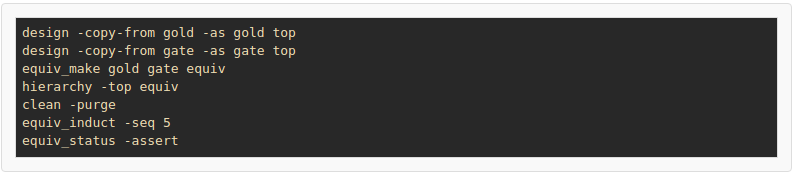
* Read the xeclibs and golden (Vivado) netlist:



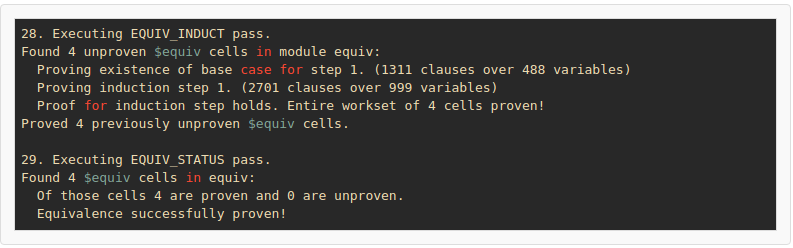
* Read the xeclibs and revised, or gate (Yosys) netlist:



* Perform equivalence checking between gold and gate netlist:



* You should see something as this, which means the same 4 comparing points are proven.



***Grade yourself:*** In Yosys, there is a “**show**” command that will show the schematic of the current cells in the design.

* Use the command to open an schematic.
* Trace back the golden cells.
* Trace back the revised (or gate) cells.
* Describe how the equivalence is performed.

# Conclusions

After completing this lab, you will be able to understand how to interface with Symbiotic EDA tool for Formal Property Verification, and had a glance of how those flows looks like. Hopefully you can understand some of it usefulness, not only when verifying circuits, but also when modelling them.