Physical OPERAND  Addrew  Addrew  SEGMENT	1		<del>,</del>	-			
PHYSICAL MEMORY  POINTER Selector Offset  Physical OPERAND  PSECRIFTOR  PSECRIFTOR  PSECRIFTOR  TABLE  Segment Rose  Address  Address  Address  To support the concept of unitual memory & memory in allotted per trask.  The virtual memory is allotted per trask.  The orderess up to 1 G.B. of virtual memory per trask.  Complete virtual memory of is mapped onto the 16 MB physical memory i.e. if program is larger than 16 MB is structure on board disk & is to be executed.  The segments are associated with a data structure called a descriptory.		19UCS122		15			
PHYSICAL MEMORY  Physical Offset  Physical Offset  Physical Operand  Pescriptor  Segment  Descriptor  TABLE  Segment Rose  Address  Address  Physical Memory operand  Descriptor  Trable  Segment Rose  Address  Address  The unitual memory of support the concept of  Unitual memory of memory memory operands  The unitual memory of support memory operands  Complete unitual memory of support makes  Physical memory is if program is larger than 16 mB is  Struct on based disk & is to be executed.  The segments are associated with a data structure called a  descriptor.	02.	Draw & explain Protected virtu	al addressing mode	(PVAM) of			
Physical Offset  Physical Operand  Segment Base  Segment Base  Rodress  Rod		80086 Microprocessor					
Physical OPERAND  Physical OPERAND  Address  Address  SEGMENT  DESCRIPTOR  TABLE  Segment Base  Address  Addres	$\longrightarrow$	PHYSICAL INCINORY					
Physical OPERAND  Physical OPERAND  Address  Address  SEGMENT  DESCRIPTOR  TABLE  Segment Base  Address  Addres		Colorby Office					
Physical OPERAND  Addrew Addrew Addrew Addrew  SEGMENT DESCRIPTOR  Segment Raise Addrews  Add		Pointer Selector Uniter					
Physical OPERAND  Addrew  Addrew  Addrew  Addrew  SEGMENT  DESCRIPTOR  TABLE  Segment Race  Addrews  Addrews  The virtual memory & management  The virtual memory is allotted per truk.  The addrew up to 1 GB of virtual memory per talk.  Complete virtual memory of is mapped onto the 16 MB physical memory i.e. if program is larger than 16 MB is to be executed.  The segments are associated with a data structure called a descriptor.							
Physical OPERAND  Addrew  Addrew  Addrew  Addrew  SEGMENT  DESCRIPTOR  TABLE  Segment Raise  Addrews	-						
Physical OPERAND  Addrew  Addrew  SEGMENT  DESCRIPTOR  TABLE  Segment Base  Addrews  Addrews  The Virtual memory is calletted per truk.  The virtual memory is calletted per truk.  The addrew up to 1 GB of virtual memory per truk.  Complete virtual memory et a mapped anto the 16 mB physical memory i.e. if program is larger than 16 mB is stored on hard disk & is to be executed.  The segments are associated with a data structure called a descriptor.			·	SEGMENT			
Physical OPERAND  Addrews  SEGMENT  DESCRIPTOR  TABLE  Segment Base  Addrews  Addrews  The virtual memory is calleted par truk.  The virtual memory is alleted par truk.  The addrews up to 1 GB of virtual memory per task.  Complete virtual memory et is mapped anto the 16 mB physical memory i.e. if program is larger than 16 mB is stored on hard disk & is to be executed.  The segments are associated with a data structure called a descriptor.	-		MEMORY				
SEGMENT  SEGMENT  DESCRIPTOR  TABLE  Segment Base  Address  Address  The Nixtual memory is collected per task.  The address up to 1 GB of virtual memory per task.  Complete virtual memory as mapped anto the 16 MB  physical memory i.e. if program is larger than 16 MB is stored on basel disk is to be executed.  The segments are associated with a data structure called a descriptor.	-		OPERAND				
SEGMENT SEGMENT DESCRIPTOR TABLE  Segment Raise Address  Address  - 80296 is the first processor to support the concept of virtual memory & memory managinant.  - The virtual memory is allotted per trusk.  - The address up to 1 GB of virtual memory per trusk.  - Complete virtual memory of is mapped anto the 16 MB physical memory i.e. if program is larger than 16 MB is stayed on hard disk & is to be executed.  - The segments are associated with a data structure called a descriptor.							
Segment Rais  Segment Rais  Address  - 802.96 is the Piret processes to support the noncept of virtual memory & memory management.  - The virtual memory is allotted per task.  - The address up to 1 GB of virtual memory per task.  - Complete virtual memory of is mapped onto the 16 MB physical memory i.e. if program is larger than 16 MB is stored on hard disk & is to be executed.  - The agaments are associated with a data structure ralled a descriptor.		Hoder		<del>  )                                   </del>			
Segment Rose  - 80286 is the first processor to support the concept of virtual memory & memory management.  - The virtual memory is allotted per task.  - It arbitres up to 1 GB of virtual memory per task.  - Complete virtual memory of is mapped onto the 16 MB physical memory i.e. if program is larger than 16 MB is stored on basel disk & is to be executed.  - The segments are associated with a data structure called a descriptor.							
Segment Base  Address  - 80286 is the first processor to support the concept of virtual memory & memory management  - The virtual memory is allotted per task.  - The address up to 1 GB of virtual memory per task.  - Complete virtual memory of is mapped onto the 16 mB  physical memory i.e. if program is larger than 16 mB is stored on based disk & is to be executed.  - The segments are associated with a data structure called a  descriptor.			SEGMENT	DESCRIPTOR			
Address  - 80286 is the first processor to support the concept of virtual memory & memory management.  - The virtual memory is allotted per task.  - It address up to 1688 of virtual memory per task.  - Complete virtual memory of is mapped anto the 16 mB physical memory i.e. if program is larger than 16 mB is stored on hard disk & is to be executed.  - The segments are associated with a data structure ralled a descriptor.	~ <u>.</u>		DESCRIPTOR	TABLE			
- 80286 is the first processor to support the concept of virtual memory & memory management  - The virtual memory is allotted per task.  - It address up to 1 GB of virtual memory per task.  - Complete virtual memory et is mapped onto the 16 mB  physical memory i.e. if program is larger than 16 mB is stored on based disk & is to be executed.  - The segments are associated with a data structure ralled a  descriptor.				/			
virtual memory & memory management.  The virtual memory is allotted per task.  The address up to 1 GB of virtual memory per task.  Complete virtual memory of is mapped onto the 16 mB physical memory i.e. if program is larger than 16 mB is stored on based disk & is to be executed.  The segments are associated with a data structure called a descriptor.		Address					
virtual memory & memory marriament.  The virtual memory is allotted per task.  The address up to 1 GB of virtual memory per task.  Complete virtual memory of is mapped anto the 16 mB physical memory i.e. if program is larger than 16 mB is stored on hard disk & is to be executed.  The segments are associated with a data structure called a descriptor.							
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The virtual momony is allotted per truk.  The address up to 1 GB of virtual memory per task.  Complete virtual memory of is mapped onto the 16 mB physical memory i.e. if program is larger than 16 mB is stored on basel disk & is to be executed.  The segments are associated with a data structure called a descriptor.							
- The address up to 1 GB of virtual memory per task.  - Complete virtual memory of is mapped anto the 16 MB  physical memory i.e. if program is larger than 16 MB is  - stored on hard disk & is to be executed.  - The segments are associated with a data structure called a descriptor.							
- Complete virtual memory of is mapped onto the 16 MB  physical memory i.e. if program is larger than 16 MB is  stored on basel disk & is to be executed.  The segments are associated with a data structure called a descriptor.		, ,	•				
physical memory i.e. if program is larger than 16 MB is stored on hard disk & is to be executed.  The segments are associated with a data structure called a descriptor.	i.	- The address up to 1 GB of Vin	rtual memory per-	talk.			
		- Complete virtus memory of	is mapped onto	the 16 MB			
The segments are associated with a data structure called a descriptor.		physical memory i.e. it progra	m is larger than	16 MB 18			
descriptor							
- The descriptor contains informat of the segment.							
- The CAPACHIPAT CONCARIA OF THE SEGMENT.		description contains inform	noth on the server	4			
		- IN CREATIFIED CONTINUE APPOINT	D we segmen				

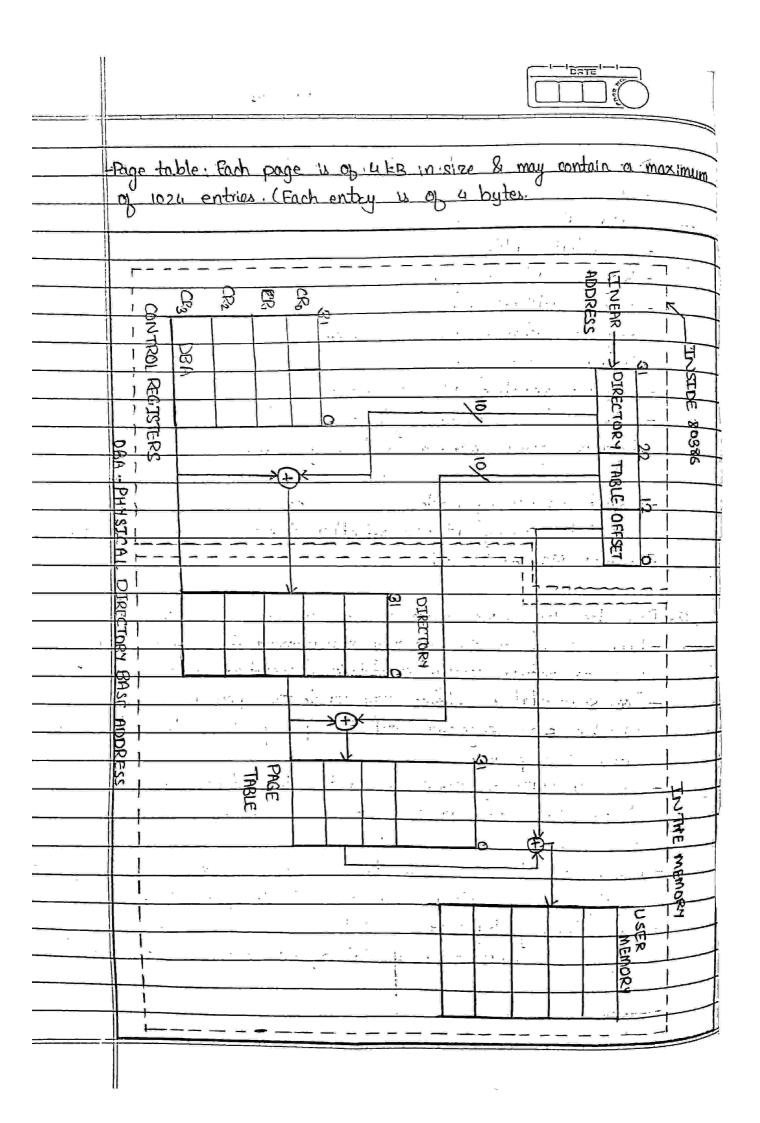


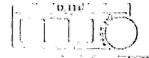
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	TIVOUTA
	- In PVAM 80286 wer 16 bit segment register as a selector to
	address a derriptur stored in physical memory.
	- Descriptur includes house address segment limit, segment type
	privilege level, segment availability in physical mamory.
	- The segment base address is see but that addresses first location
	in that segment
	- 24 bit segment base address is added with is bit offset to
	calculated 24 bit physical adoless.
	- Maximum segment size will be 64kB.
	- 80086 back to its real address made is by resolting the system.
<u>Q3</u> .	In the real mode, Show the starting & ending addrewing of ead segment tocated by the following segment reguler values
a.	2315H
	Starting address = Segment register XIOH + Offset
	= 2347×10H +0000H
	= 23450 H
	Enling address = Segment register XIDH + offset
-	- 2347XIDH + FEFFH
	- 3344FF H
b	ABCOH - Francisco de la companya de
-	Starting address = ABCDXIDH +0000H
	- ABCDO'H
	- 1 der token by the street of
	Ending address = ABCDXIOH + EFFFH
	= BBCCF H

			CATE				
	19UCS122						
C	7899H	* :	.5				
r - 1	Starting address = -88		DH				
~	= 88990 H						
~							
~	Ending address = 8899×10H + FFFFH						
·	- 9898F H						
<del></del>		a. 1-					
OV <sub>1</sub> .	Write a short note	on Flox	mode momozy.				
<u>-</u>			S SPACE C				
· · · · · · · · · · · · · · · · · · ·			FEFFFFFF				
~							
		-					
			-				
	line to the		49				
m	Cooperages		0 00 00 F0 00 0				
×			4 - 3 - 3 - 3 - 3 - 3 - 3 - 3 - 3 - 3 -				
·							
<u> </u>			111 Si ba				
			<u> </u>				
		· ·					
`			000000000				
	10.00						
	A flat made memory system in one which there is no segment?						
•	The address of first byte in memory at connoconoun & lat location is FFFFFFFFF (Address size = 40 bits)						
	- That flat morbel abors not use segment register to address a						
	locat in a memory						
	- This form of addressing is much easier to understand but offer						
	little protection to the system.						
	l						

	=
or Describe different data addressing modes with one instruct	_
example.	-
-> Data Addressing Mode	_
- Immediate addrewing mode	_
- Register achillressing mode	
- Direct addressing mode	_
- Register inclinent achirossing mode.	_
-Index addressing mode	_
- Régister relative addressing monte	-
- Based indexed addrewing mode	-
- Relative based indexed addressing mode.	_
	-
- Direct anthrewing mode	_
16 bit memory address (affect) is directly specified in instruct	<u>)</u>
Example: MOV AX, C2000]	<del></del> ;
as Describe Paging Mechanism in 80386 Microprocessor with rest diagram	<u>a-</u>
-> Paging is one of the memory management techniques	
used for virtual memory-multitasking operating system.	
The segmentation scheme may clivide the physical memory into	_
variable size segments but the paging divides the mamony into	<u> </u>
	<del></del> ,
- Paging unit: PU of 80386 was a two level table mechanism to convert the linear addresses provided by SU into physical	
addresses.	_
- Paging unit handles every task in terms of these three componer	ф —
namely page directory, page tables & the page itself.	
- Paging directory: This is at the most 4 kB in size & each directory	
entry is of 4 bytes, thus a total of 1024 entries are allowed in a	
directory.	
н	





- For converting linear addresses to physical addresses, if the conversion process uses the two levels paging for every conversion, a considerable time will be wasted in the process. - To aptimize this, a as entry page table cache is provided which stores the 32 recordly account page table entrus. - Whenever a linear address is to be converted to physical address, it is first checked to see whether it corresponds to any of the page table eache is also known as TLB. logical address CPU number number TLB hut Physical octobres TLB TLB miss Physical memory Page table