

# Advanced Microprocessor (CSL211)

Unit1 Microprocessor architecture

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# Register organization of 8086

## 1. General data registers

- ❖ AX,BX,CX and DX are general purpose data register. Letter X is used to specify complete 16 bit register
- ❖ Register CX is used as a default counter in case of an loop instructions
- ❖ AX is used as an accumulator.

## 2. Segment registers

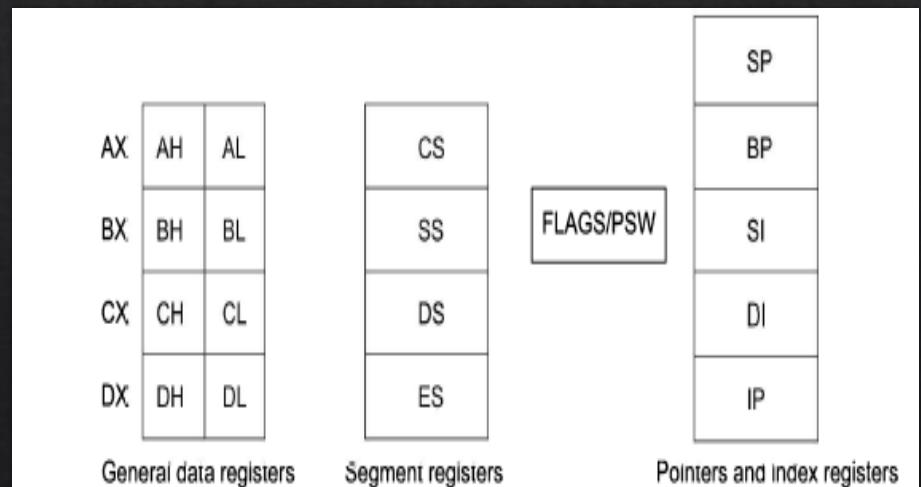
- ❖ 8086 addresses segmented memory. Complete 1MB memory is divided into 16 logical segments
- ❖ Each segment contain 64 KB of memory.
- ❖ There are four segment registers CS,DS,ES,SS
- ❖ CS: code segment of the memory where all executable program is stored.
- ❖ DS: data segment of the memory where the data is resided.
- ❖ ES: is a segment which is another data segment of the memory.
- ❖ SS: is a segment which is used to store stack data.

## 3. Flag register

- ❖ It indicate result of the computations in the ALU

## 4. Pointer and Index registers

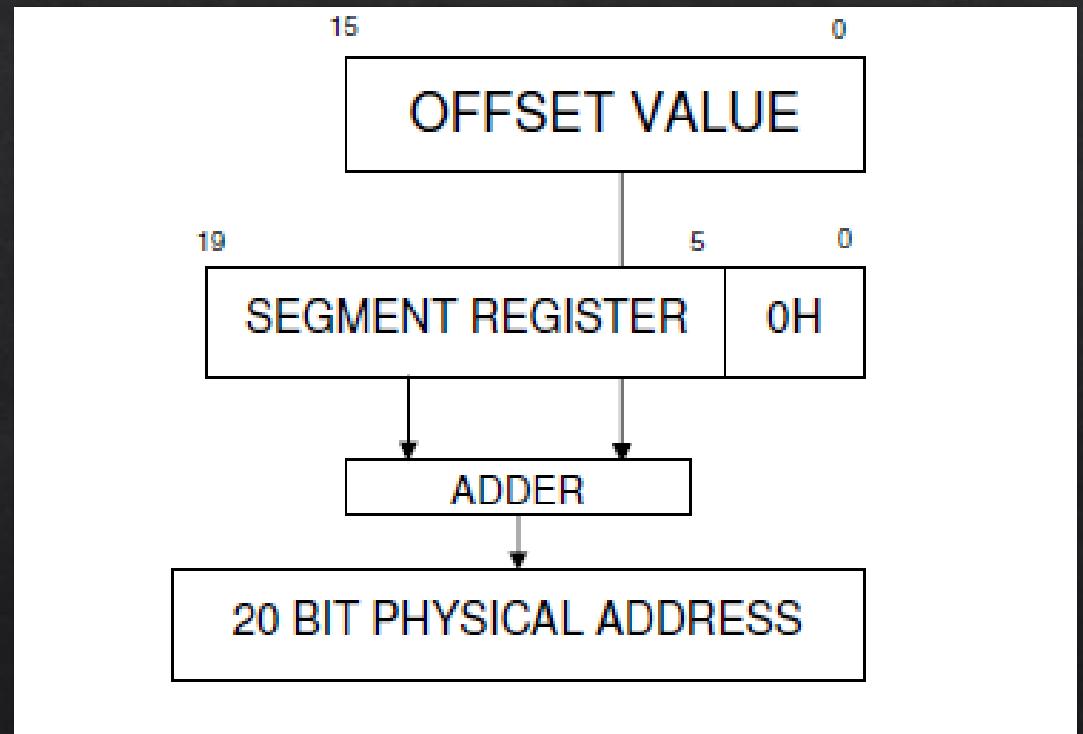
- ❖ Pointers contain offset within the particular segments. Index registers are used as general purpose registers as well as for offset storage.
- ❖ SI is used to store offset of source data in data segment while DI is used to store offset of destination data in extra segment



# Physical address formation

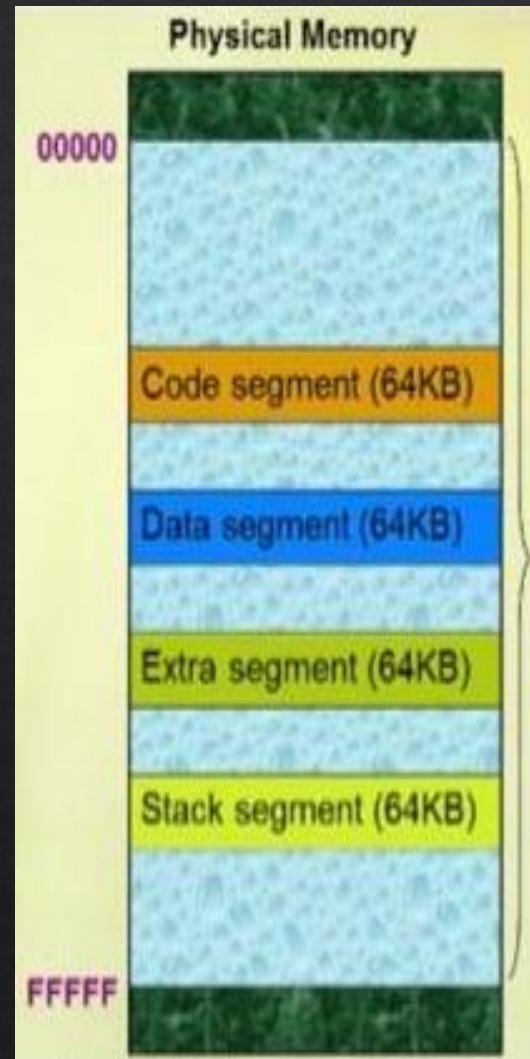
Physical address = Segment register \* 10H + Offset register

Segment address	$\rightarrow 1005H$
Offset address	$\rightarrow 5555H$
Segment address	$\rightarrow 1005H \rightarrow 0001\ 0000\ 0000\ 0101$
Shifted by 4 bit positions	$\rightarrow 0001\ 0000\ 0000\ 0101\ 0000$
	+
Offset address	$\rightarrow 0101\ 0101\ 0101\ 0101$
Physical address	$\overline{\rightarrow 0001\ 0101\ 0101\ 1010\ 0101}$
	1    5    5    A    5



# Memory segmentation

- ❖ Memory in 8086 is organized as segmented memory.
- ❖ 16 bit contents of segment register points to starting location of a particular segment. To address a specific memory location within a segment, we need an offset. Offset address is also 16 bit ranging from 0000H to FFFFH
- ❖ Physical addresses range from 00000H to FFFFFH.
- ❖ Advantages of segmented memory scheme.
  - ❖ Allow memory capacity 1MB though actual addresses are 16 bits.
  - ❖ Allow placing of code ,data and stack portion of same program in different segments.
  - ❖ Permit program and its data to put into different area of memory each time program is executed.



# Flag register of 8086

- ❖ 8086 has 16 bit flag register divided into two parts: status flags and control flags
- ❖ **Trap flag** : IF this flag is set , the processor enters the single step execution mode. A trap is generated after execution of each instruction.
- ❖ **Interrupt flag**: if this flag is set mask able interrupts are recognized by the CPU.
- ❖ **Direction flag**: this is used for string manipulation
  - ❖ If this flag is reset string is processed from lowest to highest address.
  - ❖ If this flag is set string is processed from highest to lowest address.
- ❖ **Overflow flag**: this flag is set if an overflow occurs. If the result of signed operation is larges enough to be accommodated in a destination register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	O	D	I	T	S	Z	X	Ac	X	P	X	Cy

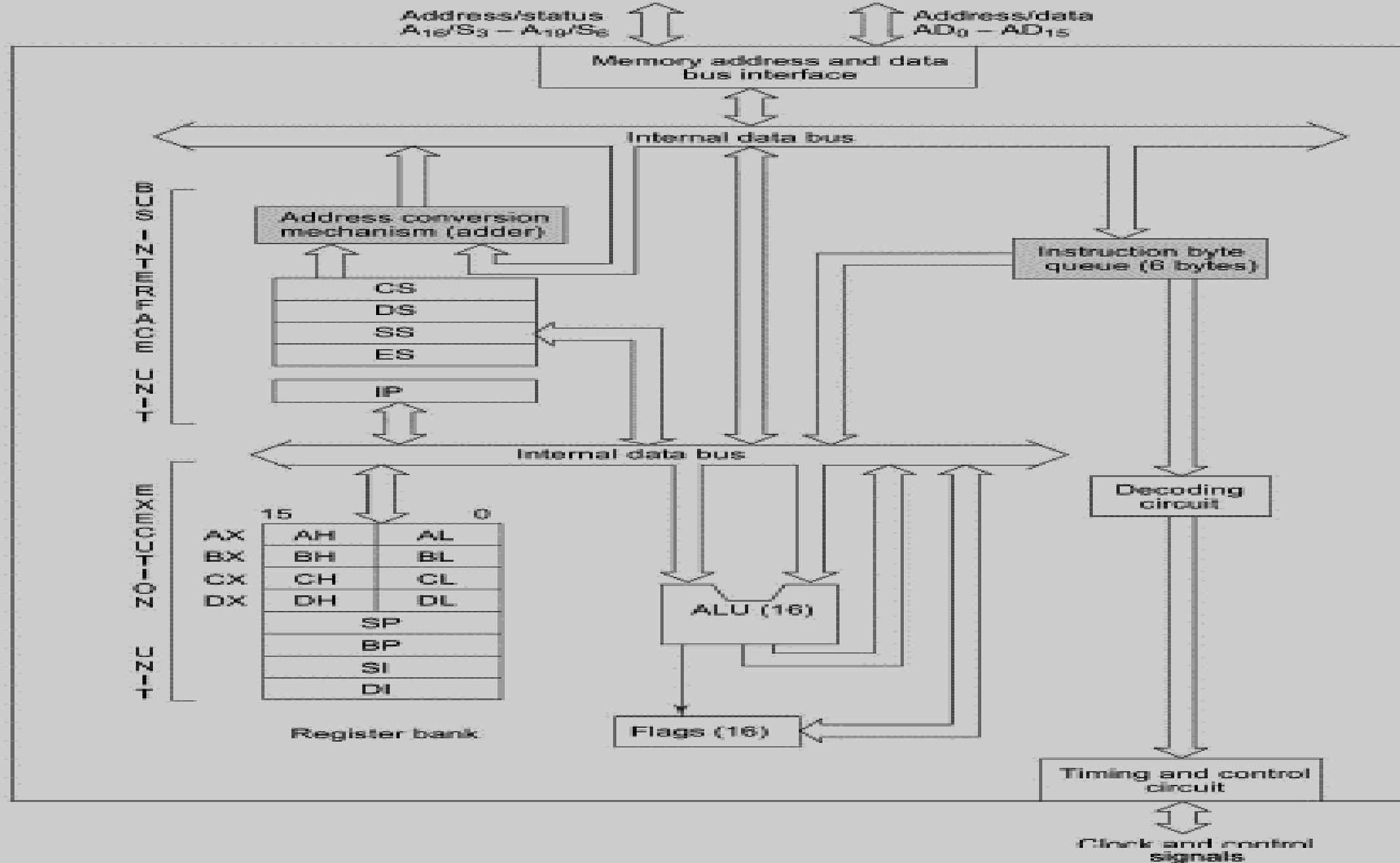


Fig. 1.2 8086 Architecture

# 8086 Architecture

Complete architecture of 8086 microprocessor is divided into two parts

## BIU

- It contain circuit for physical address calculation and pre decoding instruction byte queue.(6 Byte Queue)
- This unit is responsible for establishing communications with external devices and peripherals including memory.
- Complete physical address 20 bit is generated using segment register and offset registers, each 16 bit long.

## EU

- It contain register set of 8086 except segment registers and IP
- It has 16 bit ALU to perform Arithmetic and logical operations
- The decoding unit decodes opcode bytes issued from the instruction byte queue.
- Timing and control unit issue necessary control signals to execute the instruction opcode received from instruction byte queue.
- The EU pass the result to BIU for storing them in memory.

Hint :Size of largest instruction in 8086 is 6 byte therefore instruction byte queue is 6 byte

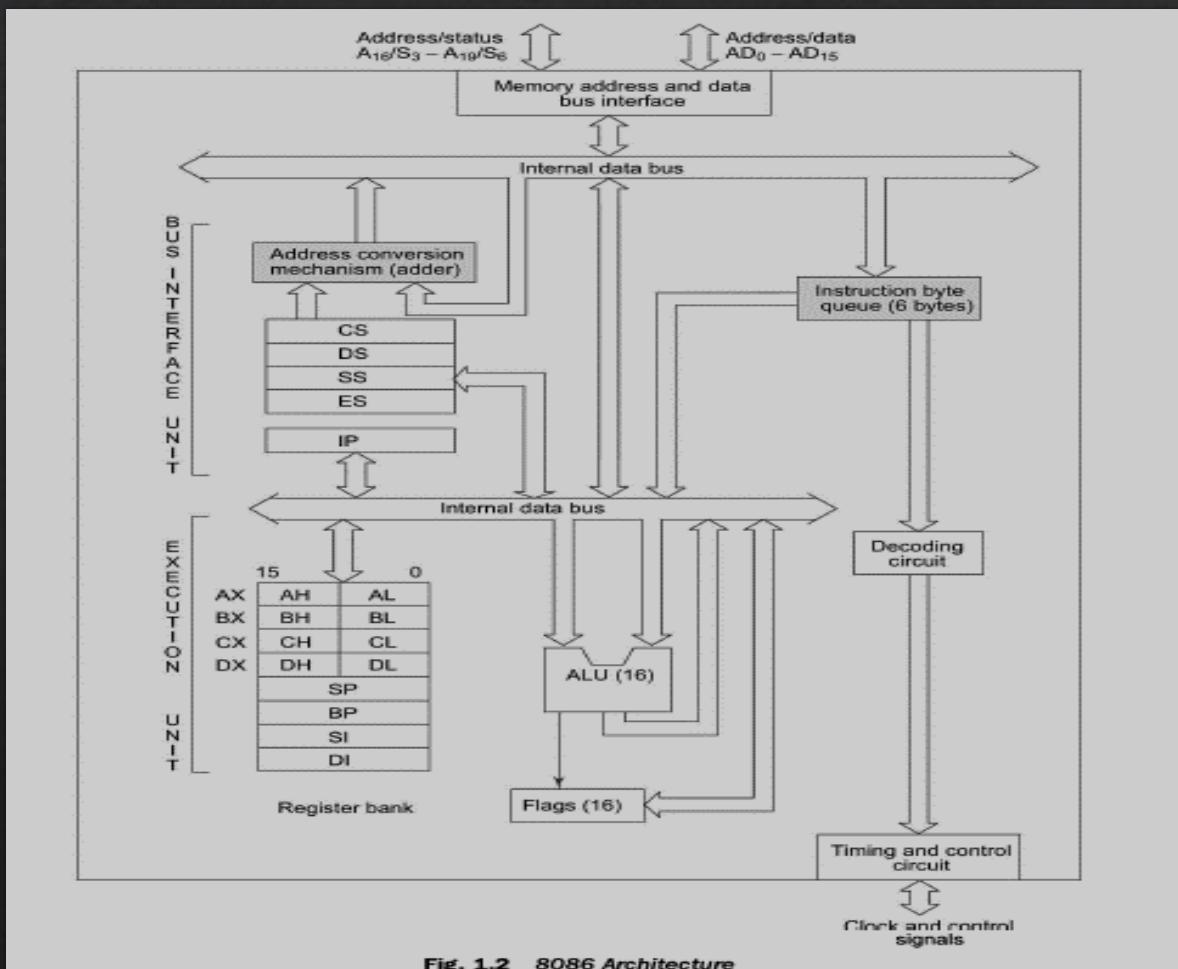
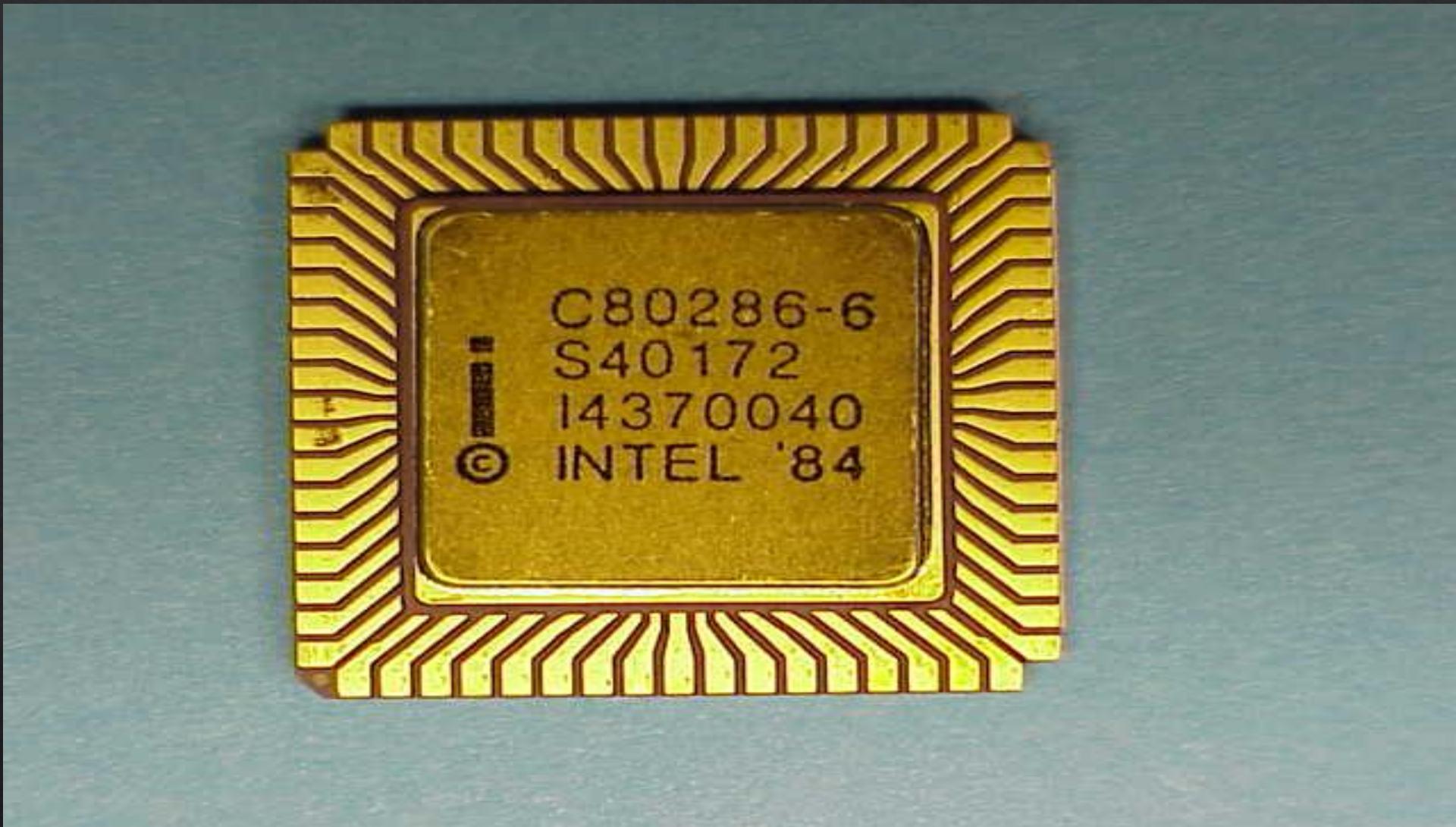


Fig. 1.2 8086 Architecture

# Let's us start Intel 80286 Microprocessor.



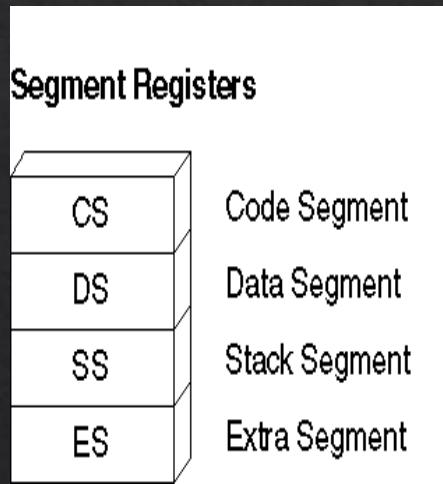
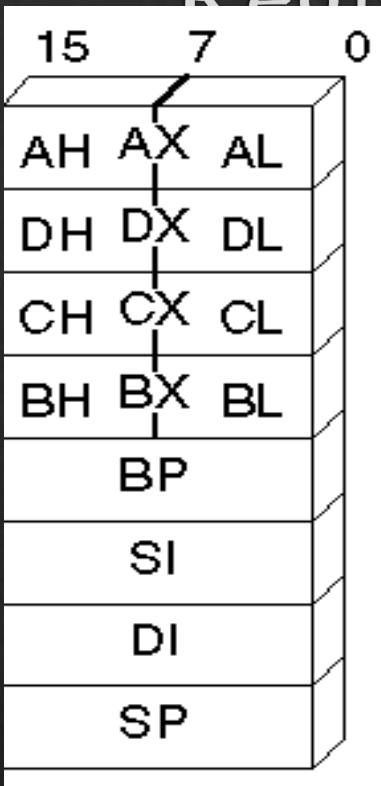
# Features of 80286

- ❖ 16 bit processor
- ❖ 24 bit address lines so access up to  $2^{24}=16$  MB of physical memory.
- ❖ Operated at different clock speeds 4 MHz,6MHz,8Mhz.
- ❖ Enhanced instruction set
- ❖ 68 pin leadless flat package
- ❖ Upward compatible with 8086.
- ❖ It supports a pipelined architecture.

# Features of 80286

- ❖ Supports two operating modes
  - ❖ Real addressing mode
  - ❖ Protected addressing mode.
- In real mode ,80286 behaves as a fast 8086
- In protected mode ,80286 can address up to 1gb of memory.
- Provide memory management and protection circuitry
- It supports multiuser and multitasking environment
- It execute instruction in fewer clock cycles than 8086.

# Register organization of 80286

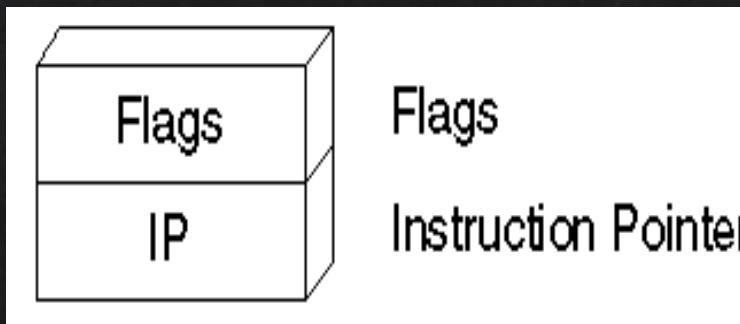


- ◆ 8, 16 bit general purpose registers

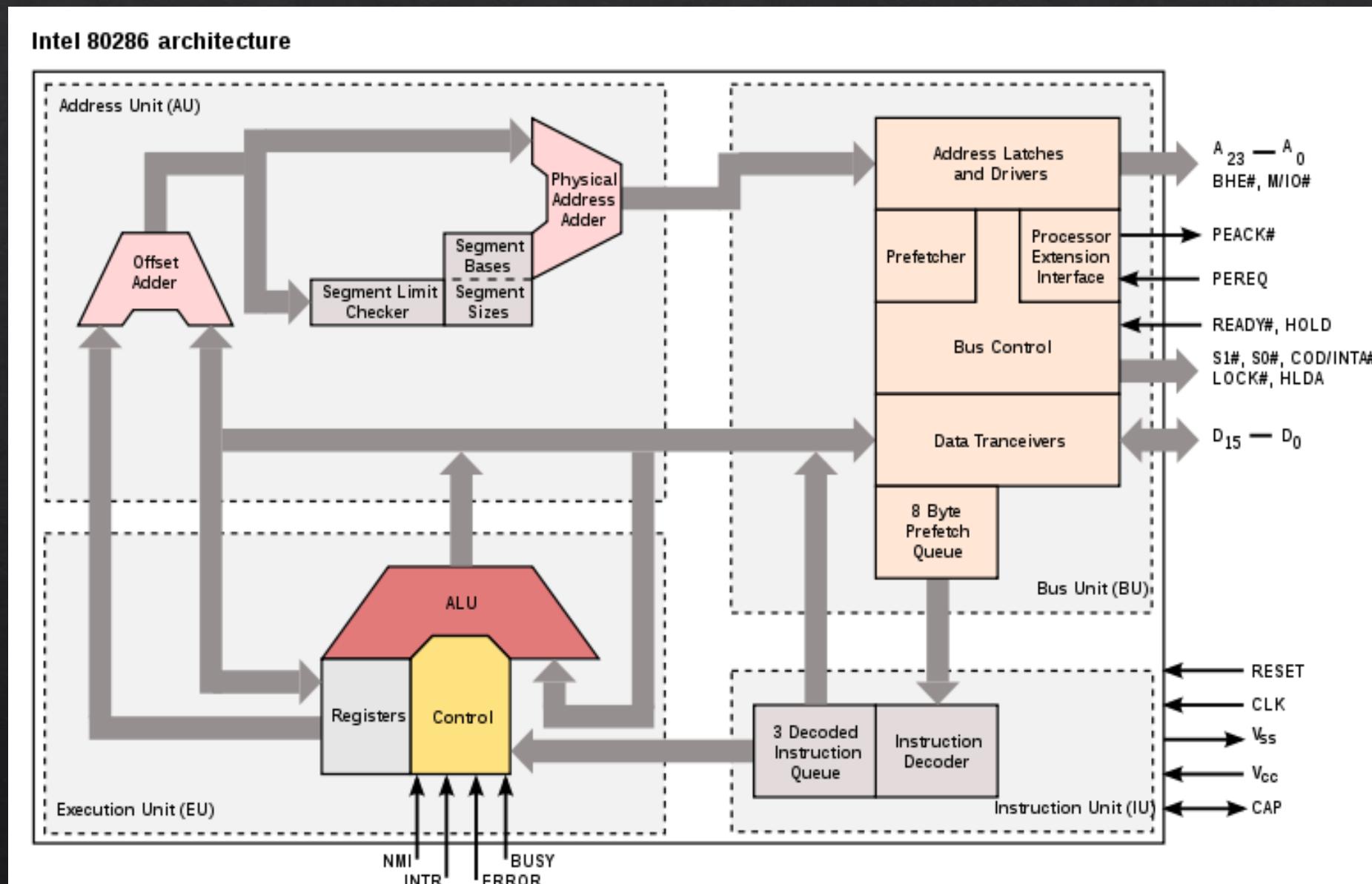
- ◆ 4, 16 bit segment registers

- ◆ Status and control register

- ◆ Instruction pointer.(IP)



# Internal block diagram of 80286



# Internal block diagram of 80286

- ❖ It contain four functional parts

1. Address unit (AU)

- ❖ The address unit (AU) computes the physical addresses that will be sent out to memory or IO .
- ❖ 80286 operate in two memory address modes
  - ❖ Real address mode. (1MB)
  - ❖ Protected virtual address mode. (1GB)

2. Bus unit (BU)

- ❖ It performs
  - ❖ All memory and IO read and writes
  - ❖ Pre fetches instruction bytes
  - ❖ Control transfer of data to and from coprocessor (80287)

3. Instruction unit (IU)

- ❖ It decodes up to three pre fetched instructions and hold them in a queue, where execution unit can access them.

4. Execution unit (EU)

- ❖ The execution unit (EU) uses its 16 bit ALU to execute instructions it receives from instruction unit.

# Limitation of 80286 microprocessor

- ❖ Only a 16 bit ALU
- ❖ Maximum segment size=64KB
- ❖ Cannot easily switch back and forth between real and protected mode.

## Features of 80386 microprocessor

- ❖ 32 bit processor that supports **8/16/32** bit data operands.
- ❖ **Compatibility** with existing processors like 80286 etc
- ❖ **32 bit ALU**
- ❖ No of segments=**16384**, each segment size=**4GB** therefore virtual address space= $16384 \times 4\text{gb} = \mathbf{64\text{TeraBytes}}$
- ❖ Physical memory size= $2^{32} = 4\text{GB}$
- ❖ The 80386 can be supported by 80387 for mathematical data processing.
- ❖ 80386 has on chip address translation cache.

# Features of 80386 microprocessor

- ❖ The concept of paging is introduced in 80386, size of each page is 4KBs under the segmented memory.
- ❖ 80386 has “virtual 8086” mode, which allow it to easily switch back and forth between real and protected mode.
- ❖ 80386 is available in versions
  - ❖ **80386SX-**
    - ❖ It has only a 16 bit data bus and 24 bit address bus.
    - ❖ Low cost
    - ❖ Low power version of 80386
  - ❖ **80386DX**
    - ❖ IT has 32 bit address and data bus.

# Assignment no. 1 CSL211: AMP

- ❖ Q1. Draw block diagram of computer system showing address, data and control bus structure.
  
- ❖ Q2. Write Short note on
  - ❖ A) Programming Model
  - ❖ B) Register organization of 8086
  - ❖ C) memory segmentation of 8086
  - ❖ D) 8086 Flag register
  
- ❖ Q3. Describe internal architecture of 8086 microprocessor with neat diagram.
  
- ❖ Q4. Describe internal architecture of 80286 Microprocessor with neat diagram.
  
- ❖ Q5. List the features of 80386 Microprocessor.