Unit 1

Microprocessor Architecture

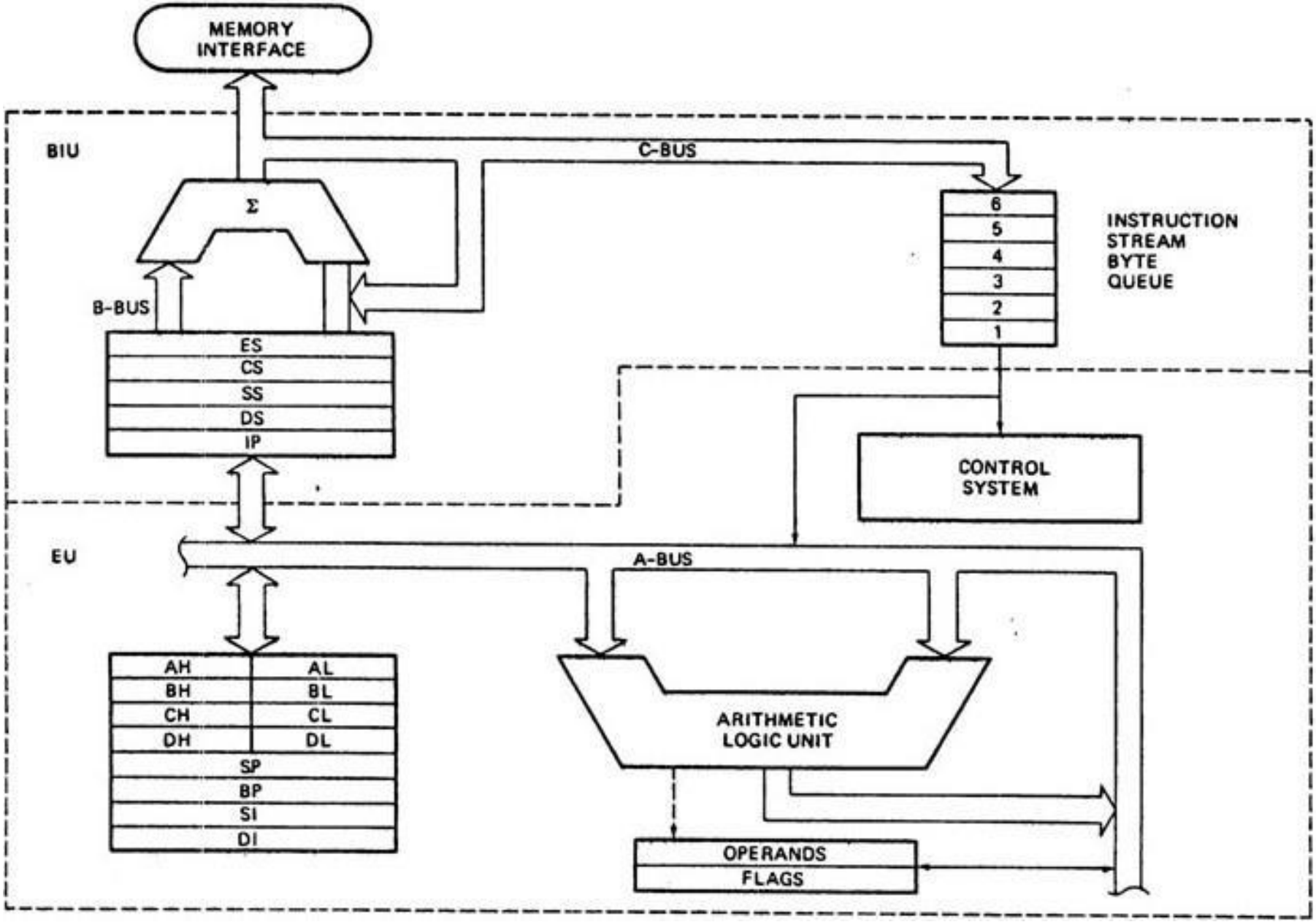
Features of 8086:

- It requires +5v power supply.
- It is 16 bit MP
- It is available in 3 versions based on the frequency of operation −
  - 8086 → 5MHz
  - 8086-2 → 8MHz
  - 8086-1 → 10 MHz
- It has 20-bit address bus, so it can directly access 2^{20} = =1MB (10,48,576) memory locations.
- It can generate 16 bit I/O address , hence it can access 2^{16} =65536 I/O ports
- Operating frequency of upto 5MHz.

Features of 8086:

- It has multiplexed address and data bus.(A_{D0} to A_{D15})
- Performs bit, byte and word operations.
- Powerful instruction set with different addressing modes.
- It supports a 16 bit ALU , a set of 16 bit registers,
- Provides segmented memory addressing capability
- It has rich instruction set, powerful interrupt structure,
- It has 6 byte Instruction queue.

Architecture of 8086



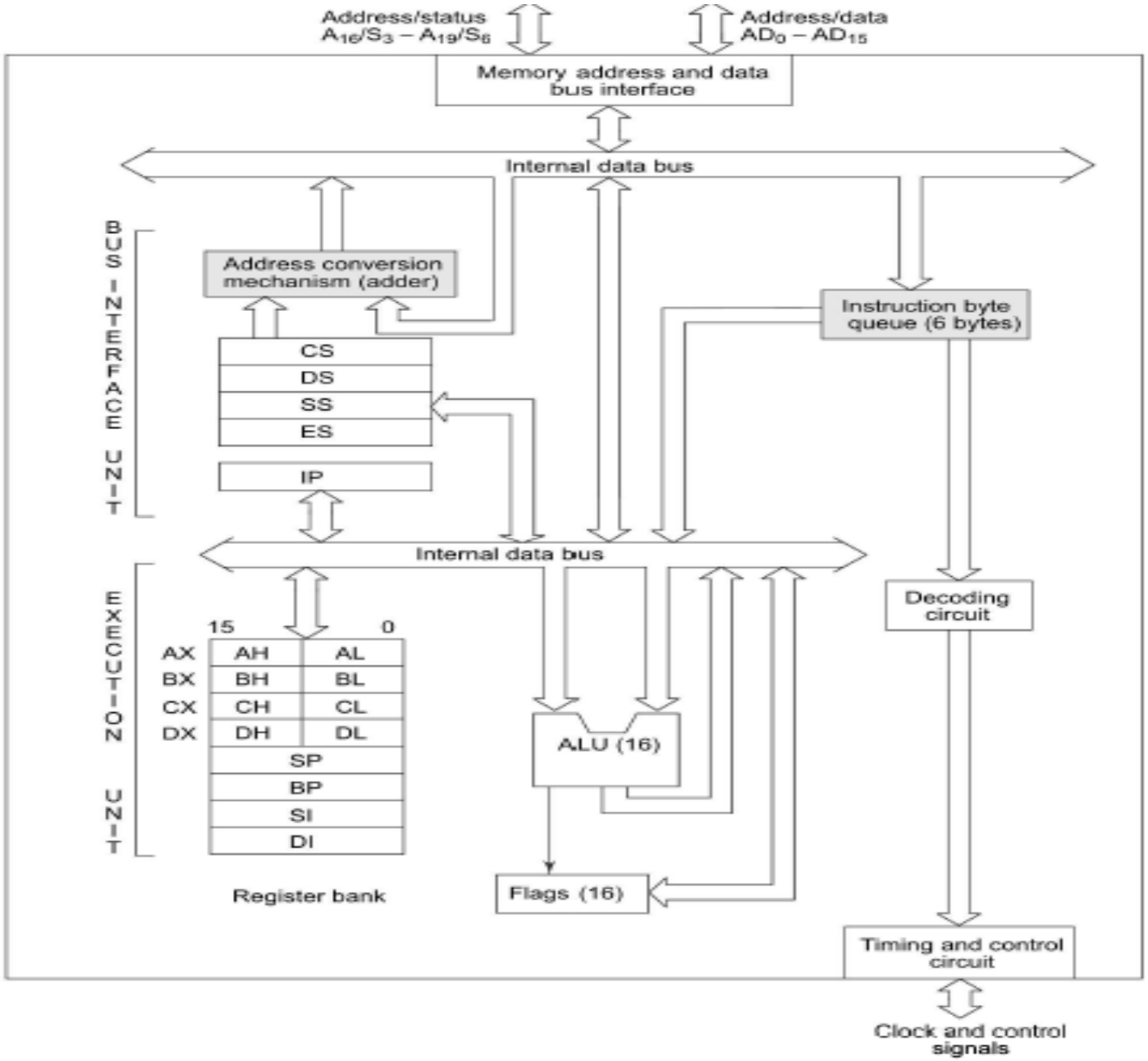


Fig. *8086 Architecture*

Register organization of 8086

– General purpose
  - Holding data , variables and intermediate results
  - Counters or for storing offset address

– Special purpose
  - Used as segment registers, pointers, index registers or as offset storage for particular addressing mode.

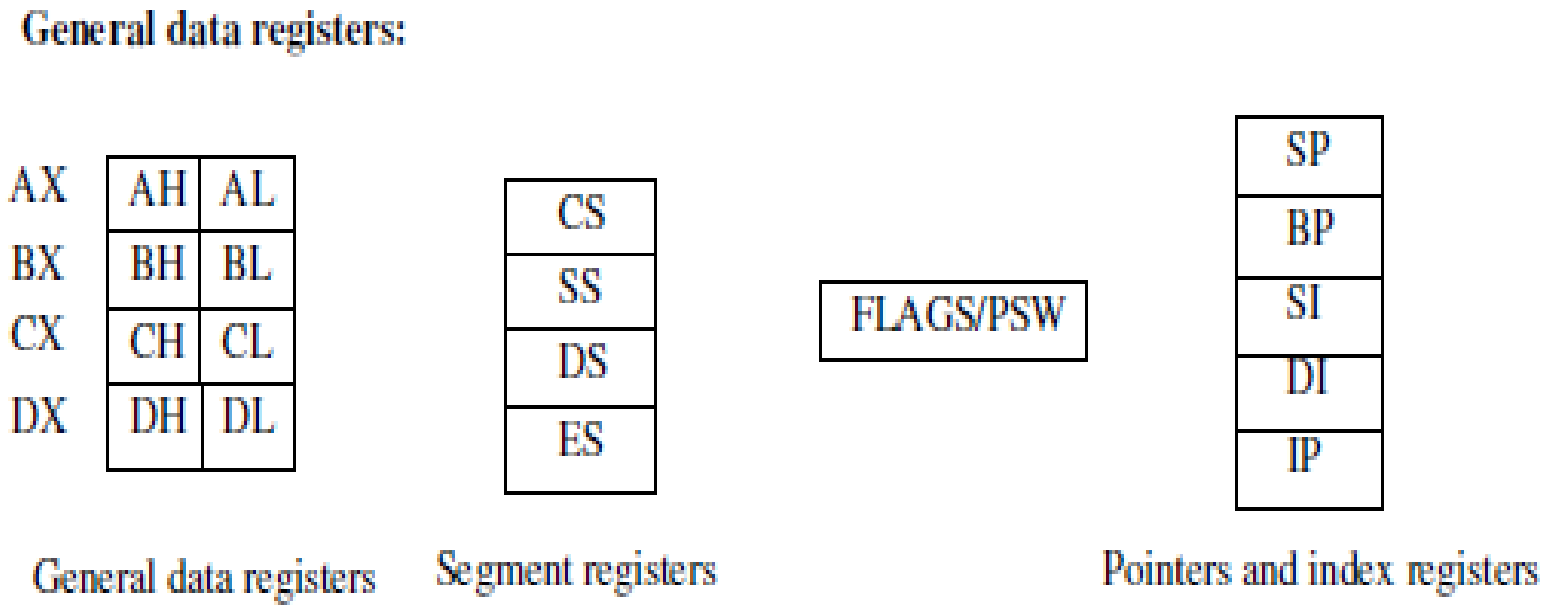


Fig. Register organization of 8086

8086 Architecture

- Segment Registers:
- CS
  - is used for addressing a memory location in the code segment of the memory, where executable program is stored.
- DS:
  - Points to the data segment of the memory, where data is resided.
- ES:
  - Essentially another data segment of the memory
- SS:
  - Memory used to store stack data

Pointers and Index registers:

- pointers contain offset within particular segment.
  - IP,BP and SP contain offset within the CS
  - BP and SP within the SS.
  - **BP –** This is the base pointer. It is of 16 bits.
  - It is primary used in accessing parameters passed by the stack.
  - It’s offset address relative to stack segment.

- Index registers:
  - Are used as general purpose registers as well as offset storage in case of indexed, base indexed and relative based indexed addressing modes.
  - SI- is used to store the offset of source data in data segment
  - DI- is used to store the offset of destination in data or extra segment

8086 Architecture

- 2 functional units:
  - BIU(Bus Interface Unit)
  - EU(Execution Unit)

- **BIU(Bus Interface Unit)**
  - It makes systems bus signals available for external interfacing of the devices.
  - Is responsible for establishing communication with external devices and peripherals including memory.
  - BIU contains the circuit for physical address calculations and predecoding instruction byte queue(6 byte)

8086 Architecture

- It looks after the operation of address and data bus. Its functions are-
  - To generate address for memory and I/O ports
  - To fetch instructions from memory
  - To read data from memory and I/O ports
  - It supports instruction queuing
  - It writes data into port /memory.

8086 Architecture

- How to generate physical address:
  - Content of segment register (seg. add) is shifted left bitwise four times and offset register (offset add) is added to this result, which produces 20 bit physical address.

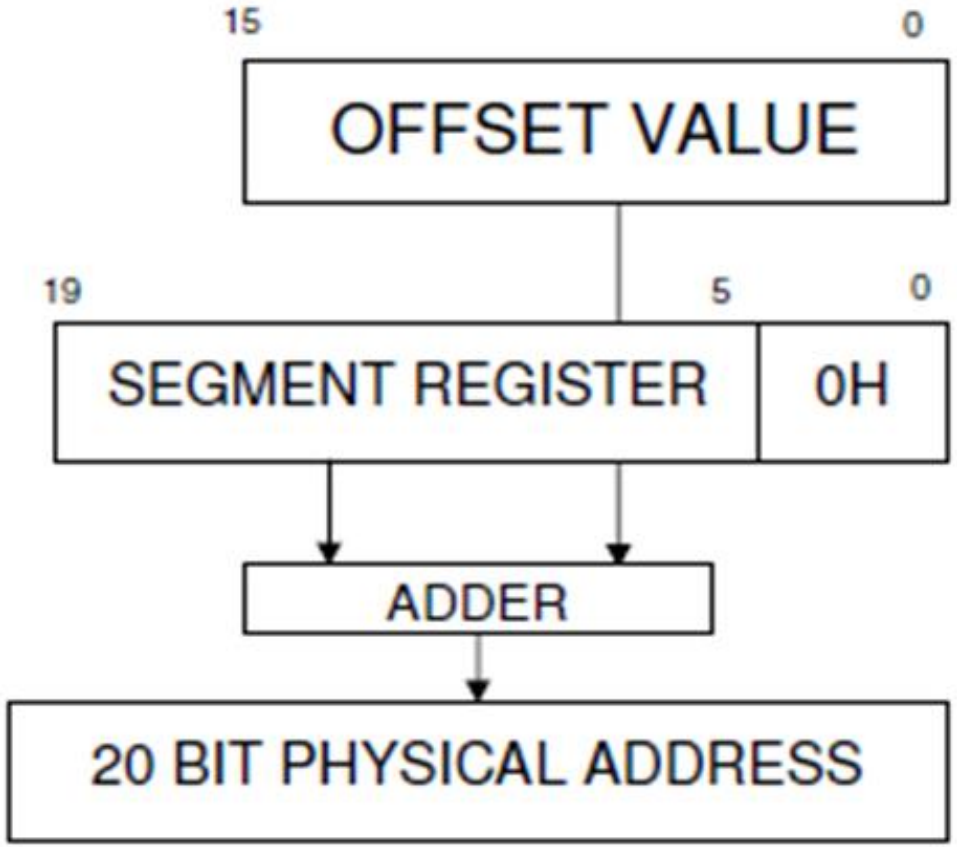


Fig. Physical address formation

8086 Architecture

e.g. seg address= 1005H

offset address= 5555H

segment address=1005= 0001 0000 0000 0101

Shifted by 4 bit 0001 0000 0000 0101 0000

\+

Offset address 0101 0101 0101 0101

0001 0101 0101 1010 0101

= 1 5 5 A 5

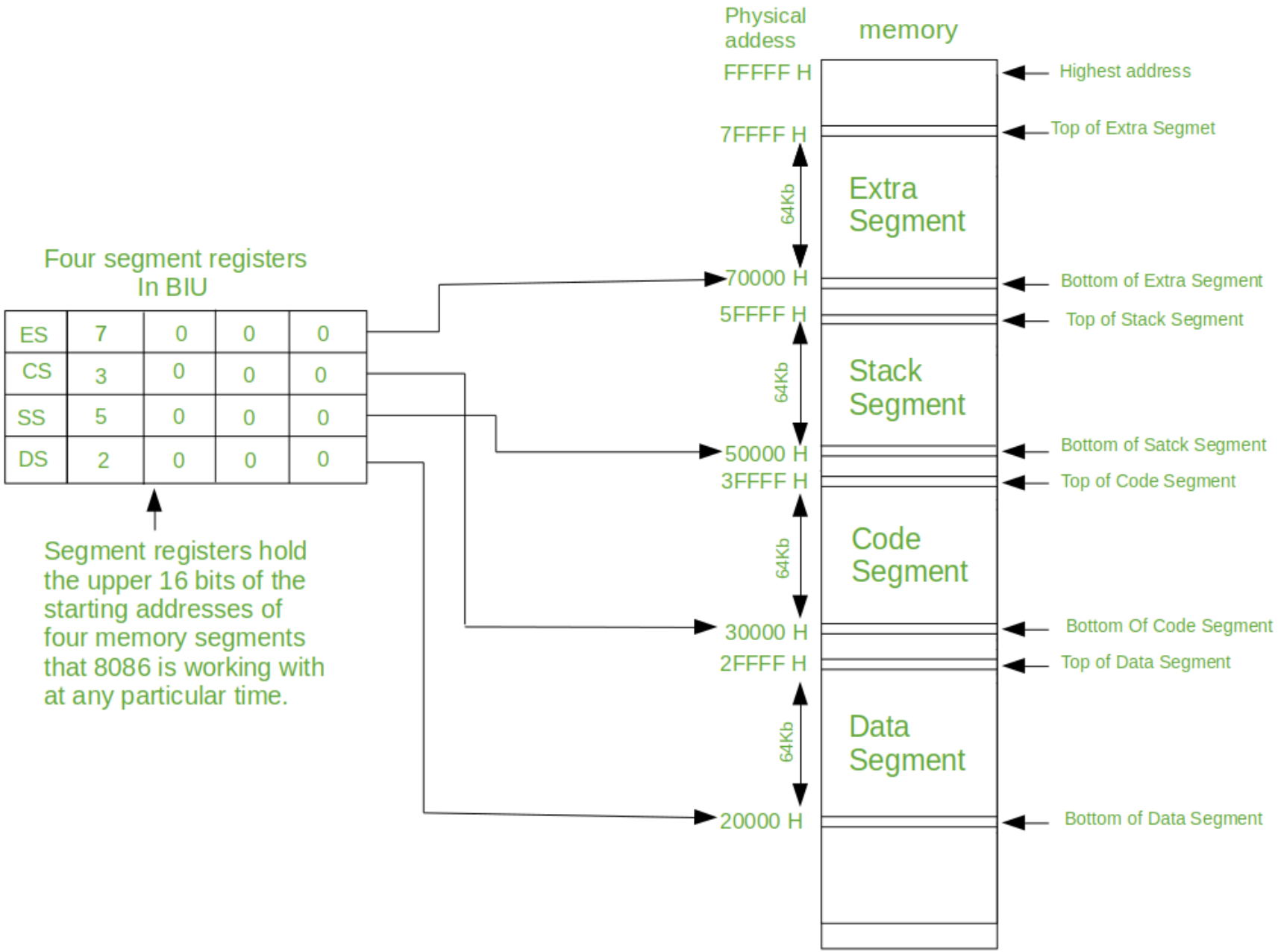
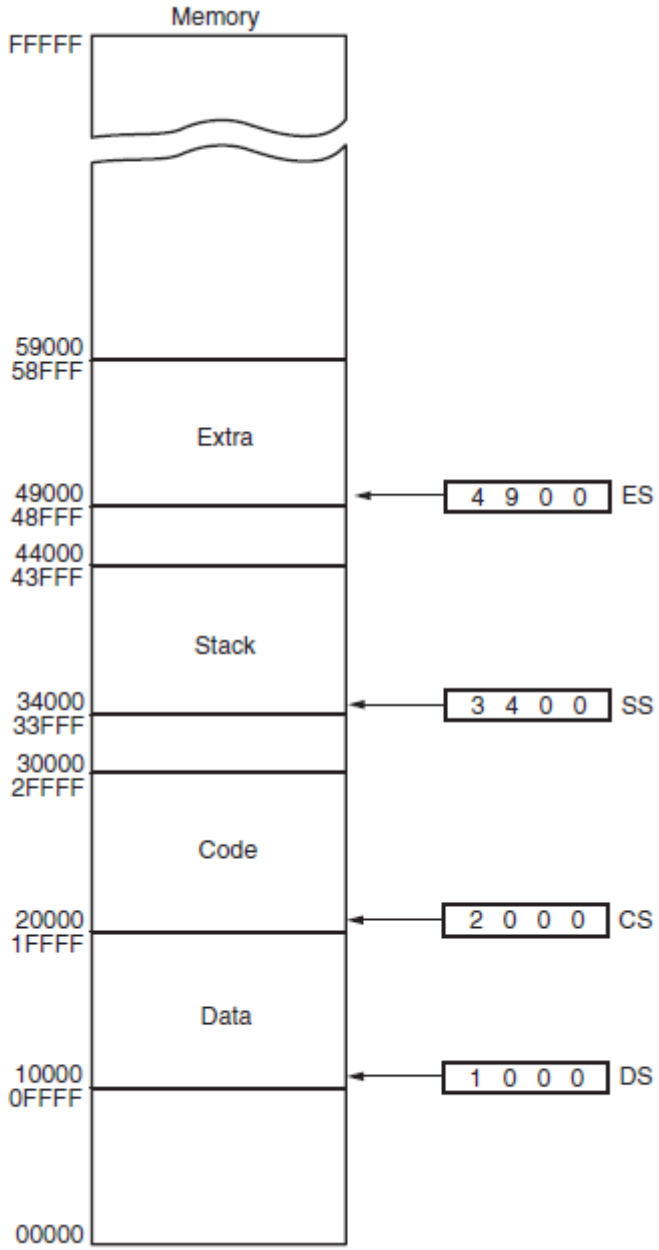

Physical addess
memory
FFFFF H
Highest address
7FFFF H
Top of Extra Segmet
64Kb
Extra Segment
Four segment registers In BIU
70000 H
Bottom of Extra Segment
5FFFF H
Top of Stack Segment
ES 7 0 0 0
CS 3 0 0 0
SS 5 0 0 0
DS 2 0 0 0
64Kb
Stack Segment
50000 H
Bottom of Satck Segment
3FFFF H
Top of Code Segment
Segment registers hold the upper 16 bits of the starting addresses of four memory segments that 8086 is working with at any particular time.
64Kb
Code Segment
30000 H
Bottom Of Code Segment
2FFFF H
Top of Data Segment
64Kb
Data Segment
20000 H
Bottom of Data Segment

FIGURE A memory system showing the placement of four memory segments.



- Maximum 64K locations may be accommodated in the segment.

- **Segment register** indicates the base address of a particular segment

- **offset indicates** the distance of the required memory location in the segment from the base address.

- BIU has summer (adder) to perform this procedure for obtaining physical address while addressing memory.

8086 Architecture

- Execution Unit:
  - Decodes and executes the instructions

- EU does:
  - To load segment registers
  - To update IP while branching a prog. Execution
  - Execution unit gives instructions to BIU stating from where to fetch the instruction and then decode and execute those instructions
  - Instructs BIU for reading or writing data from or to a memory location or an I/O ports.

8086 Architecture

- **Execution unit:**
  - Contains register set of 8086 except segment registers and IP.
  - It has 16 bit ALU
  - 16 bit flag register
  - Decoding unit decodes opcode bytes received from instruction byte queue
  - Timing and control unit derives the necessary control signal to execute instruction opcode received from decoding circuit.
  - Pass this result to BIU for storing in memory.

8086 Architecture

- Instruction Queue:
  - It is FIFO memory

8086 Architecture

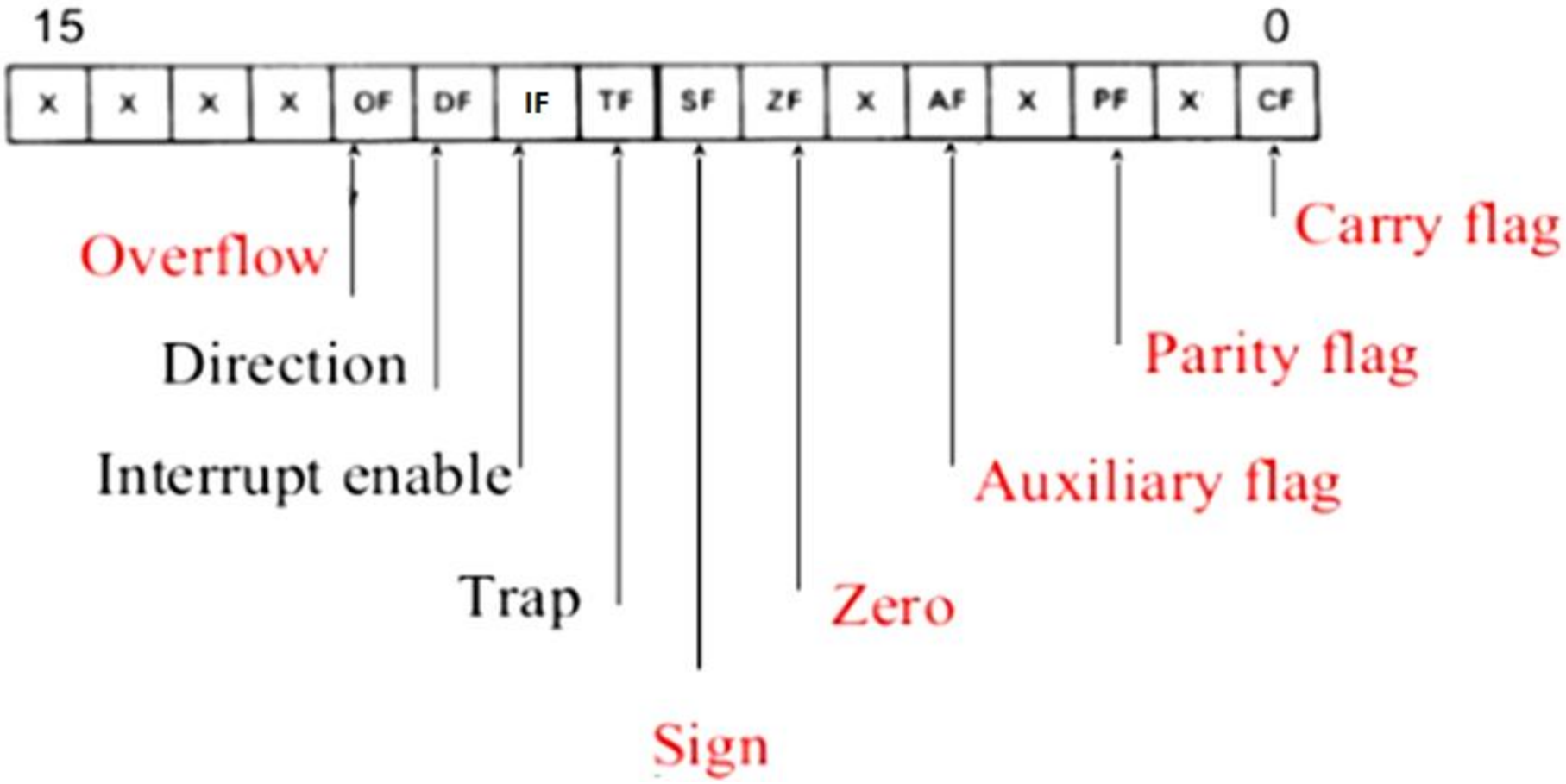


Fig 8086 Flag Register

- Conditional (status) flags=6
- Control flags=3

- TF –Trap Flag:
  - If T=1– processor enters the single step execution mode.
  - i.e. trap interrupt is generated after execution of each instruction.

- IF – Interrupt flag:
  - If this flag is set, maskable interrupts are recognized by the CPU, otherwise they are ignored.

- DF- Direction flag: used by string manipulation instructions.
  - if DF=0 –the string is processed beginning from the lowest address to the highest address i.e. auto incrementing mode.
  - if DF=1 –the string is processed from highest address towards the lowest address i.e. auto decrementing mode.

8086 Addressing Modes:

- Ways of locating data or operands.
- Describes the type of operands and the way they are accessed for executing an instruction.

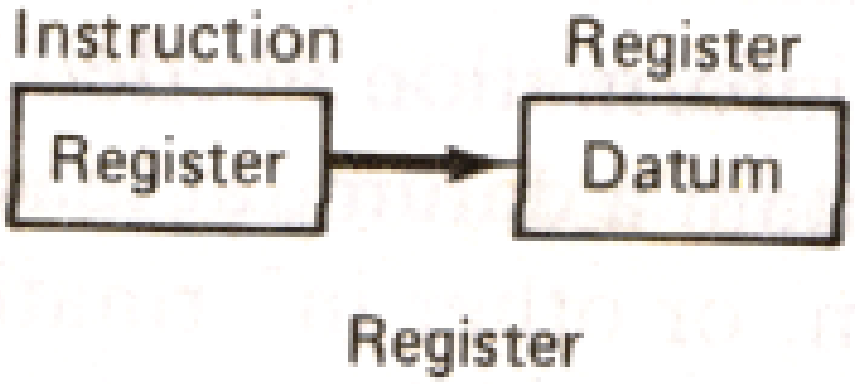
Addressing modes

- DATA-ADDRESSING MODES
- PROGRAM MEMORY-ADDRESSING MODES
- STACK MEMORY-ADDRESSING MODES

- **DATA-ADDRESSING MODES**
  - Register Addressing
  - Immediate addressing
  - Direct addressing
  - Register indirect addressing
  - Indexed
  - Register relative
  - Based indexed
  - Relative based indexed

8086 Addressing mode:

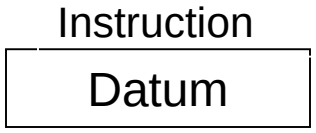
- Register addressing mode



MOV CX, AX

ADD BX, AX

- Immediate addressing mode



Immediate addressing mode

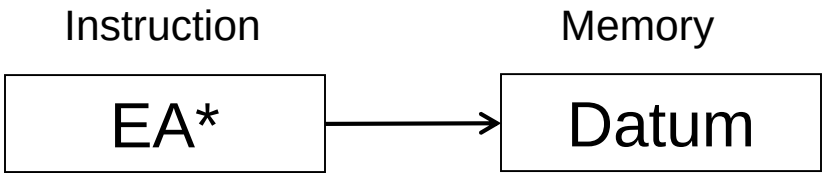
MOV DX, 4929 H

ADD AX, 2387 H,

MOV AL, FFH

8086 Architecture

- Direct Addressing:
  - 16 bit memory address (offset) is specified in the instruction



Direct Addressing Mode

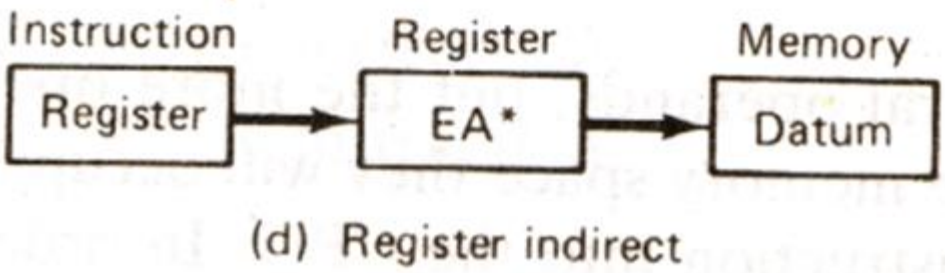
MOV AX, [5000H],

MOV AL, [C050H]

IN 80h

EA=10*DS+5000h

- Register indirect:



(d) Register indirect

MOV AX, [BX],

MOV AL, [DX]

EA=10*DS+[BX]

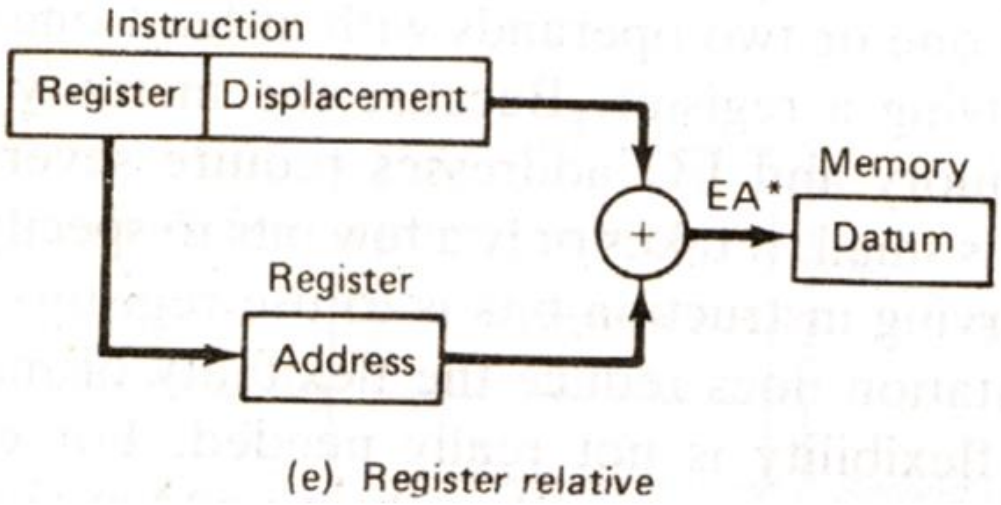
- **Indexed:** offset of the operand is stored in one of the index registers.

MOV AX, [SI],

EA=10*DS+[SI]

8086 Instruction set:

- Register relative addressing mode:
  - EA is formed by adding 8 or 16 bit displacement with the content of any one of the registers BX, BP,SI or DI in the segment(DS or ES)



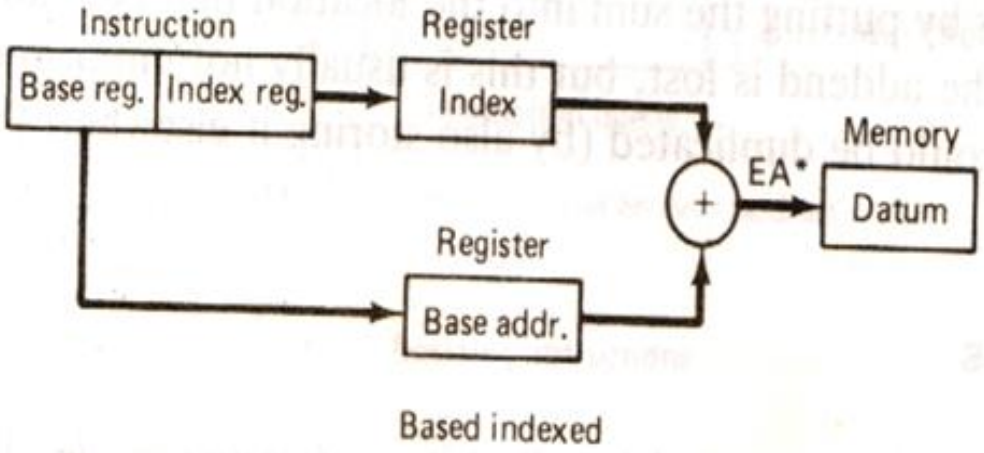
(e) Register relative

MOV AX, 50H [BX],

EA=10*DS+50+[BX]

8086 Architecture

- Based Indexed:

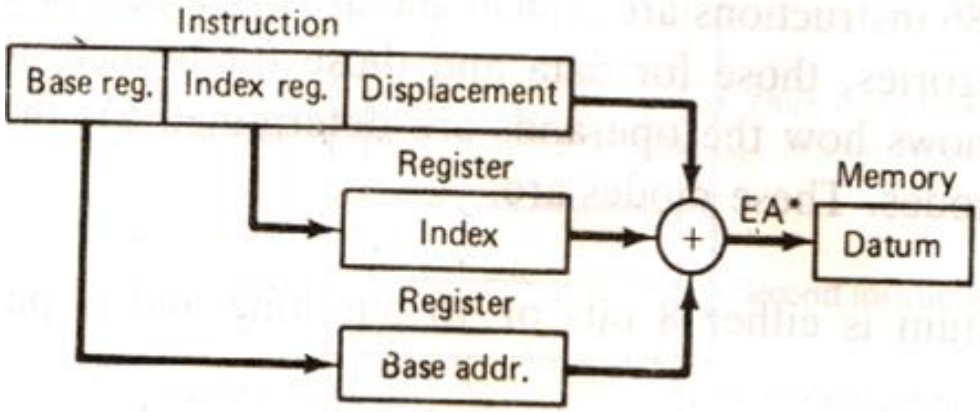


Based indexed

MOV AX , [BX] [SI]

EA=10*DS+[BX]+[SI]

- Relative Based Indexed:



Relative based indexed

MOV AX, 50H[BX] [SI]

EA=10*DS+50H+[BX]+[SI]

- For control transfer
  - Intra-segment direct Mode(within same)
  - Intra-segment indirect Mode
  - Inter-segment direct Mode (different)
  - Inter-segment indirect Mode

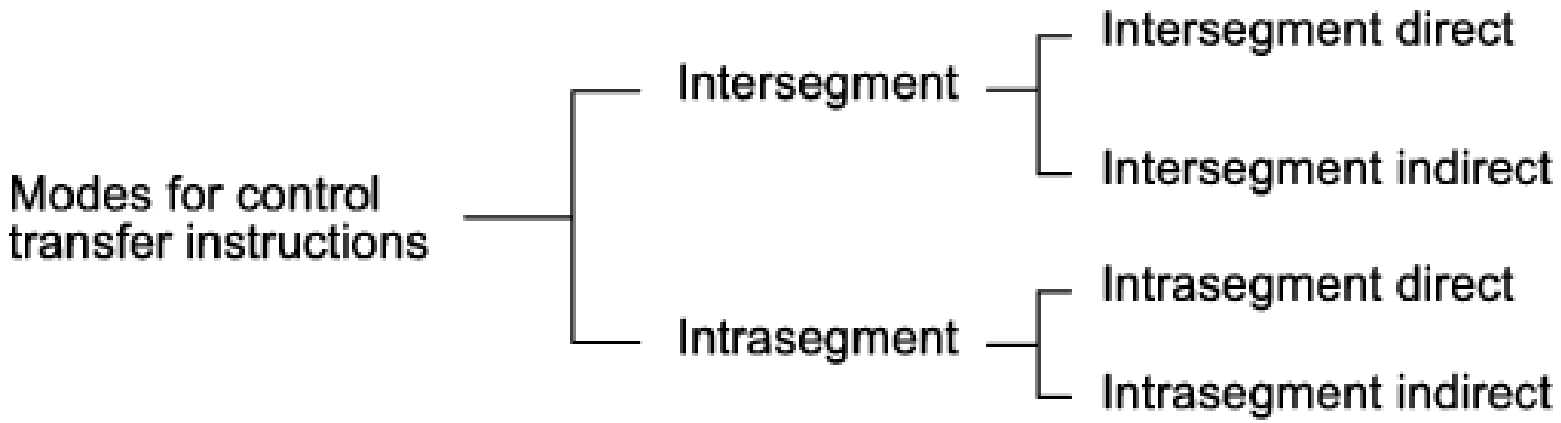


Fig. ***Addressing Modes for Control Transfer Instructions***

PROGRAM MEMORY-ADDRESSING MODES /control transfer instructions

- Intra-segment direct Mode
  - The displacement is computed relative to the content of the instruction pointer
  - Address to which control will be transferred is given by the sum of 8 or 16 bit displacement and current contents of IP
  - 8 bit displacement (-128<d<+127) –short jump
  - 16 bit displacement (-32768<d<+32767) –long jump
  - JMP SHORT LABEL
    - LABEL lies within -128<d<+127

PROGRAM MEMORY-ADDRESSING MODES /control transfer instructions

- Intra-segment indirect Mode
  - JMP [BX]
  - Jump to effective address stored in BX

PROGRAM MEMORY-ADDRESSING MODES /control transfer instructions

- Intersegment direct Mode
  - Provides branching from one code segment to another code segment.
    - JMP 5000h : 2000h

- Intersegment indirect Mode
  - The address to which control is to be transferred lies in a different segment and is passed to the instruction indirectly.
  - contents of a memory block containing four bytes, i.e. IP(LSB), IP(MSB), CS(LSB) and CS(MSB) sequentially.
  - JMP [2000]

STACK MEMORY-ADDRESSING MODES

- The stack memory is an LIFO (**last-in, first-out) memory,** which describes the way that data are stored and removed from the stack.

- Data are placed onto the stack with a **PUSH instruction** and removed with **a POP** instruction**.**

Bus:

- A bus is a common group of wires that interconnect components in a computer system.

- The buses that interconnect the sections of a computer system transfer address, data, and control information between the microprocessor and its memory and I/O systems.

- 3 buses exist for this transfer of information: address, data, and control.

- Figure shows how these buses interconnect various system components such as the microprocessor, read/write memory (RAM), read-only memory (ROM or flash), and I/O devices.

BUS:

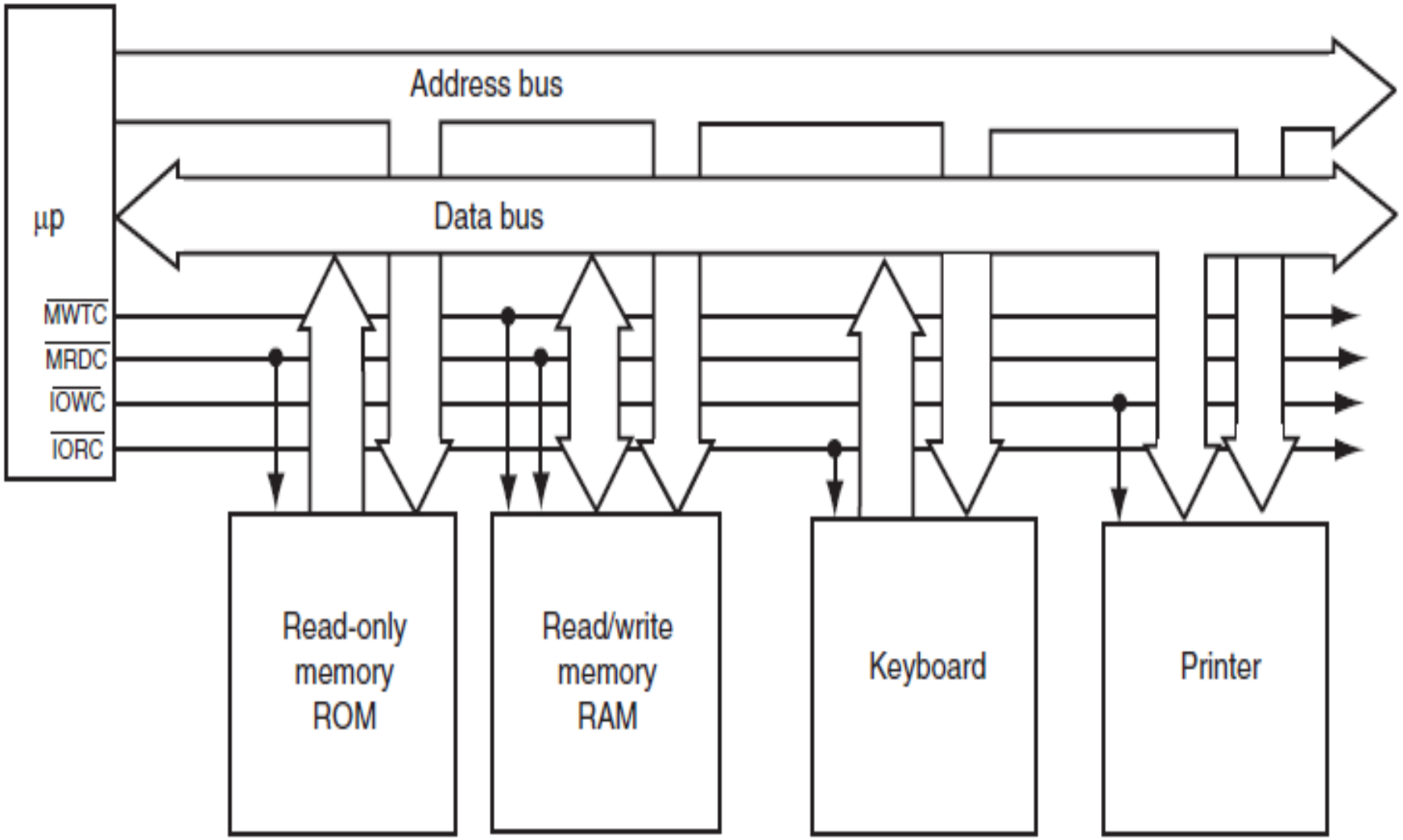


FIGURE The block diagram of a computer system showing the address, data, and control bus structure.

- **Address bus** requests a memory location from the memory or an I/O location from the I/O devices.

- **Data bus** transfers information between the microprocessor and its memory and I/O address space.
  - Data transfers vary in size, from 8 bits wide to 64 bits wide in various members of the Intel microprocessor family

- **Control bus** contains lines that select the memory or I/O and cause them to perform a read or write operation.
  - there are four control bus connections:(**memory read control**), (**memory write control**), (**I/O read control**), and (**I/O write control**).

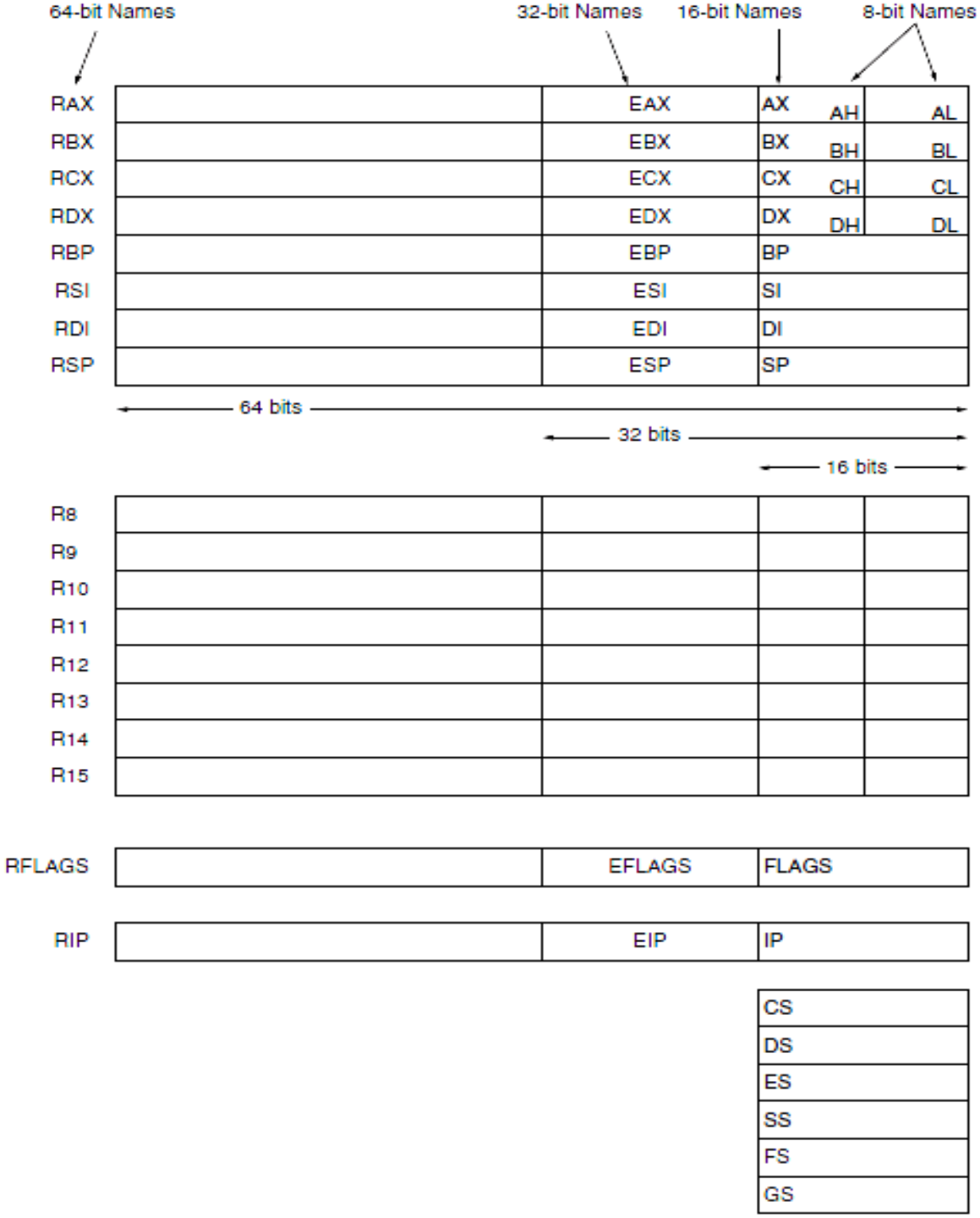
- **The Programming Model.**

  - The programming model of the 8086 through the Core2 is considered to be **program visible** because its registers are used during application programming and are specified by the instructions.

Programming model:

- The programming model contains 8-, 16-, and 32-bit registers.
- The Pentium 4 and Core2 also contain 64-bit registers when operated in the 64-bit mode as illustrated in the programming model.
  - The 8-bit registers are AH, AL, BH, BL, CH, CL, DH, and DL
  - The 16-bit registers are AX, BX, CX, DX, SP, BP, DI, SI, IP, FLAGS, CS, DS, ES, SS, FS, and GS.
  - The first 4, 16 bit registers contain a pair of 8-bit registers. e.g AX, which contains AH and AL.
  - The extended 32-bit registers are EAX, EBX, ECX, EDX, ESP, EBP, EDI, ESI, EIP (all are multipurpose) and EFLAGS. These 32-bit extended registers, and 16-bit registers FS and GS, are available only in the 80386 and above.

FIGURE 2–1 The programming model of the 8086 through the Core2 microprocessor including the 64-bit extensions.



Memory segmentation

- The complete physically available memory may be divided into a number of logical segments.
- Each segment is 64kb and addressed by one of the segment register.
- 8086 is able to address upto 1Mb of physical memory.
- Complete 1Mb memory is divided into 16 segments each of 64kb

- Advantages of memory segmentation are:
  - Allows memory capacity to be 1MB , although the actual address to be handled are 16 bit size.
    - It provides a powerful memory management mechanism.
  - Allows the placing of code, data and stack portions of the same program in different parts (segments) of memory for data and code protection.
    - Data related or stack related operations can be performed in different segments.
    - Code related operation can be done in separate code segments.
  - Permits a program and its data to be put into different areas of memory each time the program is executed.

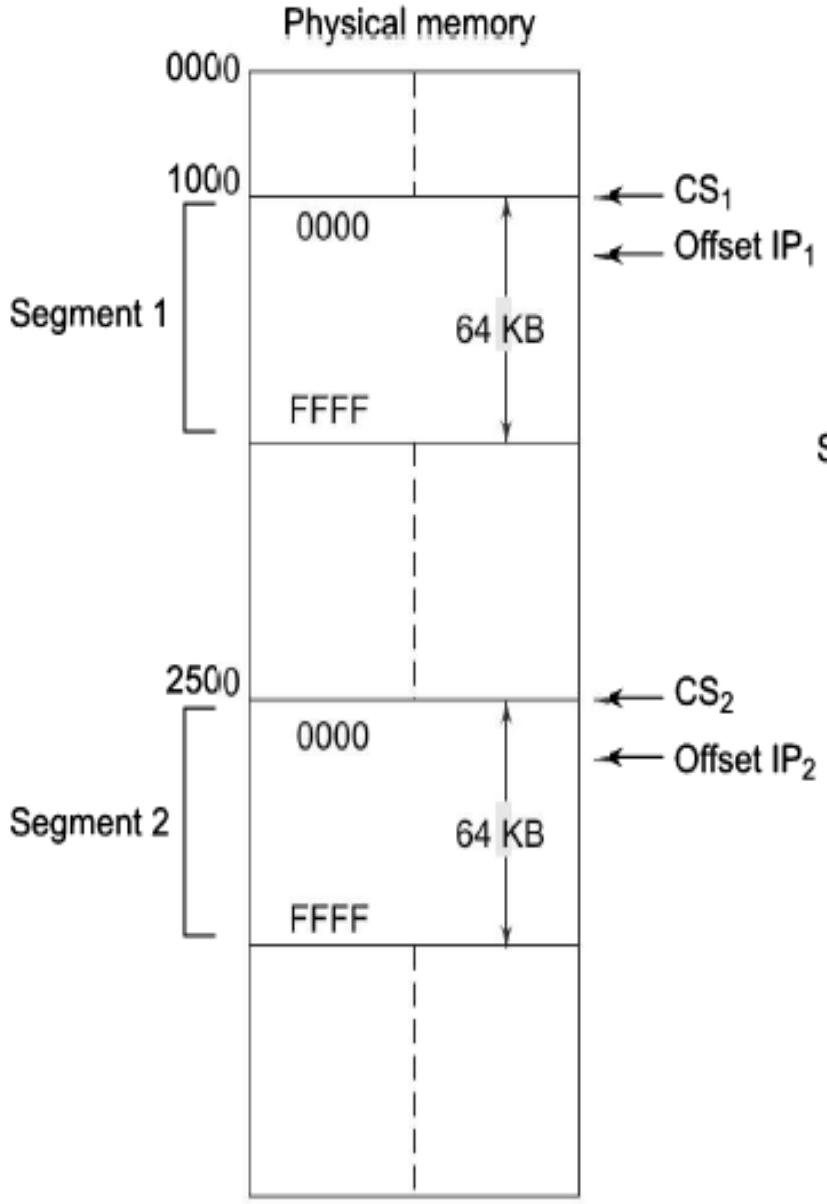


Fig. (a) *Non-overlapping Segments*

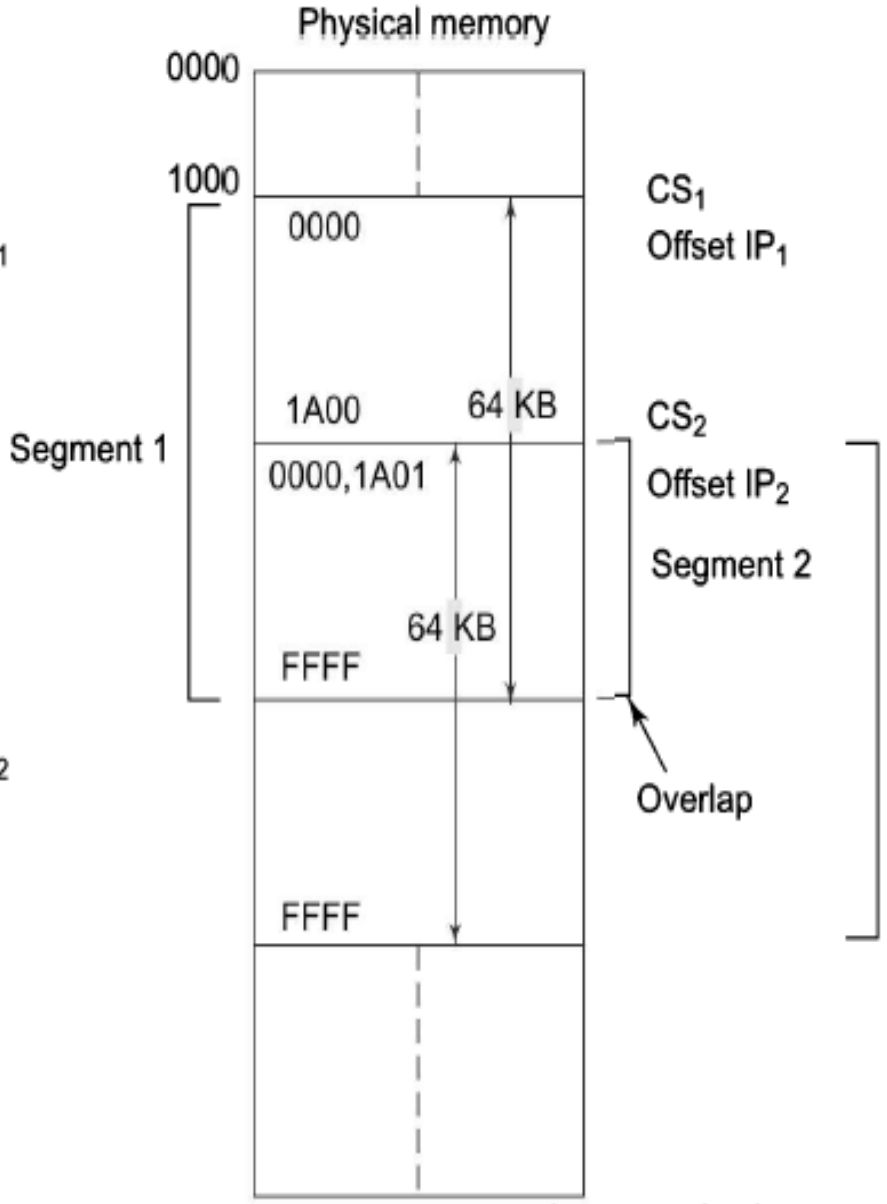


Fig. (b) *Overlapping Segments*

Features of 80286

- It is 16 bit MP but faster than 8086
- The 80286 CPU, with its 24-bit address bus is able to address 2^{24}=16 Mbytes of physical memory.
- The clock frequencies are 4MHz , 6MHz, 8MHz , 10 MHz and 12.5 MHz .
- 80286 is upwardly compatible with 8086 in terms of instruction set.

- Enhanced instruction set
- It is 4 stage pipeline microprocessor .

- **80286 works in 2 operating modes:**
- **Real address mode**
  - In RM 80286 just acts as fast 8086.(addresses 1Mb memory)
  - 8086 program can be executed without modification in 80286
  - MMU and protection mechanisms are disabled in this mode.
- **Protected virtual address mode(PVAM)**
  - 80286 can address 16Mb of memory
  - Supports multitasking –run several program at the same time.
  - Works with its MM and protection capabilities with advanced instruction set.
  - it can address upto 1GB virtual memory .

Register Organization of 80286

a) Eight 16-bit general purpose registers
b) Four 16-bit segment registers
c) Status and control registers
d) Instruction Pointer

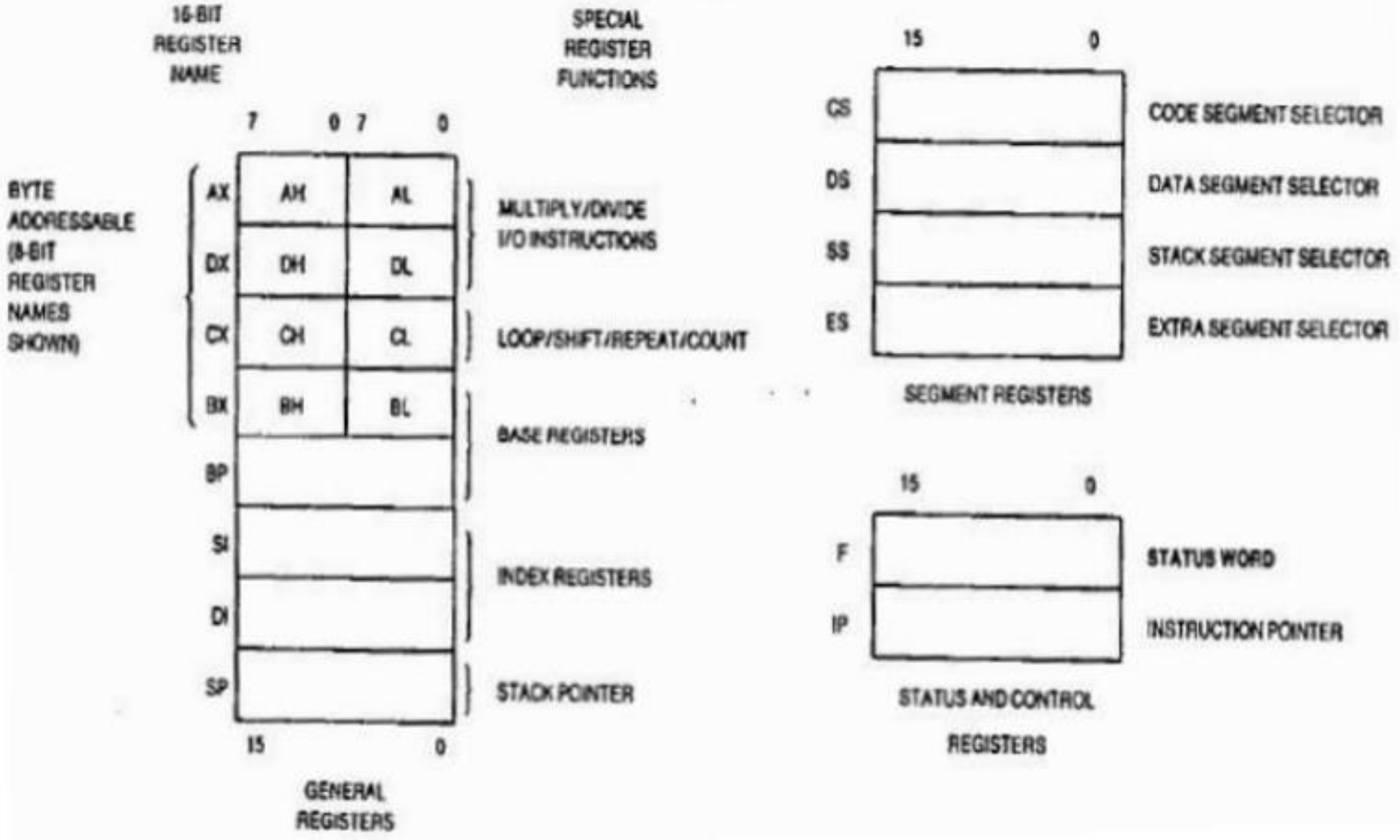


Fig.2.17 Register set of 80286

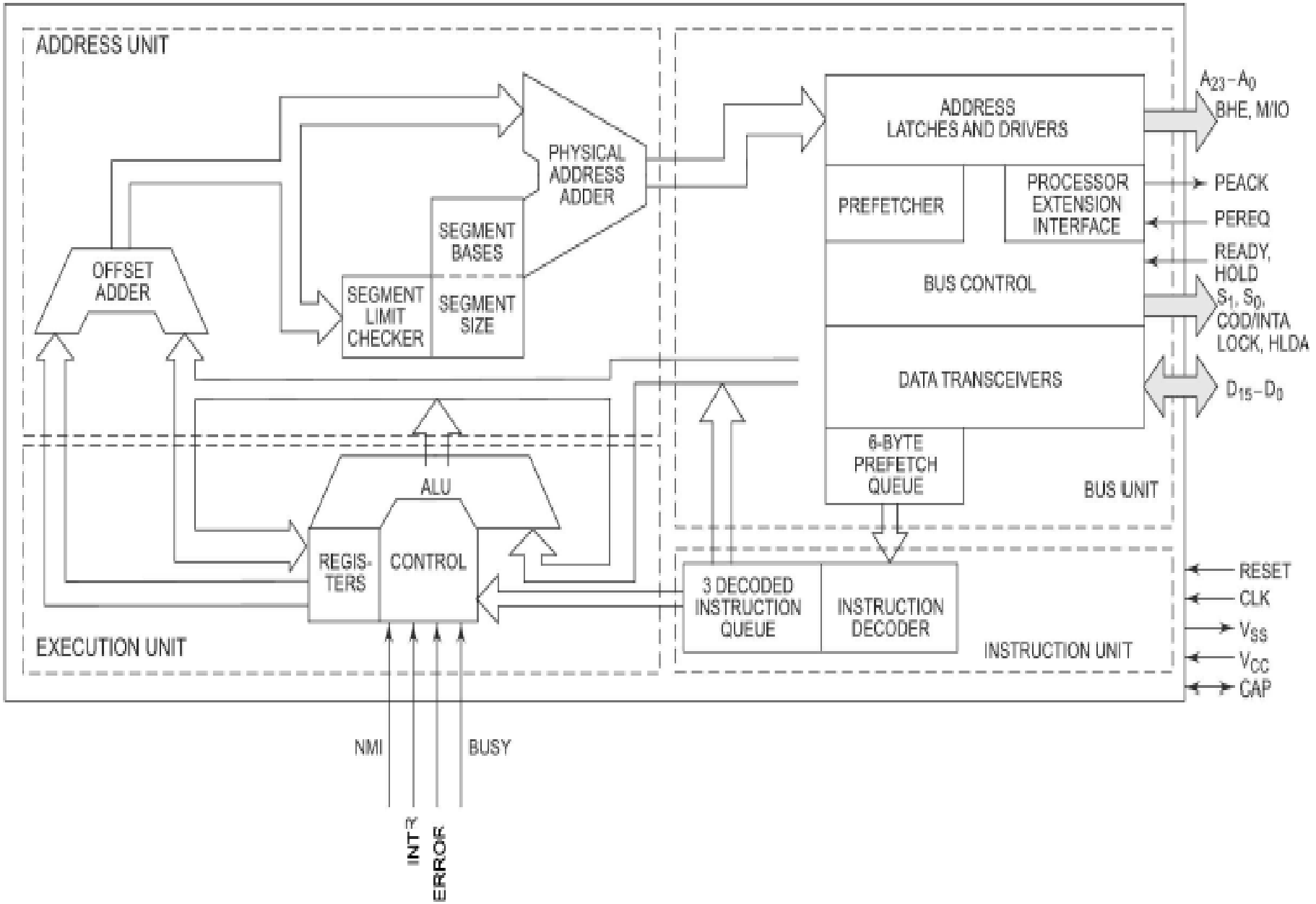


Fig. *Internal Block Diagram of 80286 (Intel Corp.)*

- Internal block diagram of 80286 contains 4 units :
- **Address Unit(AU)**
    - Address unit calculated the physical address of instruction and data that the CPU wants to access.
    - This address is send to BIU

- **Bus Unit(BU)**
    - Fetches instruction bytes from memory.
    - Bus Unit includes –
        - **Address latches and drivers-** transmits the physical address over the address bus A0-A23
        - **Prefetcher**- performs the task of prefetching
        - **Bus control module-** control the prefetcher module.
        - Processor extension interface module- takes care of communication between coprocessor and CPU
        - Transreceivers interface : control the internal data bus with the system bus
        - 6 byte prefetch queue: forwards the instructions to the IU.

- Instruction unit(IU)
  - It accepts instruction from prefetch queue and instruction unit decodes them one by one.
  - Output of decoding circuit drives the control circuit in the EU.

- Execution unit
  - Executes the instructions received from decoded instruction queue which sends the data part of the instructions over the data bus.
  - EU contains registers bank (for storing data) and ALU (for atithmatic and logical operations).

80386---32 bit processor

- Features of 80386:
- It is a 32 bit processor with 8, 16, 32-Bit Data Types
  - 8 General Purpose 32-Bit Registers
- Instruction set is compatible with all its predecessors.

- Very Large Address Space
  - With 32 address lines it can address 2^{32} = 4 GB Physical Memory
  - 4 GB each Segment Size
    - No of segments = 16384
  - Virtual space = 16384 * 4GB = 64 Terabyte

- 80386 is available in 132 PGA package and has 20MHz and 33 MHz versions
- The 80386 also includes 32-bit extended registers and a 32-bit address and data bus
- The 80386 has on chip address translation cache.
- The concept of paging is introduced in 80386 enables to organize available physical memory into page of size 4Kbytes each.

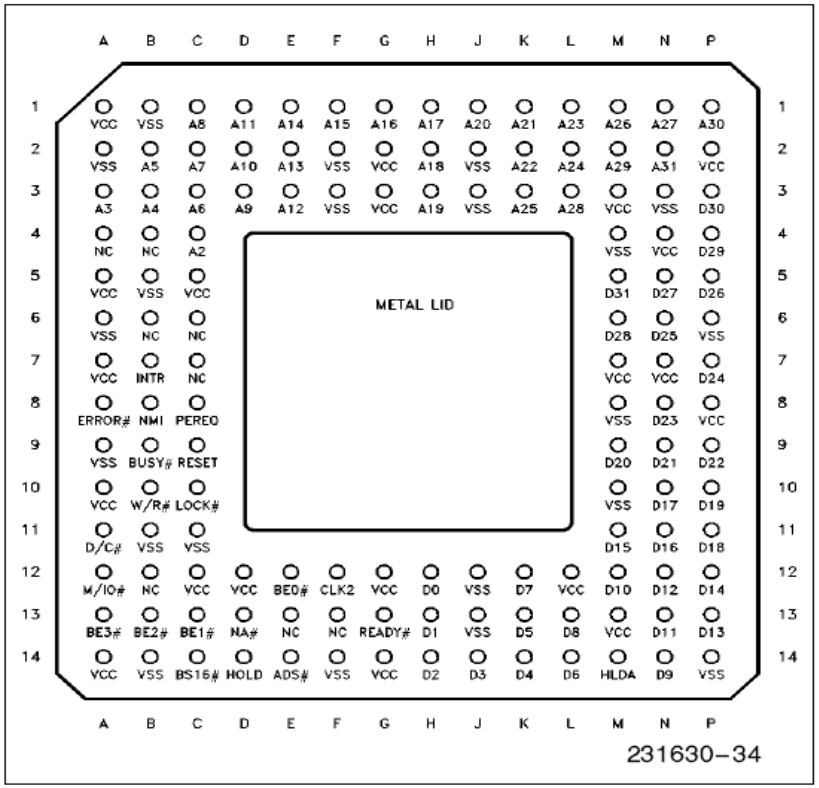
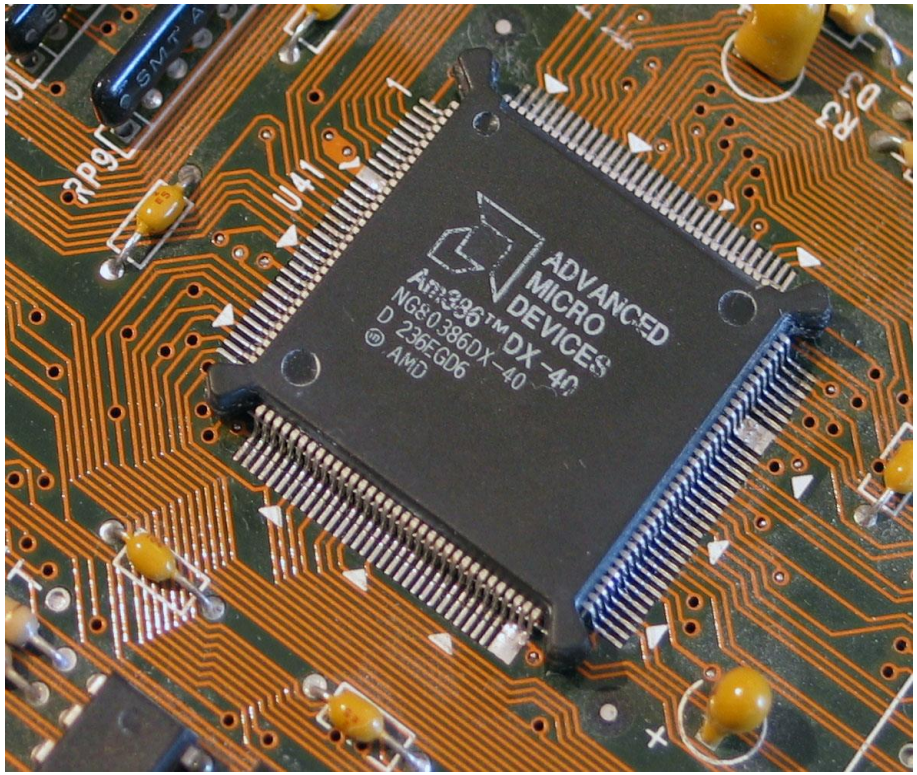


Figure 1-2. Intel386™ DX PGA Pinout—View from Pin Side



- 80386 can be supported by 80387 for mathematical data processing.

- 80386 has virtual 8086 mode which allow it to switch back and forth between real and protected mode.

- 80386 is available in different versions
  - 80386SX
    - It has 16 bit data bus and 24 bit address bus
    - Low cost
    - Low power version used in many applications
  - 80386DX
    - It has 32 bit address and data bus

Thank You