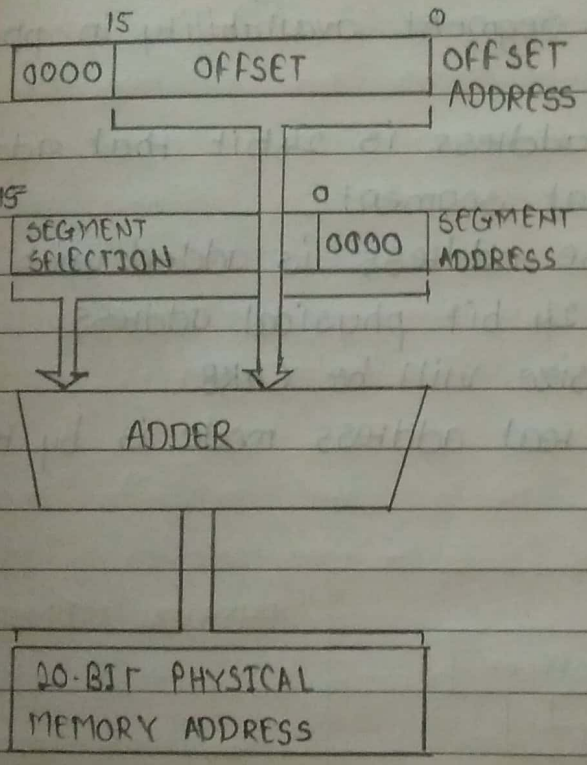
19UCS090

DATE

# Assignment No. 4

Q.1. Draw and explain real mode addressing of 80286 microprocessors.

→
- In RM 80286 just acts as fast 8086 (address of 1Mb memory).
- 8086 program can be executed without modification in 80286.
- MMU and protection mechanisms are disabled in this mode.




- 20 bit physical address is formed in same way as that in 8086.
- The contents of segment registers are used as segment base addresses.
- The other registers depending upon the addressing mode, contain the offset address.
- PA = CS * 10h + offset(IP)

Q.2. Draw and explain protected virtual addressing mode (PVAM) of 80286 microprocessor.

→
1) 80286 is the first processor to support the concepts of virtual memory and memory management.
2) The virtual memory is allocated per task.
3) It address upto 1GB of virtual memory per task.
4) It completes virtual memory is mapped onto the 16MB physical memory i.e. if program is larger than 16MB is

Q.3.

stored on hard disk & is to be executed.

5) The segments are associated with data structure called descriptor.

6) The descriptor contains information of segment.

7) In PVAM 80286 uses 16 bit segment register as a selector to address a descriptor stored in physical memory.

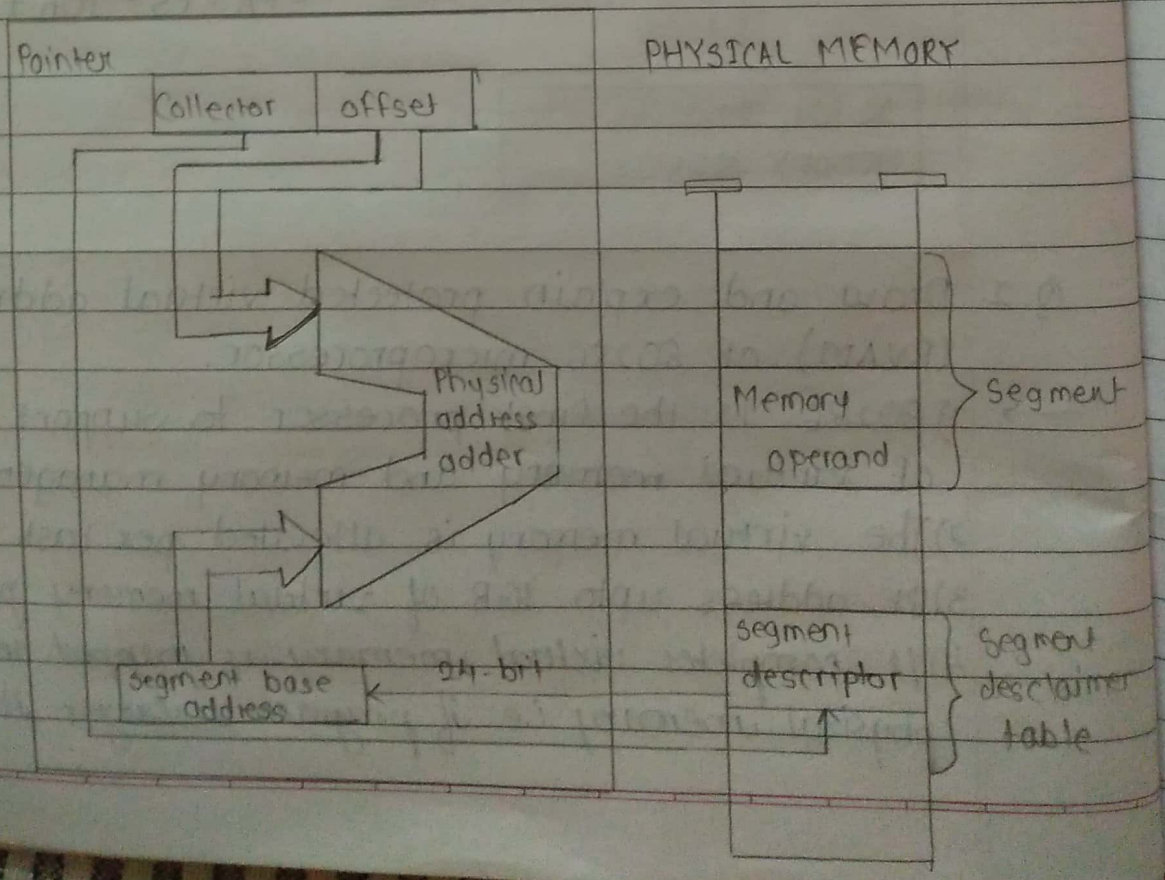
8) Descriptor includes base address, segment limit, segment type privillage level. Segment availability in physical memory.

9) The segment base address is 24 bit that addresses first location in that segment.

10) 24 bit segment base address is added with 16 bit offset to calculated 24 bit physical address.

11) Maximum segment size will be 64KB.

12) 80286 back to its real address mode is by resetting the system.



Q.3. In real mode show the starting and ending addreses of each segment located by following segment register values A) 2345 H B) ABCDH C) 8899H

→ A) 2345 H

Converting into 20 bit,

= 23450 H

23450H + FFFF H = 3344F H

∴ Starting address = 23450H

Ending address = 3344F H

B) ABCDH

Converting into 20bit,

= ABCD0 H

ABCD0 + FFFF = BBCCF

∴ Starting address = ABCD0 H

Ending address = BBCCF H

C) 8899H

Converting into 20bit,

= 88990H

88990 + FFFF = 98988F

∴ Starting address = 88990H

Ending address = 98988F H

Q.4. Write a short note on : Flat mode memory.

→ 1) Pentium-based computer (Pentium 4 or Core2) that uses

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64-bit extensions uses a flat mode memory system.

2) A flat mode memory system is one in which there is no segmentation.

3) The address of first byte in memory is at 00 0000 0000H and last location is at FF FFFF FFFFH (address 40 bits).

4) The flat model does not use segment register to address a location in memory.

5) The CS segment register is used to select a descri-ptor from the descriptor table that defines the access rights of only a code segment.

6) The offset address is actual physical address in 64-bit mode.

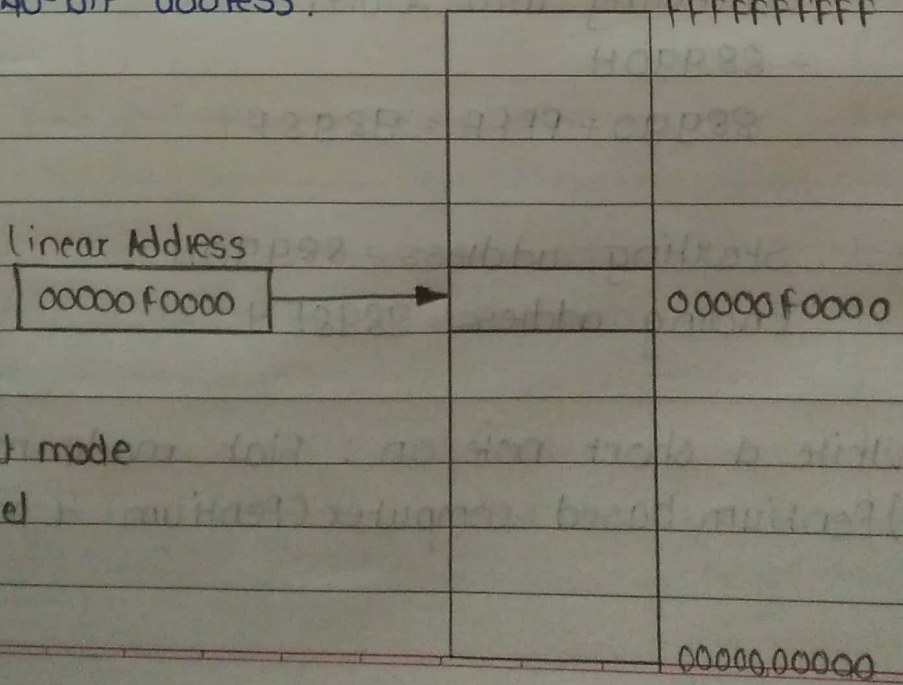
7) The 64-bit descriptor has no limit or base address.

8) The real mode system is not available if processor operates in 64-bit mode.

9) Protection and paging are allowed in 64-bit mode.

10) The CS register is still used in protected mode operation in 64-bit mode.

11) The flat mode memory contains 1T byte of memory using a 40-bit address.




The 64-bit flat mode memory model

Q.5. Describe different data addressing modes with one instruction example.

→ 1) Register addressing:

Register addressing transfers a copy of byte or word from source register or contents of memory location to destination register or memory location.

e.g. mov cx, dx

This instruction copies word-contents of register DX into register CX.

2) Immediate addressing mode

Immediate data is part of instruction.

e.g. mov AX, 1122H

3) Direct addressing mode

16 bit memory address (offset) is directly specified in instruction

e.g. mov ax, [2000]

4) Register indirect addressing mode

Some times the addresses of memory location which contains data is stored in register.

e.g. ax, [bx]

effective address = 10 * DS + [BX]

5) Index addressing mode

Offset of operand is stored in index register.

e.g mov ax,[si]

6) Register relative addressing mode

The effective address is formed by adding 8 bit displacement with content of any register.

e.g. mov ax, 50H [Bx]

7) Based indexed addressing mode

The effective address of data is formed by adding content of base register to the content of index register.

e.g. mov ax, [bx][si]

8) Relative based indexed addressing mode

The effective address is formed by adding 8 bit displacement with sum of contents of base register and index register.

e.g. mov ax, 50H [Bx][si]

Q.6. Describe paging mechanism in 80386 microprocessor with neat diagram.

→ 1) Paging is one of the memory management techniques used for virtual memory multitasking operating system.

2) The segmentation scheme may divide the physical memory into variable, size, segments but, the paging divides the memory into fixed size pages.

3) Paging unit:

PU of 80386 uses a two level table mechanism to convert the linear addresses provided by

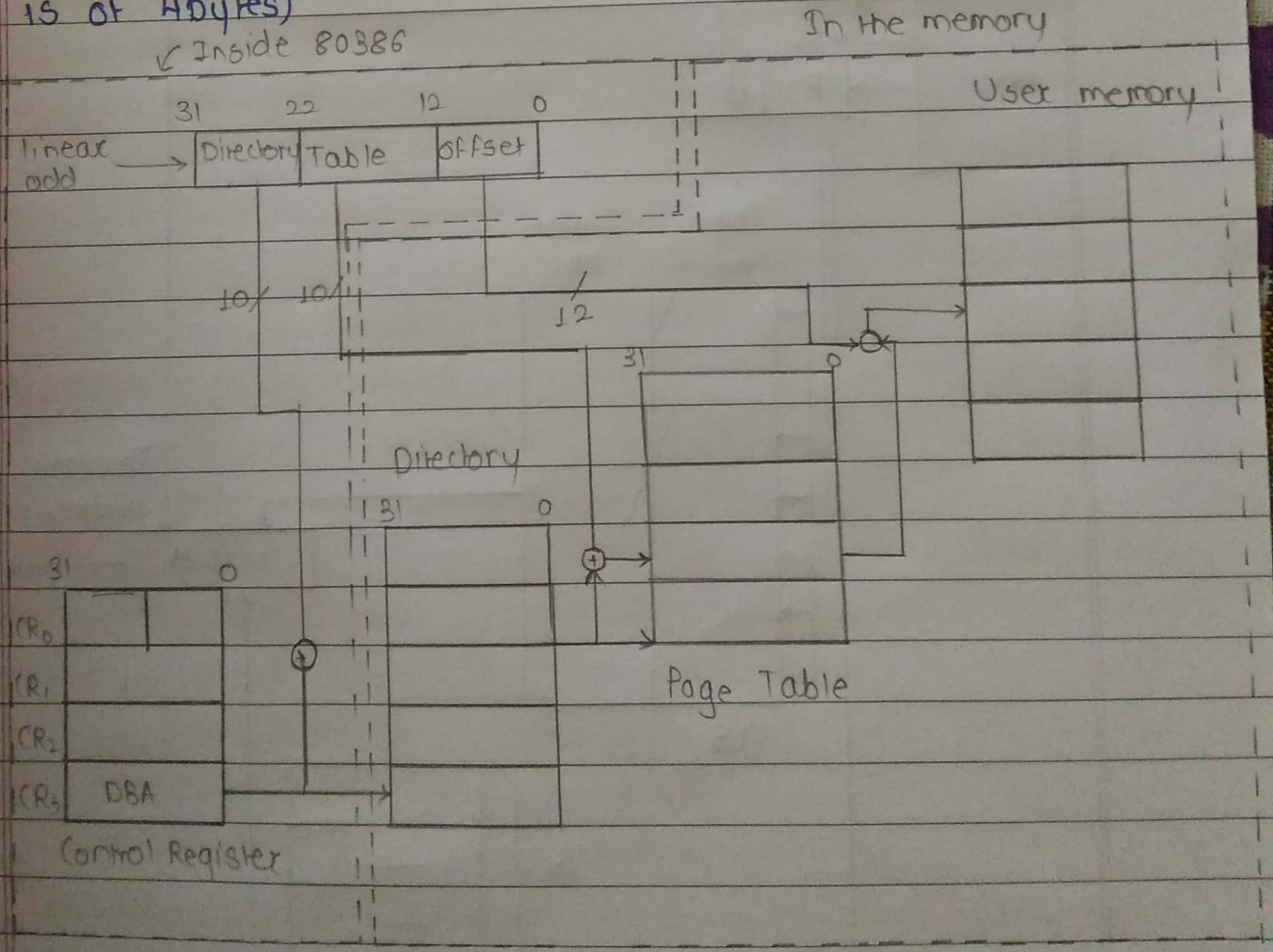
SU (segmentation unit) into physical addresses.

- Paging unit handles every task in terms of three components namely page directory, page tables and the page itself.
- Page Directory:

This is at most 4KB in size. Each directory entry is of 4 bytes. Thus a total of 1024 entries are allowed in directory.

- Page Tables:

Each page table is of 4KB in size and may contain a maximum of 1024 entries (each entry is of 4bytes)



- For converting linear addresses to physical addresses, if conversion process uses the two levels paging for every conversion, a considerable time will be wasted in process.
- To optimize this, a 32 entry page table cache is provided which stores the 32 recently accessed page table entries.
- Whenever, a linear address is to be converted to physical address, it is first checked to see whether it corresponds to any of page table cache entries. This page table cache is also known as TLB.