Assignment No. 4

19UCS122

Q1. Draw & explain real mode addressing of 80286 microprocessors.

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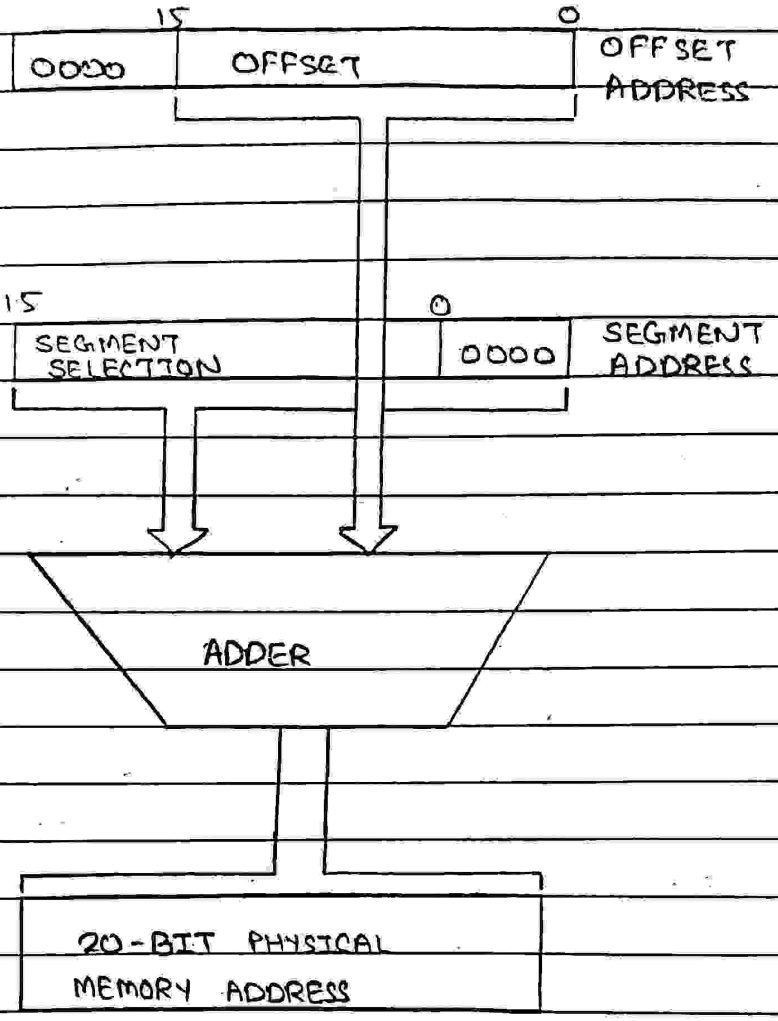

- In real mode, 80286 behaves as a fast 8086.
- Addresses only 1MB of physical memory using A0-A19.
- The lines A20-A23 are not used by the internal circuit of 8028
- 80286 much faster than 8086 in real mode because of extra pipelining & circuit level improvement (80286 is 8 times faster tha 8086).
- 80286 reserve two fixed areas of physical memory for
  - System initialization FFFF0H to FFFFFH
  - Interrupt vector table 00000H to 003FFH
- The program execution starts from FFFF0H after reset & initialization.

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Q2. Draw & explain Protected virtual addressing mode (PVAM) of 80286 Microprocessor.

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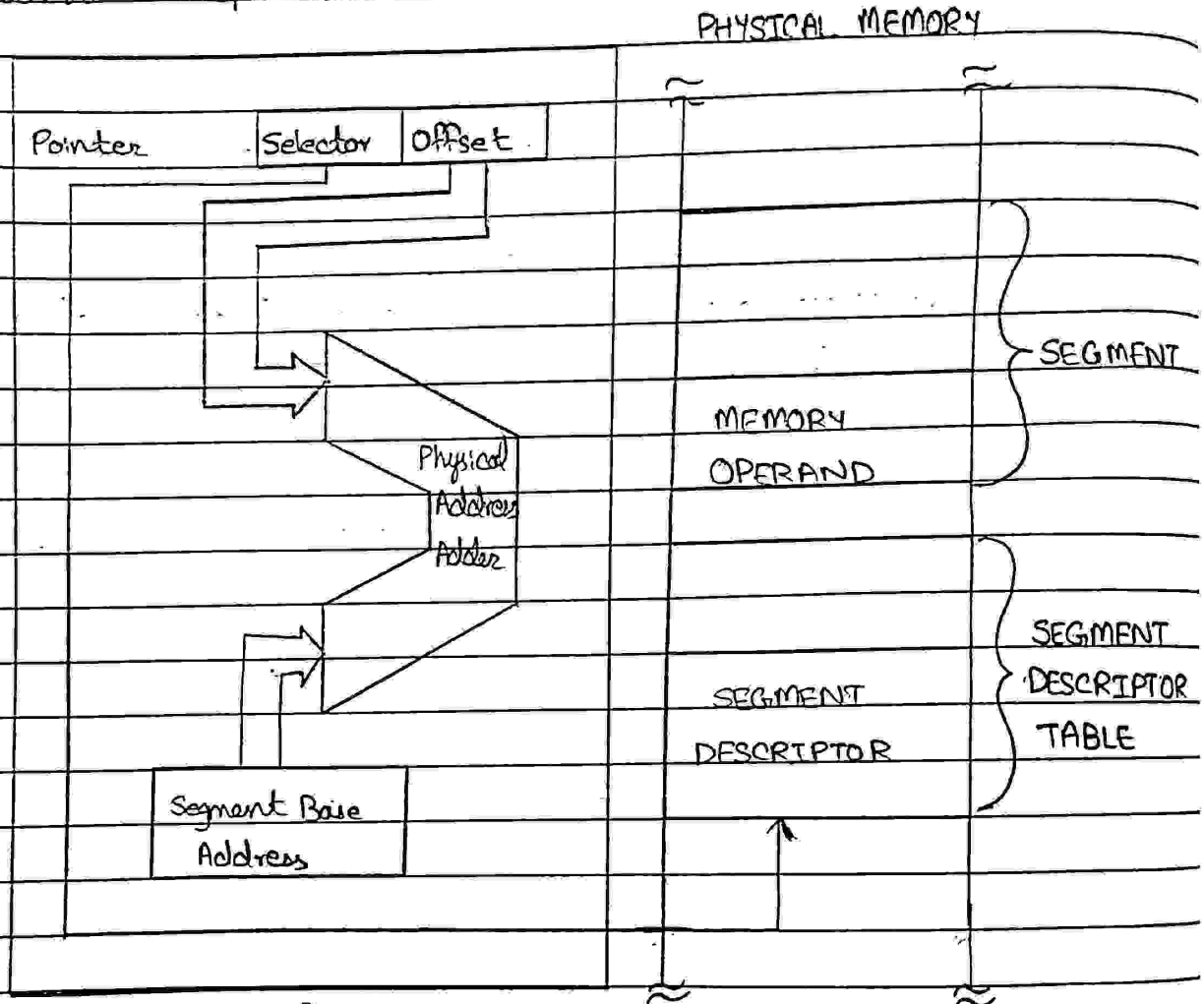

- 80286 is the first processor to support the concept of virtual memory & memory manngment.
- The virtual memory is allotted per task.
- It address up to 1 GB of virtual memory per task.
- Complete virtual memory ~~of~~ is mapped onto the 16 MB physical memory i.e. if program is larger than 16 MB is stored on hard disk & is to be executed.
- The segments are associated with a data structure called a descriptor.
- The descriptor contains informatn of the segment.

- In PVAM 80286 uses 16 bit segment register as a selector to address a descriptor stored in physical memory.
- Descriptor includes base address, segment limit, segment type privilege level, segment availability in physical memory.
- The segment base address is 24 bit that addresses first location in that segment.
- 24 bit segment base address is added with 16 bit offset to calculated 24 bit physical address.
- Maximum segment size will be 64kB.
- 80286 back to its real address mode is by resetting the system.

Q3. In the real mode, Show the starting & ending addressing of each segment located by the following segment register values

a. 2345H

Starting address = Segment register x10H + offset
= 2345x10H + 0000H
= 23450 H

Ending address = Segment register x10H + offset
= 2345x10H + FFFFH
= 3344FF H

b. ABCDH

Starting address = ABCDx10H + 0000H
= ABCD0H

Ending address = ABCDx10H + FFFFH
= BBCCF H

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c. 8899H

→ Starting address = 8899 × 10H + 0000H

= 88990 H

Ending address = 8899 × 10H + FFFFH

= 9898F H

Q4. Write a short note on Flat mode memory.

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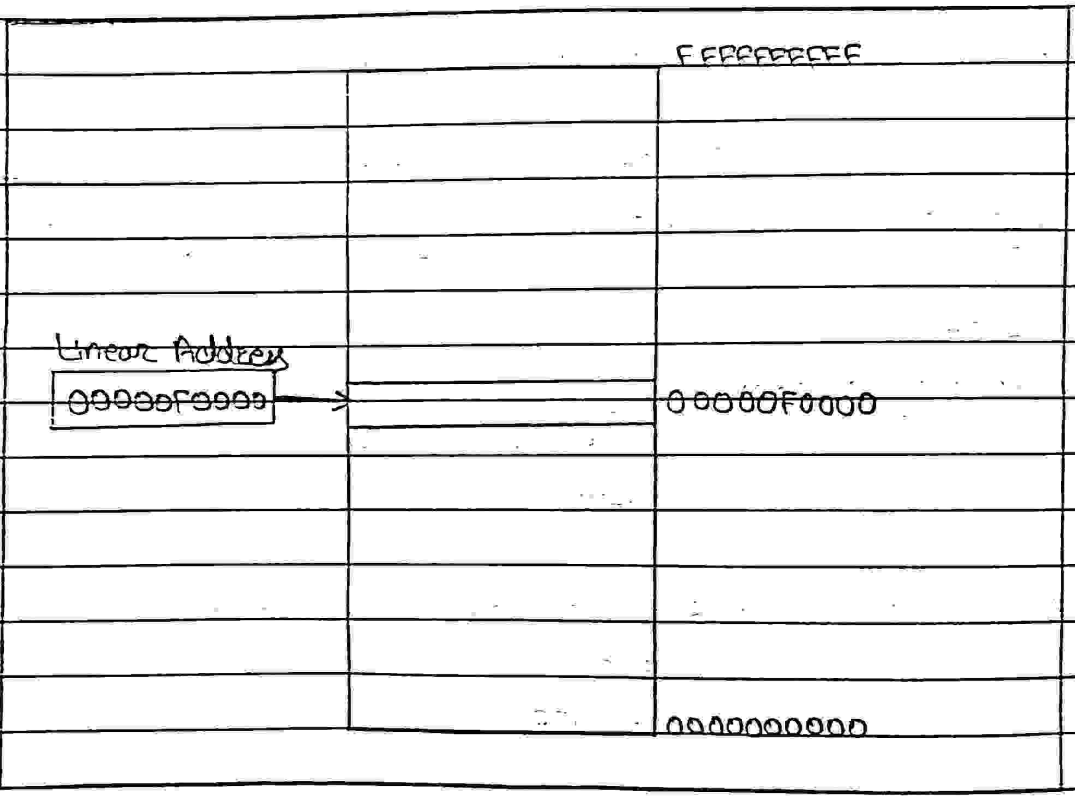


- A flat mode memory system in one which there is no segmentn.
- The address of first byte in memory at 0000000000H & last location is FFFFFFFFF (Address size = 40 bits)
- That flat model does not use segment register to address a locatn in a memory.
- This form of addressing is much easier to understand but offer little protection to the system.

05. Describe different data addressing modes with one instruct^{n} example.

→ Data Addressing Mode
- Immediate addressing mode
- Register addressing mode
- Direct addressing mode
- Register indirect addressing mode.
- Index addressing mode
- Register relative addressing mode
- Based indexed addressing mode
- Relative based indexed addressing mode.

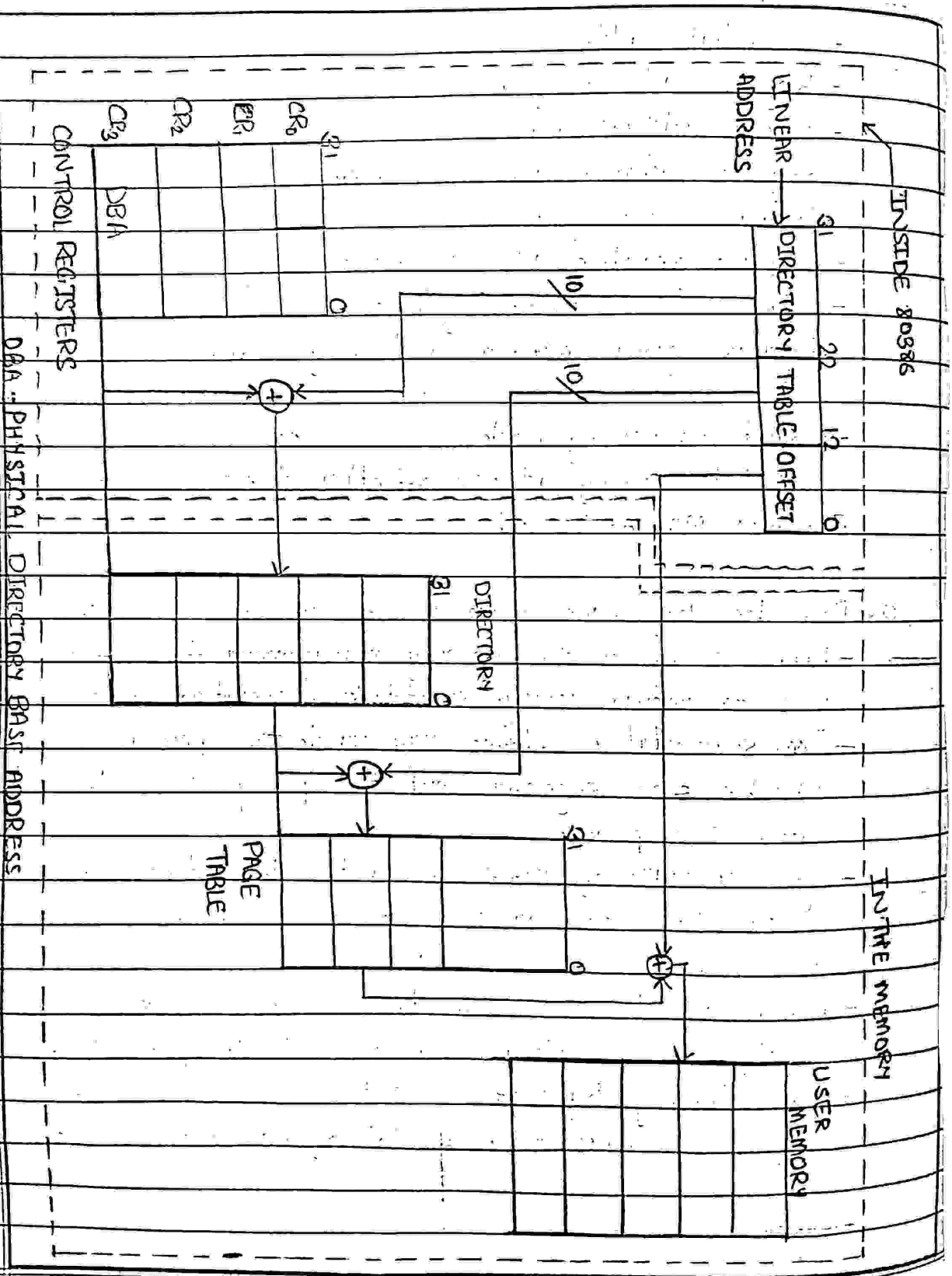
- Direct addressing mode
  16 bit memory address (offset) is directly specified in instruct^{n}.

Example: MOV AX, [2000]

06. Describe Paging Mechanism in 80386 Microprocessor with neat diagram.

→ - Paging is one of the memory management ~~technolo~~ techniques used for virtual memory multitasking operating system.
- The segmentation scheme may divide the physical memory into variable size segments but the paging divides the memory into fixed size pages.
- Paging unit: PU of 80386 uses a two level table mechanism to convert the linear addresses provided by SU into physical addresses.
- Paging unit handles every task in terms of ~~these~~ three components namely page directory, page tables & the page itself.
- Paging directory: This is at the most 4 kB in size & each directory entry is of 4 bytes, thus a total of 1024 entries are allowed in a directory.

-Page table: Each page is of 4kB in size & may contain a maximum of 1024 entries. (Each entry is of 4 bytes.



- For converting linear addresses to physical addresses, if the conversion process uses the two levels paging for every conversion, a considerable time will be wasted in the process.
- To optimize this, a 32 entry page table cache is provided which stores the 32 recently accessed page table entries.
- Whenever a linear address is to be converted to physical address, it is first checked to see whether it corresponds to any of the page table cache entries. This page table cache is also known as TLB.