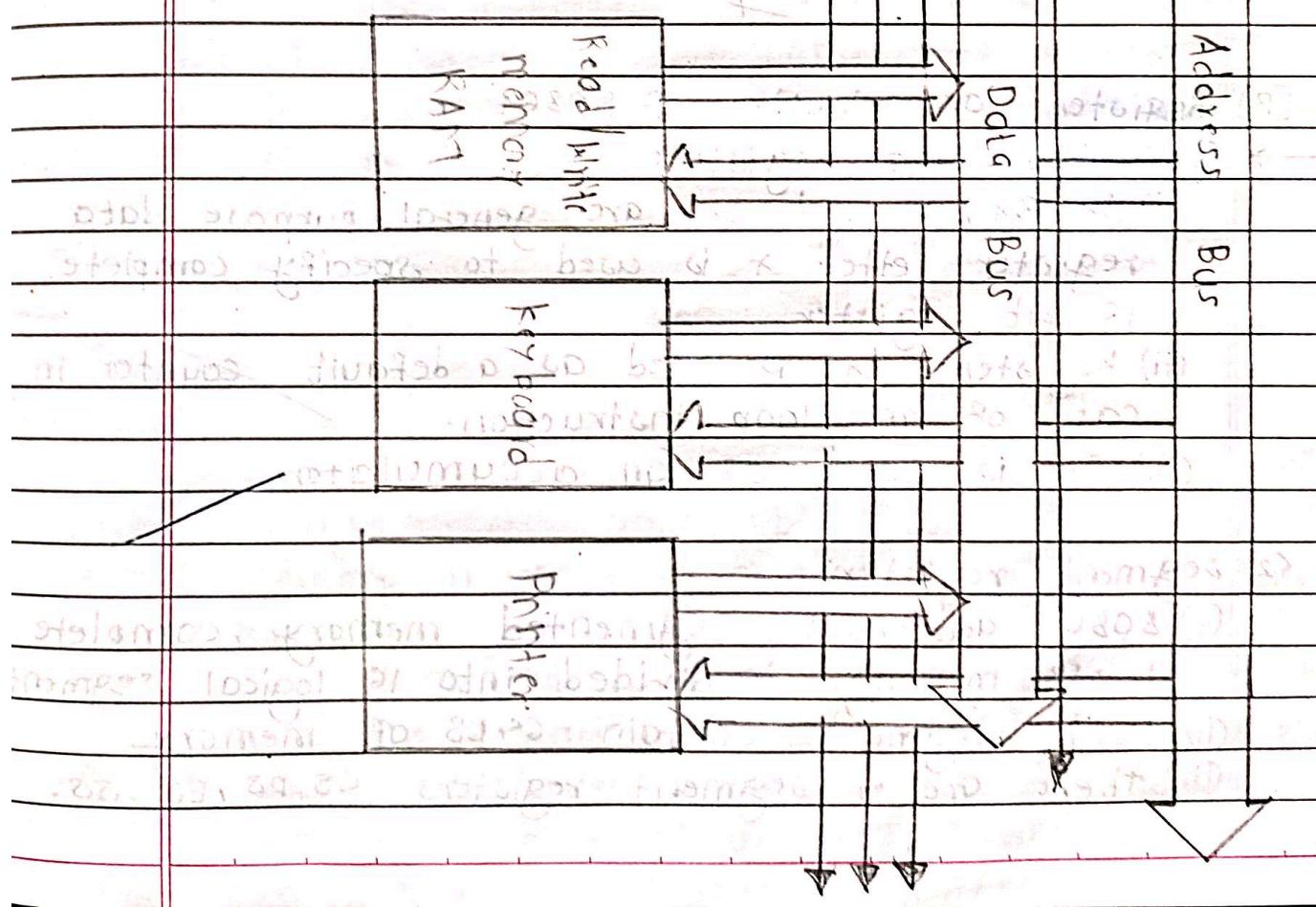
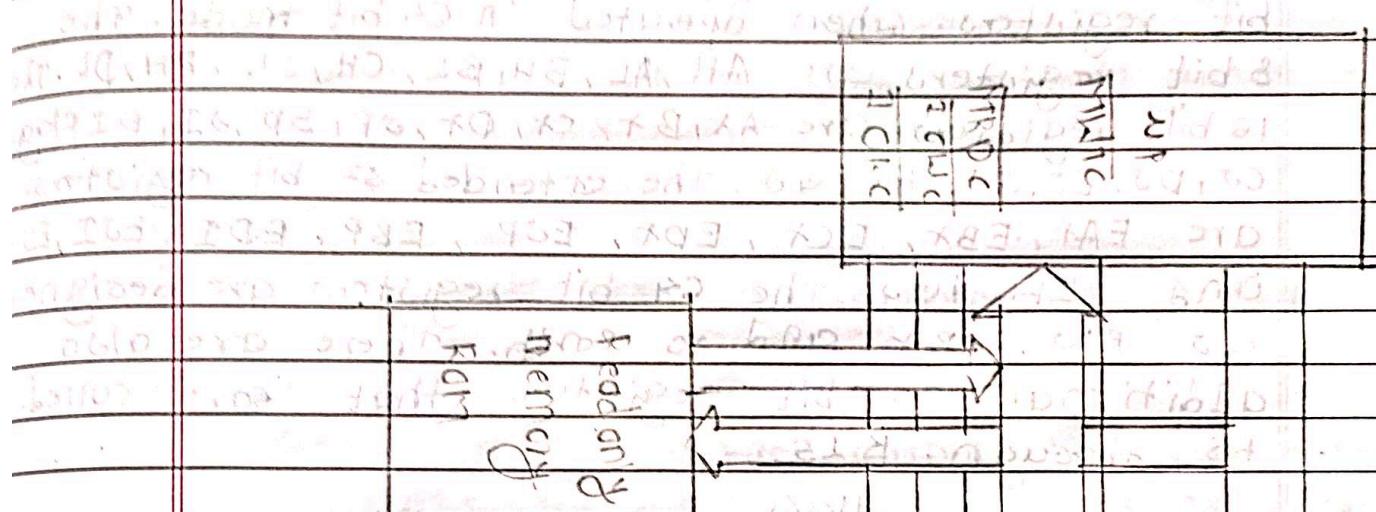


Assignment No: 1

Microprocessor Architecture.



Q1.) Draw block diagram of computer system showing address, data and control bus structure.



Q.2) Write short note on:

[A] Programming model :-

→ The programming model contains 8-, 16-, 32 bit registers. The pentium & core 2 also contain 64 bit registers. When operated in 64 bit mode. The 8 bit registers are AH, AL, BH, BL, CH, CL, DH, DL. The 16 bit registers are AX, BX, CX, DX, SP, BP, SI, DI, DS, ES, SS, FS, GS. The extended 32 bit registers are EAX, EBX, ECX, EDX, ESP, EBP, EDI, ESI, EIP and EFL AGS. The 64 bit registers are designed as RAX, RBX, and so forth. There are also additional 64 bit registers that are called R8 through R15.

diag

[B] Register organisation of 8086:

→ (1) General data register:

(i) AX, BX, CX and DX are general purpose data register. Letter X is used to specify complete 16 bit register.

(ii) Register CX is used as a default counter in case of a loop instruction.

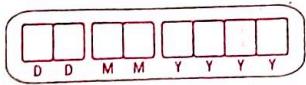
(iii) AX is used as an accumulator.

(2) Segment register:

(i) 8086 addresses segmented memory, complete 1 MB memory is divided into 16 logical segments.

(ii) Each segment contains 64 KB of memory.

(iii) There are 4 segment registers: CS, DS, ES, SS.



(a) CS :- code segment of memory where all executable program is stored.

(b) DS :- Data segment of memory when the data is resides.

(c) ES :- It is a segment which is another data segment of memory.

(d) SS :- It is a segment which is used to store stack data.

(3) Flag Register:

(i) It indicate result of computation of ALU.

(4) Pointer & Index Register:

(i) Pointer contain offset within the particular segments. Index register are used as general purpose registers as well as for offset storage.

(ii) DI is used to store offset of source data in data segment while DI is used to store offset of destination data in segment.

	AX	AH	AL	DL	DS	CS
	BX	BH	BL		DS	Flags / PSW
	CX	CH	CL		ES	
	DX	DH	DL		SS	

[C] Memory Segmentation of 8086

→ (1) Memory in 8086 is organised as segmented memory.

(2) 16 bit contents of segment register points to starting location of a particular segment to address a specific memory location within a segment, we need an offset. Offset is also 16 bit ranging from 0000H to FFFFH.

D	D	M	M	Y	Y	Y	Y
---	---	---	---	---	---	---	---

- (3) physical addresses range from 00000H to FFFFFH
- (4) Advantages of segmented memory scheme.
- (i) Allow memory capacity. 1MB through actual addresses are 16 bits.
 - (ii) Allow placing of code, data and stack portion of same program in different seg.
 - (iii) Permit program and its data to put into different areas of memory. each time, program is executed.

[D] 8086 flag Registers:

→ It has 16 bit flag Registers. divided into two parts : (1) status Flag & (2) control Flag.

(1) Trap Flag: If this flag is set, the processor enters the single step execution mode. A trap is generated after execution of each instruction.

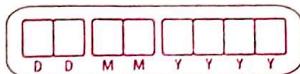
(2) Interrupt Flag: If this flag is set maskable interrupts are recognised by the CPU.

(3) direction Flag: This is used for string manipulation. If this flag is reset string is processed from lowest to highest address.

If this flag is set, string is processed from highest to lowest address.

(4) Overall flag: this flag is set if an overflow occur. If the result of signed operation is larger enough to be accommodated in a destination register.

15	14	13	12	11	10	9	8	7	C	5	4	3	2	1	0
x	x	x	x	0	D	I	T	S	2	x	A	c	x	P	x



Q3 Describe Internal Architecture of 8086 microprocessor with neat diagram

→ 8086 microprocessor is divided into 2 parts

(i) BIU

- (i) It contains circuit for physical address calculation and pre decoding instruction byte queue (6 bytes)
- (ii) This unit is responsible for establishing comm. with external devices and peripherals including memory.
- (iii) complete physical address, 20-bit is generated using segment register & offset register, each 16 bit.

(ii) EU

- (i) It contains register set of 8086 except segment registers and IP.
- (ii) It has 16-bit ALU to perform Arithmetic and logical operations.
- (iii) The decoding unit decodes opcode bytes issued from the instruction byte queue.
- (iv) Timing and control units issue necessary control signals to execute the instruction opcode received from instruction byte queue.
- (v) The EU pass the result to BIU for storing them in memory.

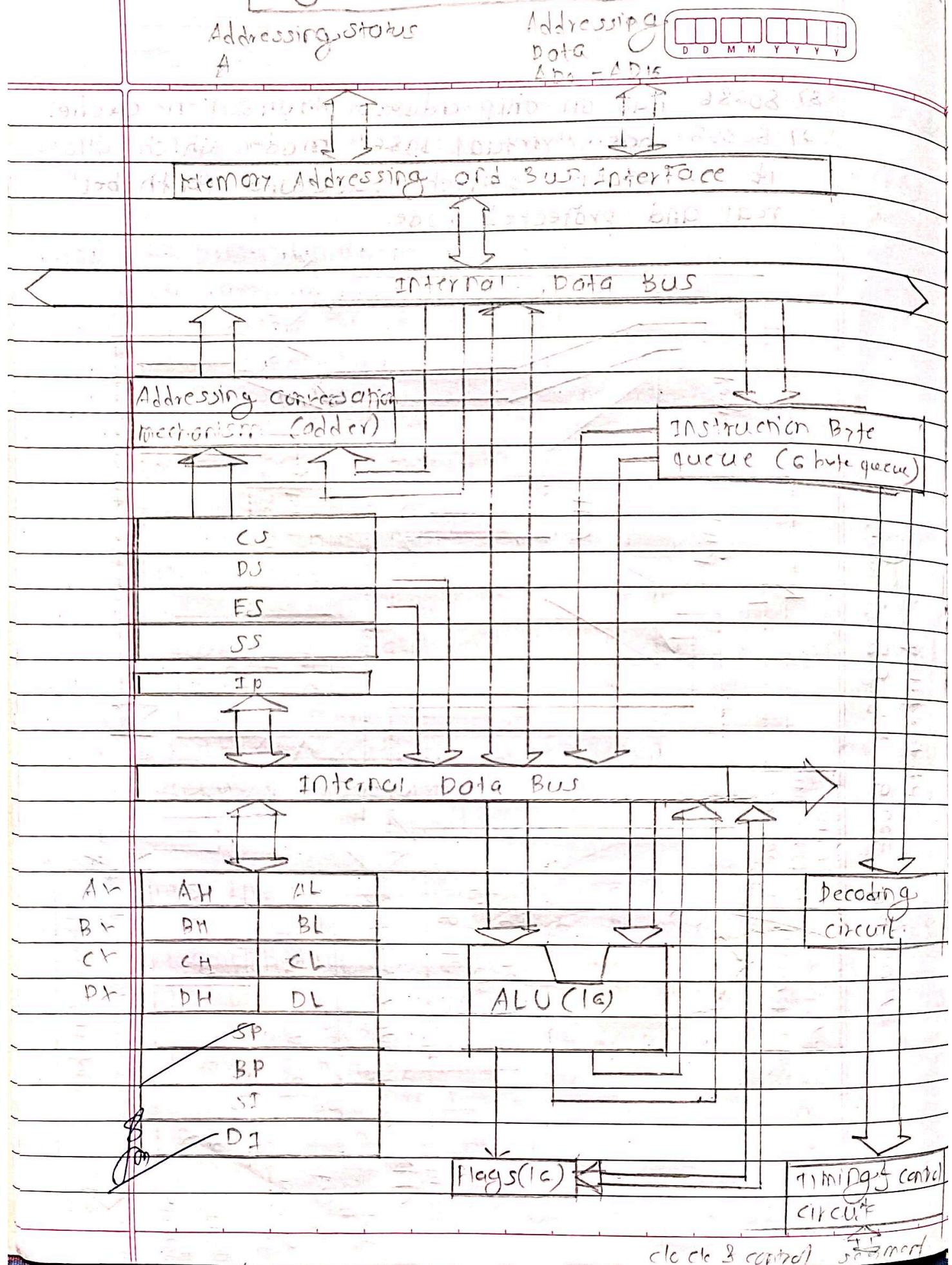
Q4 Describe internal architecture of 80286 microprocessor with neat diagram

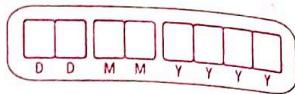
→ It contains four functional units

(i) Address Unit (AU) performs address calculations.

→ The address unit (AU) computes the physical address that will be sent out to memory.

Fig : 8086 Architecture





- 80286 operates in two memory address mode
- (1) Real address mode (1 MB)
 - (2) Protected or virtual address mode (1 GB)

(3) Bus Unit :-

It performs

- All memory & I/O read & writes.
- Pre-fetches of data to & from RAM
- Pre-fetches of instruction bytes
- Control transfer of data to & from coprocessor (80287)

(4) Instruction Unit :

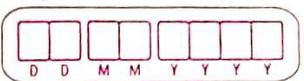
- It decodes up to three pre-fetched instructions and hold them in queue, where execution unit can access them.

(5) Execution Unit :

- The execution unit uses its 16 bit ALU to execute instructions it receives from instruction unit.

Q5 List the features of 80386 microprocessor

- (1) 32 bit processor that supports 32/16/32 bit data operations
- (2) compatibility with existing processor like 80286 etc.
- (3) 32 bit ALU
- (4) No. of segments = 16384, size = 4 GB
- virtual address space = 64 Tera bytes
- (5) physical memory size = 5 GB
- (6) The 80386 can be supported by 80387 for mathematical data processing
- (7) The concept of paging is introduced in 80386, size of each page is 4 KB under the segment memory.



- (8) 80286 has on chip address translation cache.
 (9) 80286 has "virtual 8086" mode, which allow it to easily switch back and forth bet real and protected mode.

