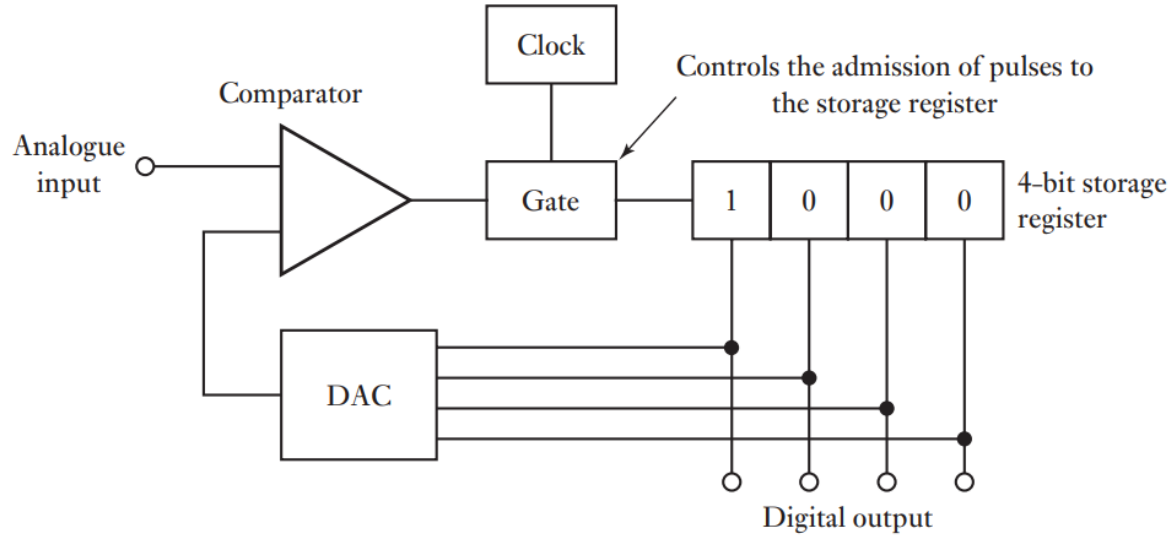
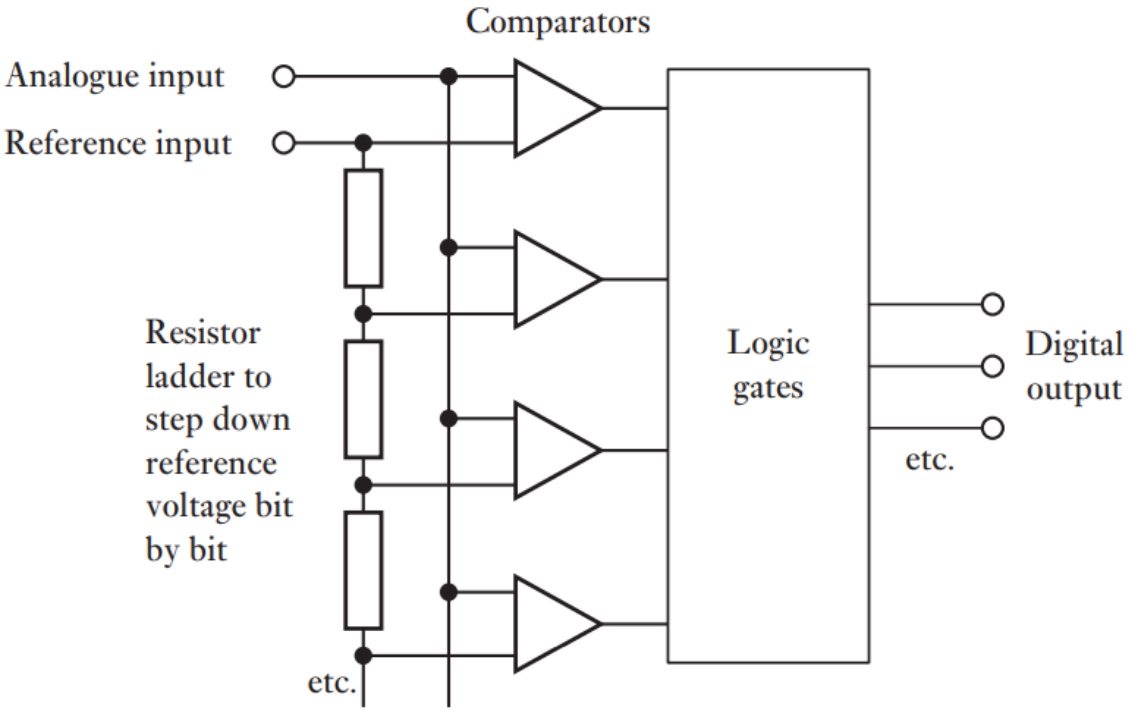


ADC

- ADCs The input to an ADC is an analogue signal and the output is a binary word that represents the level of the input signal.
- There are a number of forms of ADC, the commonest being successive approximations, ramp, dual ramp and flash.
- Successive approximations is probably the most commonly used method.
- Figure 4.9 illustrates the subsystems involved.
- A voltage is generated by a clock emitting a regular sequence of pulses which are counted, in a binary manner, and the resulting binary word converted into an analogue voltage by a DAC.
- This voltage rises in steps and is compared with the analogue input voltage from the sensor.
- When the clock-generated voltage passes the input analogue voltage, the pulses from the clock are stopped from being counted by a gate being closed.
- The output from the counter at that time is then a digital representation of the analogue voltage.
- While the comparison could be accomplished by starting the count at 1, the LSB, and then proceeding bit by bit upwards, a faster method is by successive approximations.

- This involves selecting the MSB that is less than the analogue value, then adding successive lesser bits for which the total does not exceed the analogue value.
- For example, we might start the comparison with 1000. If this is too large we try 0100. If this is too small we then try 0110. If this is too large we try 0101.
- Because each of the bits in the word is tried in sequence, with an n-bit word it only takes n steps to make the comparison.
- Thus if the clock has a frequency f, the time between pulses is 1/f .
- Hence the time taken to generate the word, i.e. the conversion time, is nf. Figure 4.10 shows the typical form of an 8-bit ADC (GEC Plessey ZN439) designed for use with microprocessors and using the successive approximations method.
- Figure 4.11 shows how it can be connected so that it is controlled by a microprocessor and sends its digital output to the microprocessor.
- All the active circuitry, including the clock, is contained on a single chip.
- The ADC is first selected by taking the chip select pin low.
- When the start conversion pin receives a negative-going pulse the conversion starts.
- At the end of the conversion the status pin goes low.
- The digital output is sent to an internal buffer where it is held until read as a result of the output enable pin being taken low.



The flash ADC

- The flash ADC is very fast. For an n-bit converter, 2n 2 1 separate voltage comparators are used in parallel, with each having the analogue input voltage as one input (Figure 4.14).
- A reference voltage is applied to a ladder of resistors so that the voltage applied as the other input to each comparator is 1 bit larger in size than the voltage applied to the previous comparator in the ladder.
- Thus when the analogue voltage is applied to the ADC, all those comparators for which the analogue voltage is greater than the reference voltage of a comparator will give a high output and those for which it is less will be low.
- The resulting outputs are fed in parallel to a logic gate system which translates them into a digital word.
- In considering the specifications of ADCs the following terms will be encountered.

- 1 Conversion time, i.e. the time required to complete a conversion of the input signal.
- It establishes the upper signal frequency that can be sampled without aliasing; the maximum frequency is 1 (2 3 conversion time2. 2 Resolution, this being the full-scale signal divided by 2n , where n is the number of bits.
- It is often just specified by a statement of the number of bits. 3 Linearity error, this being the deviation from a straight line drawn through zero and full-scale.
- It is a maximum of 61 2 LSB