4. How the degree of memory conflicts is not encountered in loosely coupled multiprocessor systems? Draw and explain Non-hierarchical loosely coupled multiprocessor system.

Loosely coupled multiprocessor system do not generally encounter the degree of memory conflict experienced by tightly coupled system. In such systems, each processor has a set of input-output devices and a large local memory where it accesses most of instructions and data. We refer to the processor, its local memory and I/O interfaces as a computer module. Processes which execute on a different computer modules communicate by exchanging message through a message-transfer (MTS). The degree a coupling in such system is very loose. Hence it if often referred to as a distributed system. The determinant factor of the degree of coupling if the communication topology of the associated message transfer system.

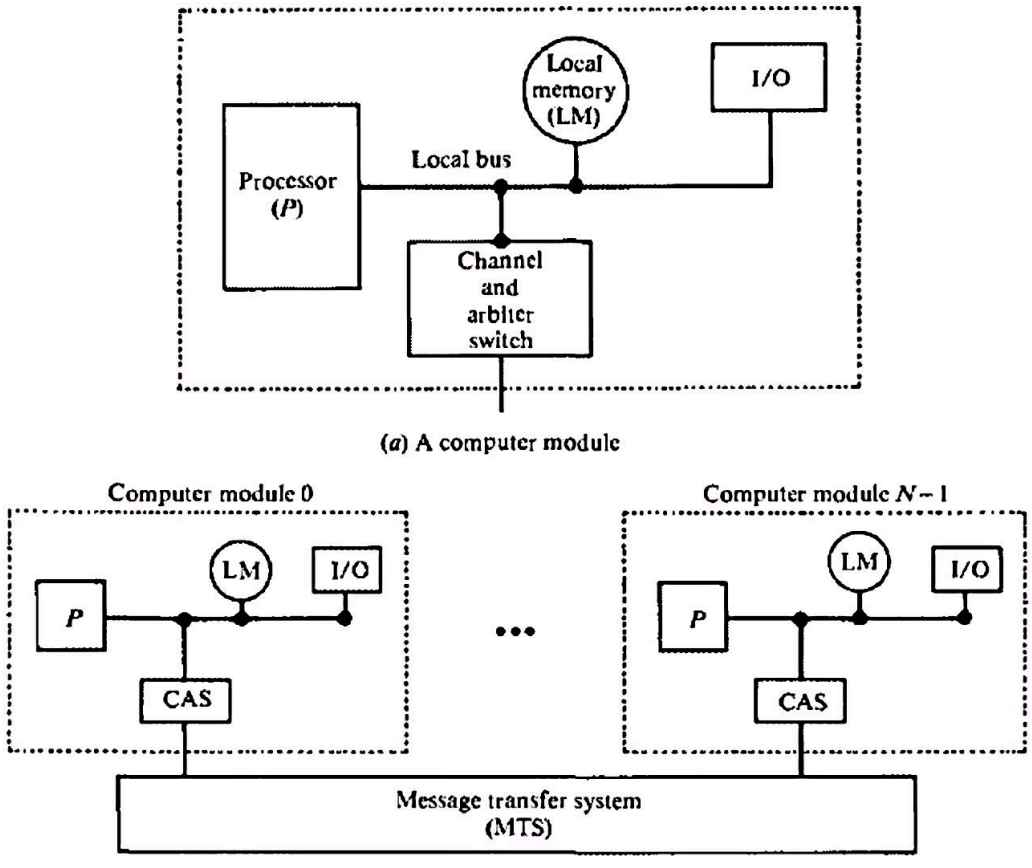
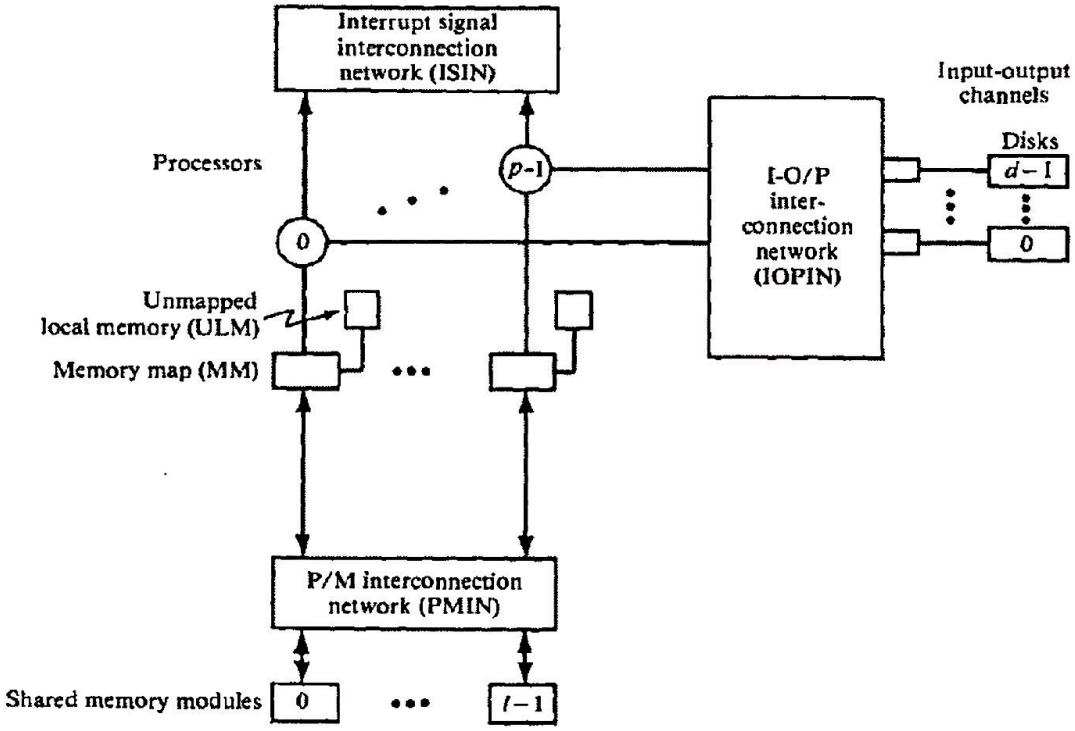


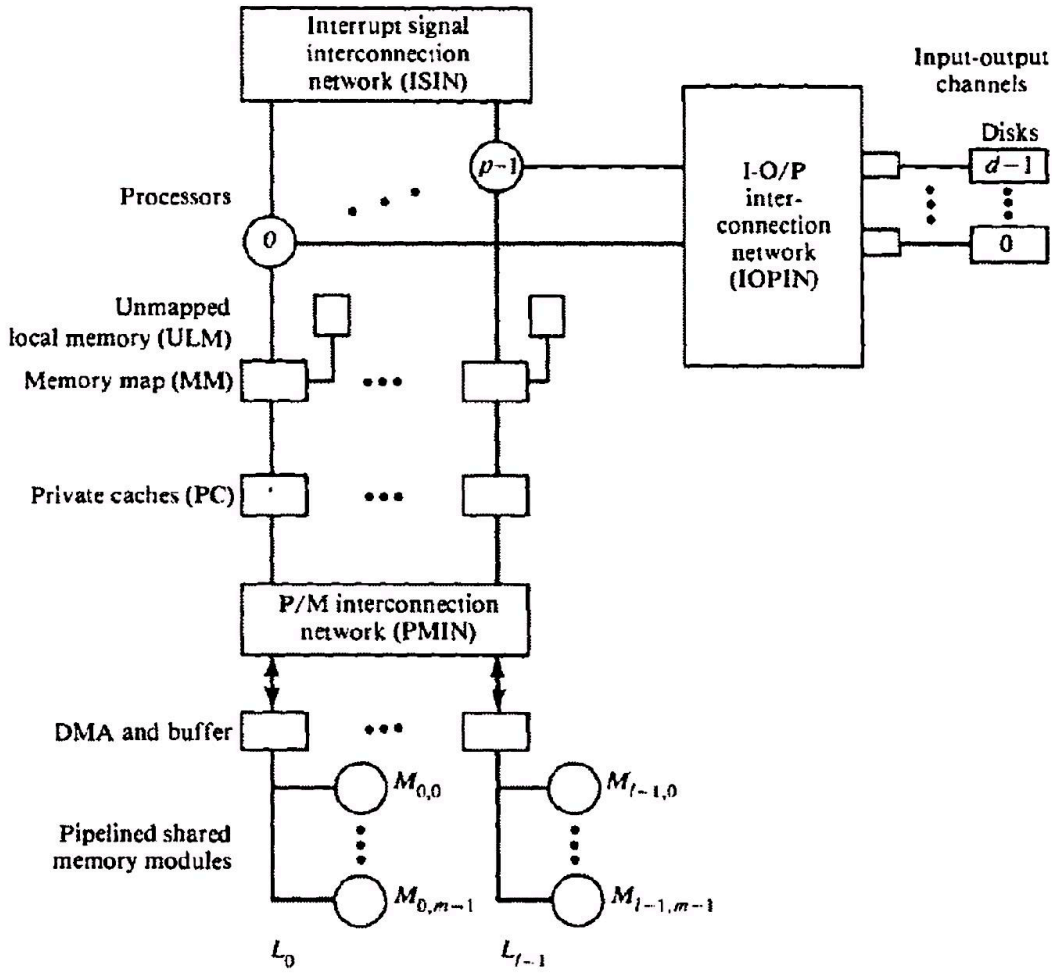
Figure: - Non- hierarchical loosely coupled multiprocessor system.

a. Figurer (a) shows a computer module of a non-hierarchical loosely coupled multiprocessor system
b. It consist of a processor, a local memory, local input-output devices and an interface to another computer module. The interface may contain a channel and arbiter switch (CAS).
c. Figure (b) shows the connection between the computer modules and a message-transfer system.
d. If request from two or more different computer modules collide in accessing a physical segment of the MTS, the arbiter is responsible for choosing one of the simultaneous request according to a given service discipline. It is also responsible for delaying other request until the serving of the selected request is completed.
e. The channel within the CAS may have high speed communication memory which is used for buffering block transfer of message. The communication memory is accessible by all processors.
f. The message transfer system for a non-hierarchical Loosely Coupled multiprocessor System could be a simple time shared bus, as in the PDP-11, or a shared memory system.
g. The letter case can be implemented with a set of memory modules and a processor-memory interconnection network or a multiport main memory.

3. **Why tightly coupled systems are preferred for high speed and real time processing? Draw and explain tightly coupled multiprocessor configuration.**



(*a*) Without private cache



(*b*) With private cache

a. Above figure shows the tightly coupled multicomputers system configuration.

b. In this system the processor shares clock generator, bus control logic, entire memory and I/O system.
c. This system communicate through memory.
d. One of the limitation of this system is the performance degradation due to memory contentions which occur when two or more processors attempts the same memory simultaneously.
e. When high speed of real-time processing is desired, this system may be used.
f. This tightly coupled multicomputer system is divided into two different models
   i) Tightly coupled multicomputers without private cache.
   ii) Tightly coupled multicomputers with private cache.

i) Tightly coupled multicomputers without private cache.
   a. The above figure (a) show the tightly coupled multicomputer without private cache.
   b. This system is consist of following things
      1) *p* processor
      2) *l* memory modules
      3) *d* input-output channel.
   c. These units are connected through a set of three interconnection network namely, the processor memory interconnection networks (PMIN), the I/O processor interconnection network (IOPIN), the interrupt-signal interconnection network (ISIN).
   d. The PMIN is a switch which is used to connect every processor to every memory module
   e. The IOPIN is used to allow a processor to communicate with the I/O channel which is connected to I/O devices.
   f. The ISIN is used for two purpose: To direct an interrupt to any other inter-processor network and to initiate hardware alarm in case of processor failure.
   g. There are no separate private cache memory to any processor.

ii) Tightly coupled multicomputers with private cache.
   a. In previous module each memory reference goes through the PMIN, it encounters delay in the processor or memory switch and hence the instruction cycle time is increases.
   b. It reduces system throughput. This delay can be reduced by associating a cache with each processor.
   c. The advantage of the cache is that the traffic through the crossbar switch can be reduced.
   d. More than one inconsistent copy of data may exist in the system as this multicomputer system encounters cache coherence problem