HPCA

Q.1. Architectural classification scheme.

→ There are three computer architectural classification schemes -

① Flynn's classification (1966) - based on multiplicity of instruction stream & data stream

② Feng's scheme (1972) - based on serial vs parallel processing

③ Handler's classification (1977) - determined by degree of parallelism & pipelining in various subsystem levels.

A] Flynn's classification -

① The essential computing process is execution of a sequence of instrⁿ on a set ~~of~~ of data.

② The term stream denotes sequence of items as executed or operated upon by a single processor.

③ An instrⁿ stream is sequence of instrⁿ as executed by machine.

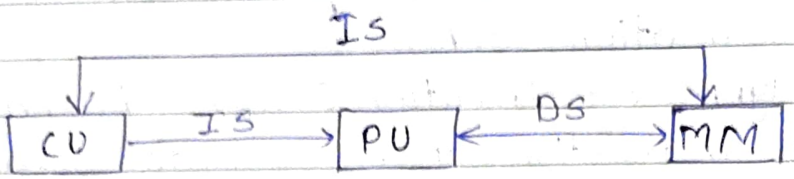
④ Data stream is sequence of data including input, partial or temporary results, called for by instrⁿ stream.

⑤ Both instrⁿ & data are fetched from the memory modules. Instructions are decoded by control unit which sends the decoded instrⁿ stream to processor units for execution. Data streams flow betⁿ processors & memory bidirectionally.

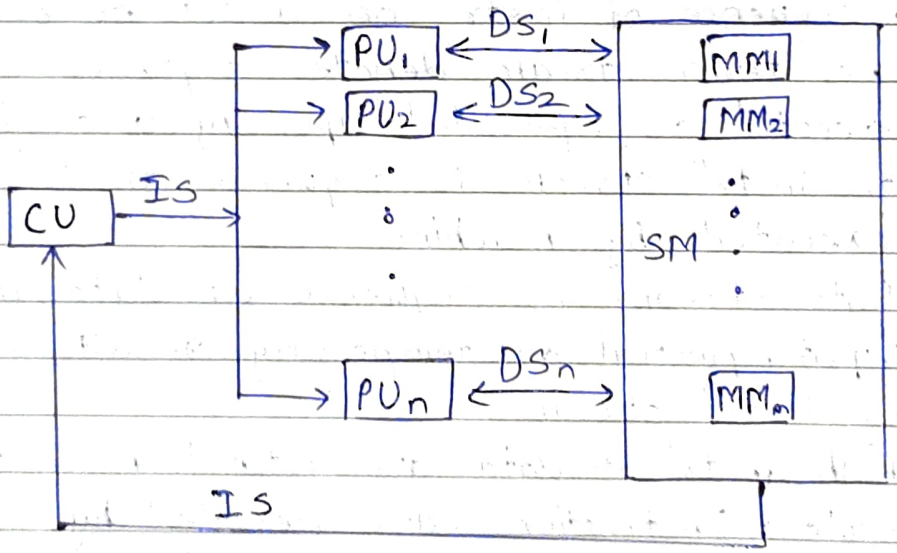
⑥ There are four Flynn's machine organizations:-

1) Single instrⁿ stream - single data stream (SISD) - Instrⁿ are executed sequentially but may be overlapped in their execution stages. Most SISD uniprocessor systems are pipelined. An SISD computer may have more than one

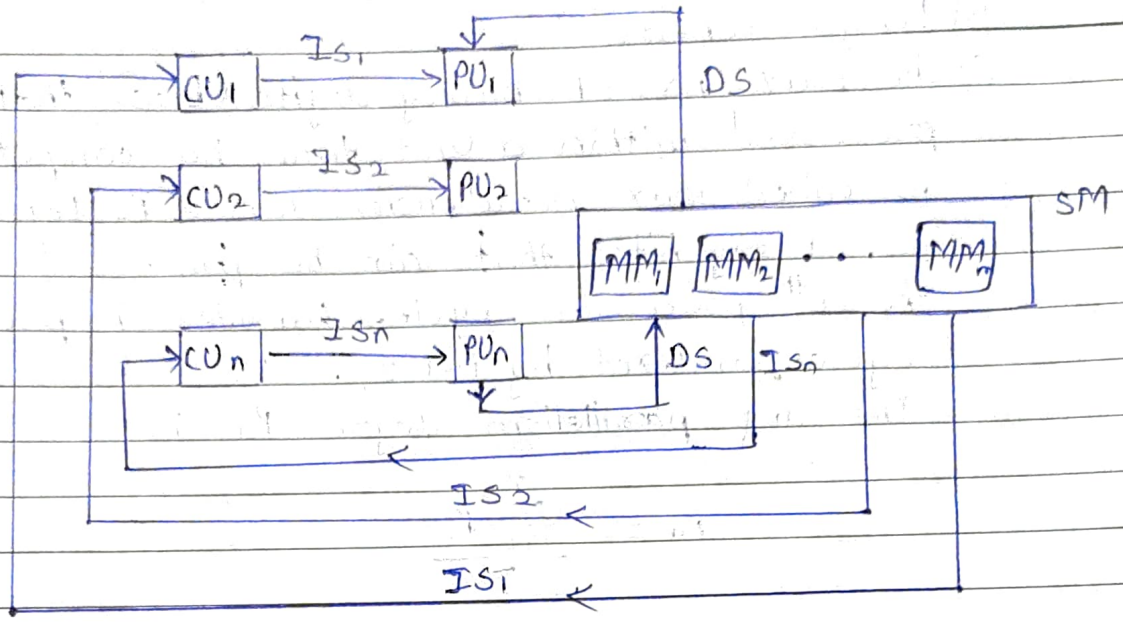
functional unit in it. All the functional unit are under supervision of one control unit.



2) Single instr^n stream - multiple data stream (SIMD)-
There are multiple processing elements supervised by the same ~~controlling~~ control unit. All PUs receive same instr^n broadcast from control unit but operate on different data sets from distinct data stream. The shared memory subsystem may contain multiple modules.



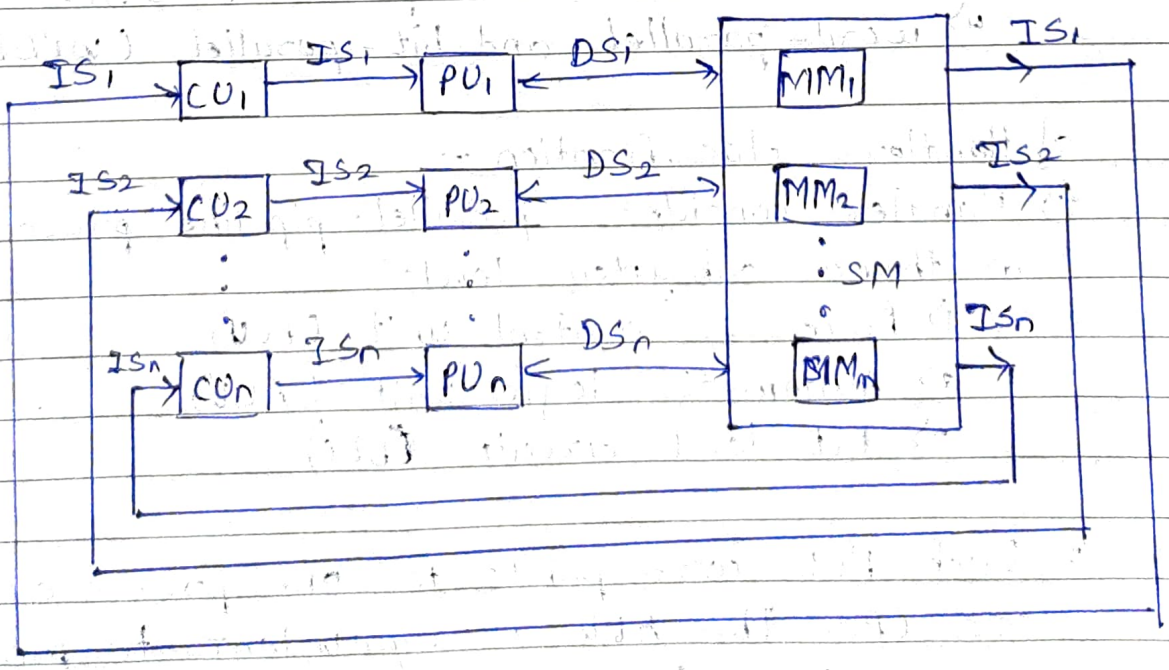
3) Multiple instr^n stream - single data stream (MISD)-
There are n processor units, each receiving distinct instructions operating over the same data ~~stream~~ & its derivative. The output of one processor become the input of next processor in micropipe.



4) Multiple instr^{n} ~~stream~~ stream - multiple data stream (MIMD) -

Most multiprocessor systems & multiple computer systems can be classified in this category.

MIMD computer implies interactions among n processors ~~bec~~ because all memory streams are derived from some data space shared by all processors.



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B] Feng's scheme

① The max no. of binary digits (bits) that can be processed within a unit time by computer system is called max parallelism degree P. Let P_i be no. of ~~big~~ bits that can be processed within the i^{th} processor cycle. Consider T processor cycles indexed by $i = 1, 2, \ldots T$.
The avg parallelism degree P_a is

$$P_a = \frac{\sum_{i=1}^{T} P_i}{T}$$

② Utilization rate μ of computer system within T cycles is

$$\mu = \frac{P_a}{P} = \frac{\sum_{i=1}^{T} P_i}{T \cdot P}$$

③ There are four types of processing methods -
1) word-serial and bit-serial (WSBS)
2) word-parallel and bit-serial (WPBS)
3) word-serial and bit-parallel (WSBP)
4) word-parallel and bit-parallel (WPBP)

c] Handler's classification -

① Handler considers parallel-pipeline processing at three subsystem levels:
1) Processor control unit (PCU)
2) Arithmetic logic unit (ALU)
3) Bit-level circuit (BLC)

② Each PCU corresponds to one processor or one CPU. The ALU is equivalent to processing element (PE). The BLC corresponds to the

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combinational logic circuitary needed to perform 1-bit operations in ALU.

(3) A computer system C can be characterized by triple containing six independent entities.

$T(C) = \langle K \times K', D \times D', W \times W' \rangle$

where K = no. of processors
K' = no of PCU that can be pipelined
D = no. of ALU
D' = no. of ALU that can be pipelined
W = word length of ALU
W' = no. of pipeline stages in all ALUs.

Q.2. Speedup in linear pipelining.

→ (1) The pipeline consists of cascade of processing stages. The stages are pure combinational circuits performing arithmetic or logic operations over the data stream flowing through pipe.

(2) The stages are separated by high-speed interface latches. The latches are fast registers for holding the intermediate results bet^n stages.

(3) We define speedup of a k-stage linear pipeline processor over an equivalent nonpipeline processor as

$$S_k = \frac{T_1}{T_k} = \frac{n \cdot k}{k + (n-1)}$$

(4) Max speedup is $S_k \to k$, for $n >> k$. That is, max speedup a linear pipeline can provide is k, where k is no. of stages in pipe.

(5) This max speedup is never fully achievable because of data dependencies bet^n instr^n, interrupts, program branches & other factors.

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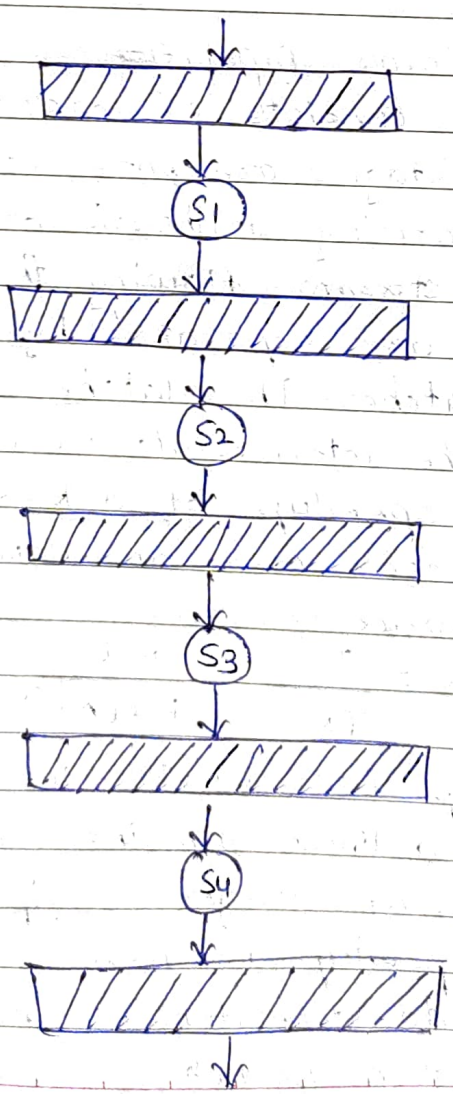
⑥ Many pipeline cycles may be wasted on a waiting state caused by out-of-sequence instr^{n} execution.

2.5 Uniform classification of pipeline processors.

→ According to levels of processing, Handler has proposed following classification scheme for pipeline processors -

1] Arithmetic pipeline -

The arithmetic logic units of a computer can be segmentized for pipeline operations in various data formats. Examples are: four-stage pipes used in Star-100, eight-stage pipes used in TI-ASC.



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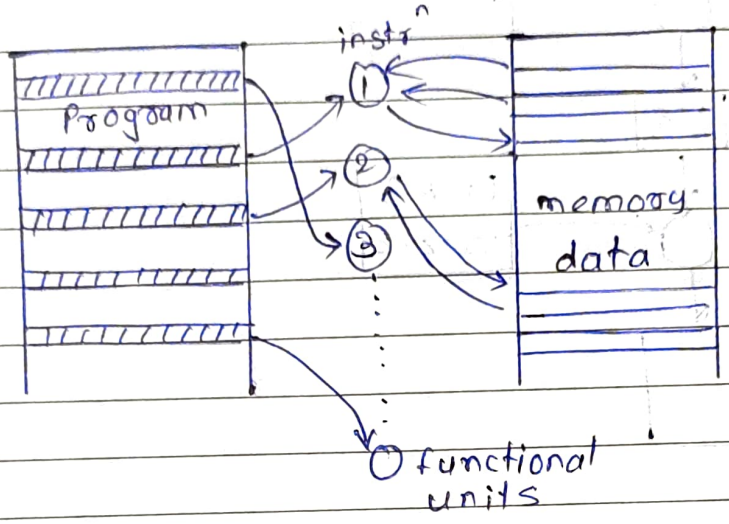
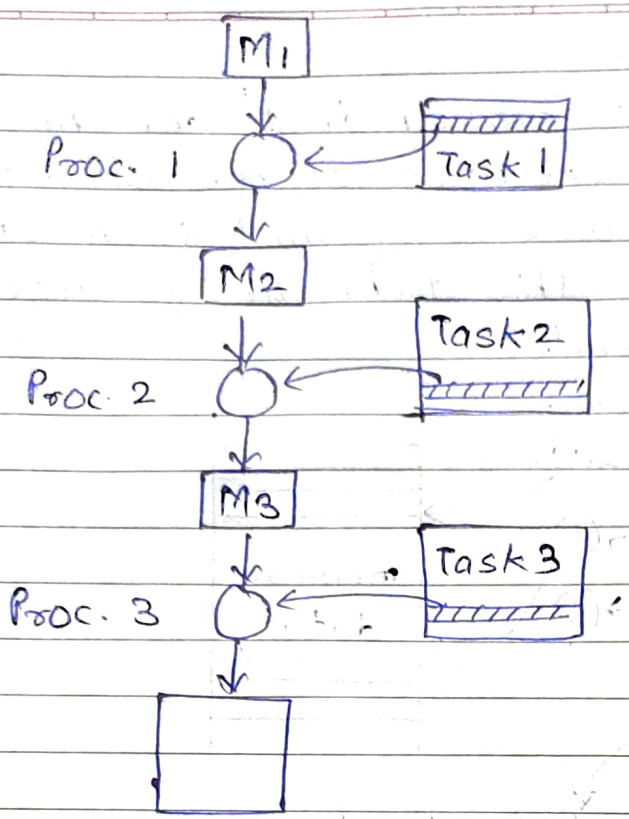
2] Instr^n pipelining -
The execution of stream of inst^n can be pipelined by overlapping the execution of the current instr^n with the fetch, decode & operand fetch of subsequent instr^n. This technique is also known as instr^n lookahead.



3] Processor pipelining -
The data stream passes the first processor with results stored in memory block which is also accessible by second processor. The second processor then passes the refined results to third and so on.



Ramamoorthy & Li have proposed following three pipeline classification schemes:

1] Unifunction vs. multifunction pipelines -
A pipeline unit with a fixed & dedicated function, such as floating point adder is called unifunctional pipeline. A multifunction pipe may perform different functions, either at different times or at same time, by interconnecting different subsets of stages in pipeline.

2] Static vs dynamic pipelines -
A static pipeline may assume only one functional configuration at a time. Static pipelines can be either unifunctional or multifunctional. A dynamic pipeline processor permits several functional configurations to exist simultaneously. A dynamic pipeline must be multifunctional.

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3] Scalar vs vector pipelines -

A scalar pipeline processes a sequence of scalar operands under control of DO loop. Instructions in a small DO loop are prefetched into instr^ buffer. Vector pipelines are specially designed to handle vector instr^ vector operands. Computers having vector instr^ are called vector processors.