Content Product
Detailed syllabus
DIGITAL ELECTRONICS

UNIT I - MINIMIZATION TECHNIQUES AND LOGIC GATES

Introduction to digital electronics - History of digital system, Basics of digital electronics, Digital revolution. **Introduction to number system** - What is number system, Types of number systems. **Different types of number system** - Binary number system, Decimal number system, Octal number system, Hexadecimal number system. **Number base conversion** - Binary to decimal conversion, Conversion of octal number systems, Conversion of hexadecimal number systems. **Arithmetic operations** - Binary arithmetic, Negative numbers in 1's complement form, Negative numbers in 2's complement form, Binary multiplication, Binary division, Hexadecimal arithmetic. **Binary codes** - Binary codes, BCD (Binary Coded Decimal) code, Excess-3 code, Gray code, Gray to binary and binary to gray code conversion, Five-bit BCD codes. **Boolean Algebra and theorems**- Introduction, Boolean postulates and law, Duality theorem. **DeMorgan's theorem** - DeMorgan's theorem, DeMorgan's theorem and other postulates to simplify Boolean expressions. **Boolean Expression** - Boolean Expression, Sum of Product Form, Product of Sum Form, Standard SOP and POS Forms, Converting expressions in Standard SOP or POS Forms, M-Notations : Minterms and Maxterms, Complements of Canonical formulae. **Minimization of Boolean expression** - Minimization of Boolean expression. **Karnaugh (K) map** - Introduction of Karnaugh (K) map, Variable of K - map, Plotting a Karnaugh map, Grouping cells for simplification. **Simplification of SOP And POS Expressions** - Simplification of SOP Expressions, Incompletely specified Functions (Don't Care Terms), Describing incomplete boolean function, Don't Care conditions in logic design, Minimization of incompletely specified Function, Simplification of POS Expressions, Five variable K-map. **Quine - Mccluskey method** - Limitations of Karnaugh map, Quine-Mccluskey minimization technique, Example of Quine-Mccluskey method, Quine-Mccluskey using don't care terms, Prime implicant table and Redundant prime implicants. **Logic gates** - Introduction to logic gates, Types of logic gates, OR gate, AND gate, NOT gate (inverter), Derived or complex gates, Boolean function for logic gates, Alternative logic-gates Representation. **Universal gates** - Introduction of universal gates, NAND gate, NOR gate, Conversion of AND/OR/NOT Logic to NAND/NOR Logic using Graphical Procedure, Properties of EX-OR gates. **Implementation of logic function using logic gates** - Implementing the expression with logic gates, Implementation of SOP boolean expression, Implementation of POS boolean expression, NAND – NAND implementation, NOR – NOR implementation, Multilevel gate implementations, Multilevel NAND and NOR implementation. **Multilevel gates** - Multilevel gate implementations, Multilevel NAND and NOR implementation, Multiple output implementation. **TTL logic** - Transistor Transistor Logic (TTL), 3-input TTL NAND Gate, Input and Output Currents Fan-out, Standard TTL Characteristics, High-Speed (H) and Low-Power (L) TTL, Schottky TTL, Comparison of TTL Series Characteristics, Open Collector Output, Wired-AND Connection, Tri-state Gates, TTL NOR Gate, Comparison of TTL Series Characteristics. **CMOS logic** - Introduction to MOS transistor, MOS Logic Families, Basic CMOS inverter circuit, CMOS NAND Gate, CMOS NOR Gate, FAN in and FAN out, CMOS Characteristics.

UNIT II - COMBINATIONAL LOGIC

Introduction to Combinational circuit - Combinational circuit, Introduction of Design Procedure. **Adders** - Half adder, Half adder using NAND gates, Half - adder using NOR gates, Introduction of full adder. **Subtractor** - Half subtractor, Introduction of Full subtractor. **Parallel binary adder** - Introduction of parallel adder, 4-bit parallel adder. **Parallel binary subtractor** - Introduction of Parallel Subtractor, Comparison between Serial and Parallel Adder. **Carry Look Ahead adder** - Introduction of Carry Look Ahead Adder. **Serial adder/subtractor** - Introduction of serial adder, Operation of serial adder, Serial subtractor. **BCD Adder** - BCD Adder, Introduction of BCD Adder. **Binary multiplier** - Introduction of Binary multiplier. **Binary divider** - Binary divider, Restoring Division, Non Restoring Division, Comparison of Restoring and Non Restoring Division. **Multiplexers** - What is a multiplexer (MUX), 74XX151 8 to 1 multiplexer, 74XX157 Quad 2-Input Multiplexer, 74XX153 Dual 4 to 1

multiplexer, Expanding Multiplexers, Application of Multiplexer. **Demultiplexers** - Introduction of demultiplexer, Introduction of 1 to 16 demultiplexer, IC 74X154 1 to 16 demultiplexer. **Encoders** - Introduction to encoders, Decimal to BCD encoder, IC 74XX147 decimal to BCD encode, Introduction of Octal to Binary Encoder, Introduction of Priority Encoder, **Parity Generators and Checke**r - Parity Generators and Checkers, Logic Diagram, IC 74180 Parity Generator/Checker. **Code converters** - Introduction of code converter, Binary to BCD converter, BCD to Binary converter, BCD to Excess-3, Excess-3 to BCD code converter, Binary to Gray code converter, Gray Code to Binary code converter, Introduction of BCD to Gray code converter, Introduction of Gray to BCD code converter. **Magnitude comparato**r - Digital comparator, One – bit comparator, Two – bit comparator, 4 – Bit Comparator, IC 7485 (4-bit Comparator), IC 74X682 (8-bit comparator).

UNIT III - SSEQUENTIAL CIRCUITS

Sequential logic circuits - Introduction to sequential logic circuits, Level triggering. **Latches** - Gated SR latch, Gated D latch, Latches vs flip-flops. **Flip-flops** - Introduction to flip-flop, Preset and clear inputs, Clocked D flip-flop, JK flip-flop, JK flip-flop using NAND gates, Race-around condition. **Master slave flip-flops** - Master-slave JK flip-flop, Master-slave SR flip-flop, Clocked D flip-flop, Clocked T flip-flop, Flip-flop characteristics, Characteristic equations of flip-flops, Flip-flops as finite state machines, Flip-flop excitation table. **Realization of one flip-flop using other flip-flop**s - SR flip-flop to D flip-flop, SR flip-flop to JK flip-flop, SR flip-flop to T flip-flop, JK flip-flop to T flip-flop, JK flip-flop to D flip-flop, D flip-flop to T flip-flop, T flip-flop to D flip-flop, JK flip-flop to SR flip-flop, D flip-flop to SR flip-flop - Applications of flip-flops. **Asynchronous Counters** - Introduction of counters, Asynchronous counters, Asynchronous/ripple down counter, Asynchronous up/down counter. **Synchronous counter** - Synchronous counters, Synchronous vs asynchronous counters, **Programmable Counter** - Programmable Counter. **Design of synchronous counter** - Design of synchronous counter, Design of a synchronous 3-bit up-down counter using JK flip-flops, Design of a synchronous modulo-6 gray code counter, Design of a synchronous modulo-10 gray code counter, Design of a synchronous BCD counter using JK flip-flops. **Mod-N counter** - Modulo-n counter, Mod-3 counter. **Shift registers** - Introduction of shift registers, Shift registers, Serial-in serial-out shift register, Serial-in parallel-out shift register, Bidirectional shift register, Parallel-in serial-out shift register, Parallel-in parallel out-shift register, 4-bit parallel access shift register (7495), Parallel access shift register (74195), Register with reset facility. **Universal shift register** - Universal shift register, Universal shift register (IC 74194). **Shift register counters** - Shift register counters, Ring counter, Applications of ring counter, Johnson Counter. **Sequence generator** - Sequence generator using counters, Sequence generator using shift register, Design of sequence generator using shift register.

UNIT IV - MEMORY DEVICES

Introduction to memories - Introduction to memories. **Classification of memories** - Classification of memories. **Read Only Memory (ROM)** - Introduction of Read Only Memory, Types of ROM, PROM (Programmable Read Only Memory), EPROM (Erasable Programmable Read Only Memory, EEPROM (Electrically Erasable Programmable Read Only Memory), Comparison of EPROM and EEPROM, Difference between UVPROM and EEPROM, Comparison between RAM and ROM, Types of ROM and RAM ICs, Flash Memory, CD-ROM. **Random Access Memory (RAM)** - Introduction of Random Access Memory, Static RAM, Dynamic RAM, Comparison between SRAM and DRAM. **Memory Decoding** - Introduction of Memory Decoding. **Memory Expansion** - Memory Expansion, Expanding Memory Capacity. **Programmable logic devices (PLD's)** - Introduction of Programmable Logic Devices (PLDs), Programmable Read Only Memory (PROM), PLA(Programmable Logic Array), Programmable Array Logic Devices. **Sequential programmable devices** - Sequential programmable devices, Sequential programmable logic devices (SPLD's), Complex programmable logic devices (CPLD's), Field Programmable Gate Array (FPGA). **Implementation of combinational logic circuits** - Implementation of

combinational logic circuit using PROM, Implementation of combinational logic circuit using PLA, Implementation of combinational logic circuit using PAL.

UNIT V - SYNCHRONOUS AND ASYNCHRONOUS SEQUENTIAL CIRCUIT

General model of synchronous sequential circuits - General model of synchronous sequential circuits. **Classification of synchronous sequential circuit** - Mealy and Moore machine representations, State machine notations. **Design procedure of Synchronous sequential circuit**- Design procedure of Synchronous sequential circuit. **Algorithmic State Machine (ASM)** - Introduction of Algorithmic State Machine (ASM), SM symbols / notations, Salient features of ASM chart, Control subsystem implementation, K-map simplification method, Multiplexer control method, ASM for binary multiplier, ASM for weighing machine, Datapath subsystem for weighing machine. **Analysis of Synchronous sequential circuit** - Analysis of Synchronous sequential circuit, Example. **Design of asynchronous sequential circuits** - Design of asynchronous sequential circuits. **Incompletely specified State machines** - Introduction of Incompletely Specified State Machines. **Problems in asynchronous circuits** – Races, Free state assignment, Shared row state assignment, One hot state assignment. **Logic Hazards** - Hazards, Design of hazard free switching circuit. **Design of combinational circuit using VERILOG** - HDL for combinational circuits, Structure of the data flow description, Signal declaration and assignment statement, Execution of assignment statement, Data type – vectors, 4-bit Ripple-Carry and Carry-Look ahead Adder, Structure of the HDL behavioral descriptions, Sequential statements, Loop statement, While – loop statement, Repeat statement, Forever statement, Gate Level / Structural description. **Design of sequential circuit using VERILOG** - Description of D-latch, Description of Flip-flops, Description of sequential circuits, Description of Moore circuit, HDL for registers and counters, Descriptions of registers in Verilog HDL, Structural model of a universal shift register, Description of counters.