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Question Paper Code: 1214453

B.E. / B.Tech. DEGREE EXAMINATIONS, NOV / DEC 2024
Fourth Semester
Biomedical Engineering
U20BM402 – DIGITAL AND INTEGRATED CIRCUITS
(Regulation 2020)

Time: Three Hours | Maximum: 100 Marks

Answer ALL questions

PART – A (10 x 2 = 20 Marks)

1. Outline the difference between binary code and BCD?
2. Recall the limitations of K-map?
3. Compare Decoder and Demultiplexer
4. Define modulus of a counter? Write down the number of flip flops required for mod-5 counter?
5. What are the limitations of basic differentiator circuit?
6. Illustrate the advantages of Clipper and Clamper.
7. Define lock in range in PLL.
8. How do switching regulators have better efficiency than series regulators?
9. Interpret the significance of the center frequency in a band pass filter's performance.
10. Summarize the merits and demerits of Binary weighted resistor DAC.

PART – B (5 x 16 = 80 Marks)

11. (a) (i) Using K – map, simplify the Boolean function and obtain the minimal SOP expression for the function. (10)
$Y= \sum_m (1,5,7,13,14,15,17,18,21,22,25,29) + \sum_d 6,9,19,23,30)$
(ii) Simplify the given expression. (6)
$Y= \bar{A}B + ABD + A\bar{B}C\bar{D} + BC$

(OR)

(b) Find the minimal sum of products for the Boolean expression , f = ∑(1,2,3,7,8,9,10,11,14,15), using Quine – McCluskey method. (16)

12. (a) Make use of the logic diagram of 4 bit parallel adder / Subtractor and construct a 4 bit parallel adder / Subtractor using IC 7483. (16)

(OR)

(b) (i) Apply the knowledge of 1:8 Demultiplexer to design a circuit that controls multiple devices using a single control signal. (8)
(ii) Apply the concepts of 4 bit SISO shift register and develop truth table and timing diagram. (8)

13. (a) Explain input bias current in inverting amplifier and how it can be compensated. Derive the expression for compensation resistance. (16)

(OR)

(b) Design a fourth order Butterworth filter low pass having upper cutoff frequency F= 1KHZ. (16)

14. (a) (i) Design an astable multivibrator circuit which will flash the electric bulb such that it's ON time will be 4 seconds and OFF time will be 2 seconds. (8)
(ii) Identify how PLL circuit functions as a frequency multiplier and illustrate its operation with relevant waveforms. (8)

(OR)

(b) (i) Design series voltage regulators and analyze the performance parameters of voltage regulators. (8)
(ii) Utilize the principle of voltage regulators and explain the working of low and High voltage 723 regulator with neat sketch. (8)

15. (a) (i) Design an active first order low pass filter and obtain its frequency response. (12)
(ii) A 12 bit DAC has a step size of 8mv.Determine the full scale output voltage and percentage resolution. Also find the output voltage for the input (011101110001). (4)

(OR)

(b) (i) Elaborate the functional diagram and circuit operation of Dual Slope ADC. (12)
(ii) A 10 bit ADC with V_{FSR} = 10.24 V is found to have actual signal to noise plus distortion ratio as 56 dB. Determine the effective number of bits and $SNR_{max.}$ (4)

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