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Question Paper Code: 1066182

B.E. / B.Tech. DEGREE EXAMINATIONS, NOV / DEC 2024
Sixth Semester
Electronics and Communication Engineering
U20EC602 – VLSI CIRCUITS AND CAD DESIGN
(Regulation 2020)

Time: Three Hours Maximum: 100 Marks

Answer ALL questions

PART – A (10 x 2 = 20 Marks)

1. Define threshold voltage.

2. Compare between enhancement and depletion mode transistor.

3. Mention the sources of power dissipation in CMOS circuits.

4. What is the effect of transistor sizing? Why is it needed?

5. What are the different types of shift registers?

6. What is Ripple Carry Adder?

7. What is the job of symbolic layout editor?

8. An algorithm with polynomial time complexity is preferred over an exponential algorithm. Is the above statement is true. Justify your answer.

9. How do you select the floor plan order?

10. List the parameters characterizing the local routing problem.

PART – B (5 x 16 = 80 Marks)

11. (a) Derive the drain current I_D of NMOS transistor in different regions of operation. Illustrate graphically the derived I-V characteristics. (16)

(OR)

(b) Analyze in detail about the second order effects of MOS transistor. (16)

12. (a) Examine the static and dynamic power dissipation of the CMOS inverter with relevant expressions and waveforms. (16)

(OR)

(b) Explain Transmission gates with neat sketches. (16)

13. (a) Write a HDL code for 4 to 1 multiplexer and 3 to 8 decoder. (16)

(OR)

(b) Design a carry look ahead adder circuit using HDL. (16)

14. (a) List the various semicustom design methodologies. Discuss their layout and compare their performance. (16)

(OR)

(b) Write an algorithm for constraint-graph compaction and explain it. (16)

15. (a) Why do we say that the channel routing problem as NP-Complete? With an example, explain channel routing algorithm. (16)

(OR)

(b) (i) Describe the Terminology and representation of floor plan with suitable diagrams. (8)

(ii) List the optimizing problems in the floor planning. (8)

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