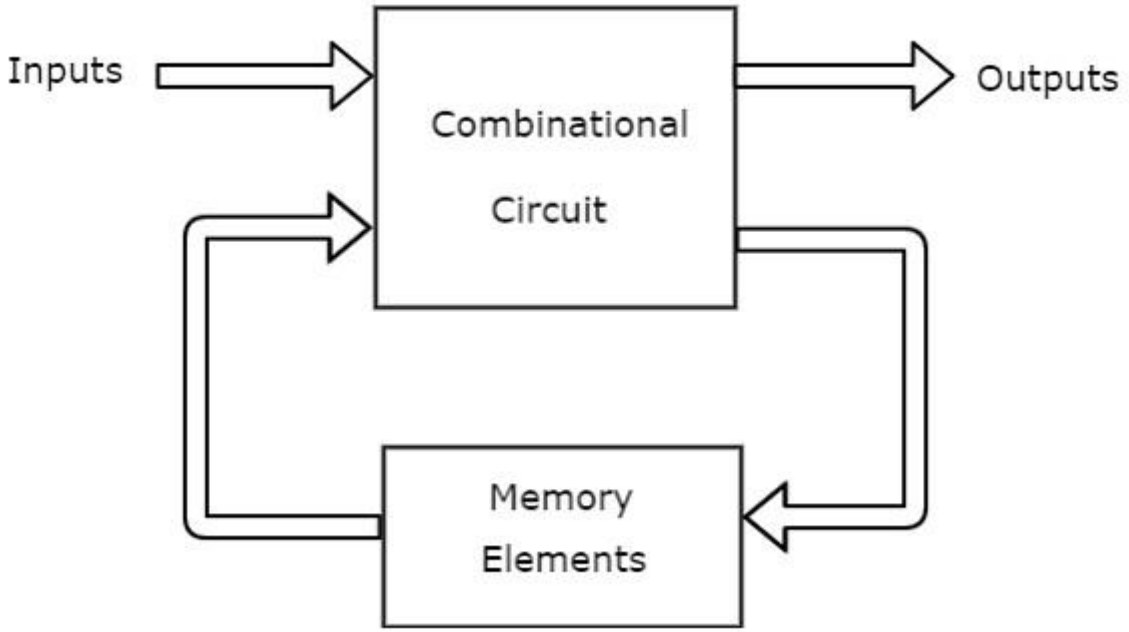
Unit 3:Sequential Circuits

- Sequential circuit is the combination of Combinational circuit and memory.
- In sequential circuit present output is depending on present input and past output so It acts as a Feedback Mechanism.



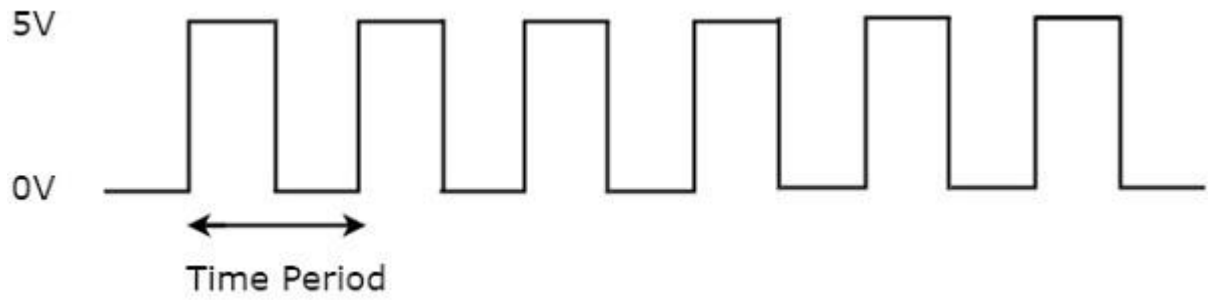
- This sequential circuit contains a set of inputs and outputs.
  The outputs of sequential circuit depends not only on the combination of present inputs but also on the previous outputs.
  Previous output is nothing but the **present state**.
  Therefore, sequential circuits contain combinational circuits along with memory storage elements.
  Some sequential circuits may not contain combinational circuits, but only memory elements.

Types of Sequential Circuits

- Asynchronous sequential circuits
- Synchronous sequential circuits

What is Clock?

- In Sequential circuits, many processes are going on and the output of circuit is the input of other. Thus their should be control over the processes. They can not Operate Randomly.
- clock signal as **a particular type of signal that oscillates between a high and a low state**.
- We can represent the clock signal as a **square wave**, when both its ON time and OFF time are same. This clock signal is shown in the following figure.



- square wave is considered as clock signal.
- This signal stays at logic High 5V for some time and stays at logic Low 0V for equal amount of time.
  This pattern repeats with some time period.
- The reciprocal of the time period of clock signal is known as the frequency of the clock signal.
- All sequential circuits are operated with clock signal.
- So, the frequency at which the sequential circuits can be operated accordingly the clock signal frequency has to be chosen.

- Types of Triggering

Following are the two possible types of triggering that are used in sequential circuits.

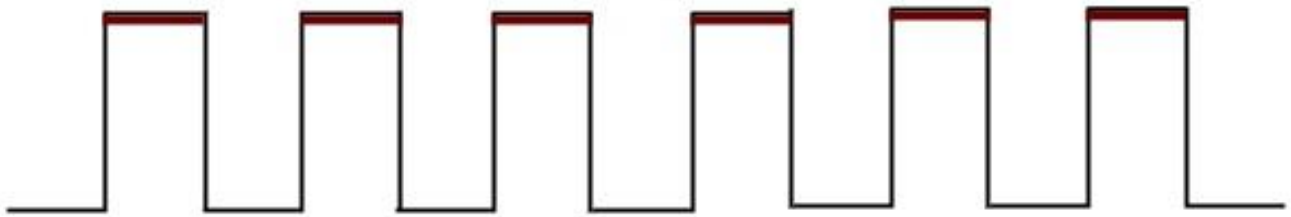
  - Level triggering
  - Edge triggering

Level triggering

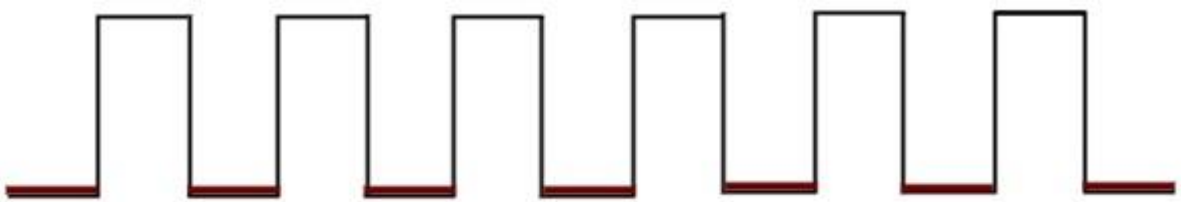
There are two levels, namely logic High and logic Low in clock signal. Following are the two **types of level triggering**.

  - Positive level triggering
  - Negative level triggering

- If the sequential circuit is operated with the clock signal when it is in **Logic High**, then that type of triggering is known as **Positive level triggering**. It is highlighted in below figure.



If the sequential circuit is operated with the clock signal when it is in **Logic Low**, then that type of triggering is known as **Negative level triggering**. It is highlighted in the following figure.



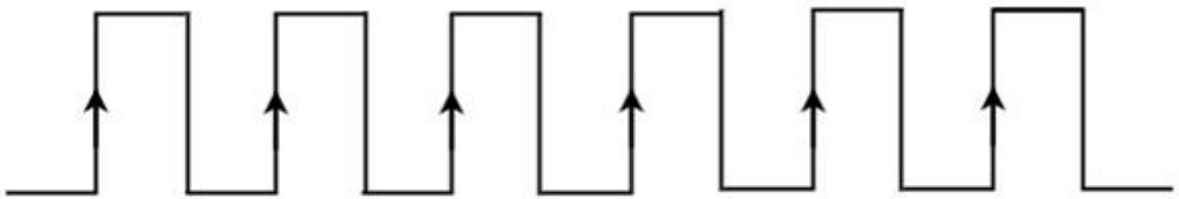
Edge triggering

There are two types of transitions that occur in clock signal. That means, the clock signal transitions either from Logic Low to Logic High or Logic High to Logic Low.

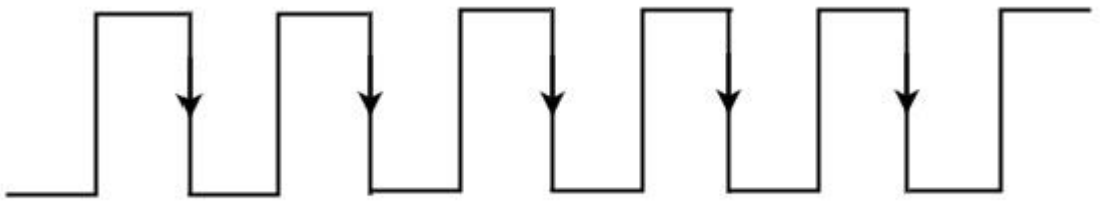
Following are the two **types of edge triggering** based on the transitions of clock signal.

- Positive edge triggering
- Negative edge triggering

- If the sequential circuit is operated with the clock signal that is transitioning from Logic Low to Logic High, then that type of triggering is known as **Positive edge triggering**. It is also called as rising edge triggering. It is shown in the following figure.



If the sequential circuit is operated with the clock signal that is transitioning from Logic High to Logic Low, then that type of triggering is known as **Negative edge triggering**. It is also called as falling edge triggering. It is shown in the following figure.



- There are two types of memory elements based on the type of triggering that is suitable to operate it.
- Latches
- Flip-flops

Basics of Flip-Flop and Latches

- Flip Flop is a binary storage device.
- It can store binary bit either 0 or 1.
- It has two stable states high and low i.e 1 and 0
- It is also called bistable multivibrator.

Flip Flop

- A flip flop can maintain a binary state for an unlimited period of time as long as-Power is supplied to the circuit.
- Or until it is directed by an input signal to switch states.
- A flip flop is also called as **Bistable Multivibrator** because it has two stable states either 0 or 1.

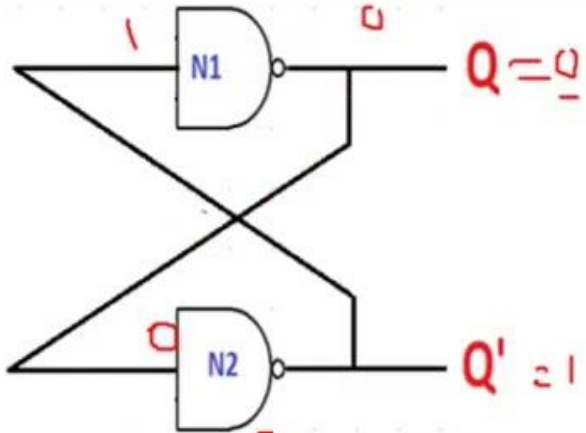
Flip Flop

Flip-Flop v/s Latch

- The primary difference between a latch and a flip-flop is a gating or clocking mechanism.
- In Simple words. Flip Flops are edge-triggered and a latch is level-triggered.
- Latches operate with enable signal, which is **level sensitive**. Whereas, flip-flops are edge sensitive.

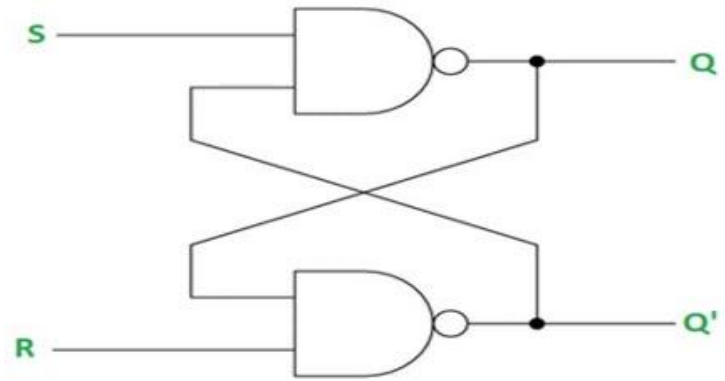
One bit memory cell

- One bit memory cell is designed using two cross coupled invertors N1 and N2. (NAND gates are used as invertors).
- It is known as bistable element as it contain only two states logic 1 state (HIGH) and logic 0 state (LOW).



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NAND gate S-R Latch (Active Low)



- Case 1 – S=0, R=0, Q=1 & Q'=1
  Invalid
- Case 2 – S=1, R=0, Q=0 & Q'=1
  S=1, R=1, Q=0 & Q'=1
- Case 3 – S=0, R=1, Q=1 & Q'=0
  S=1, R=1, Q=1 & Q'=0

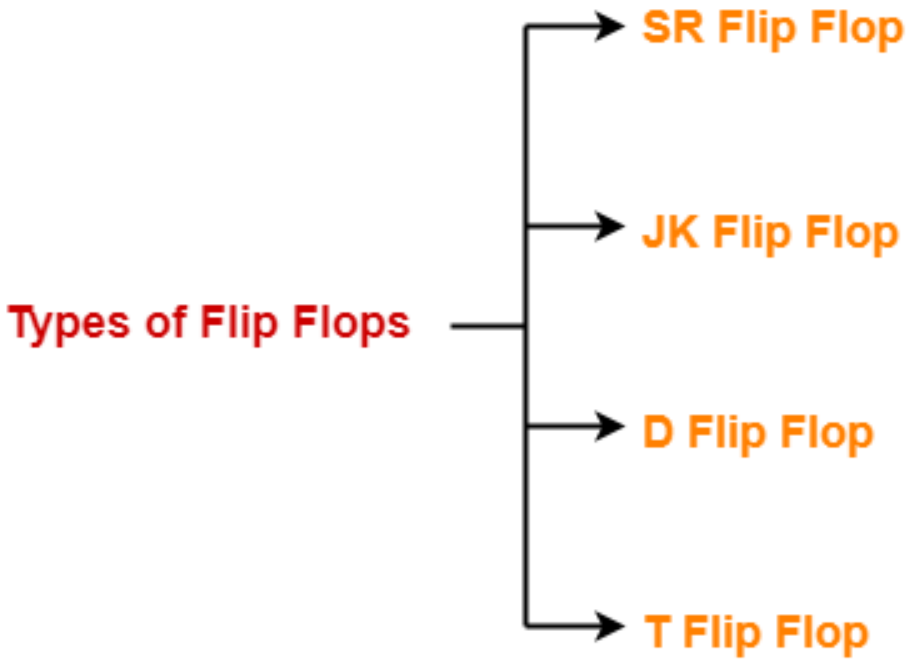
NAND Truth table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

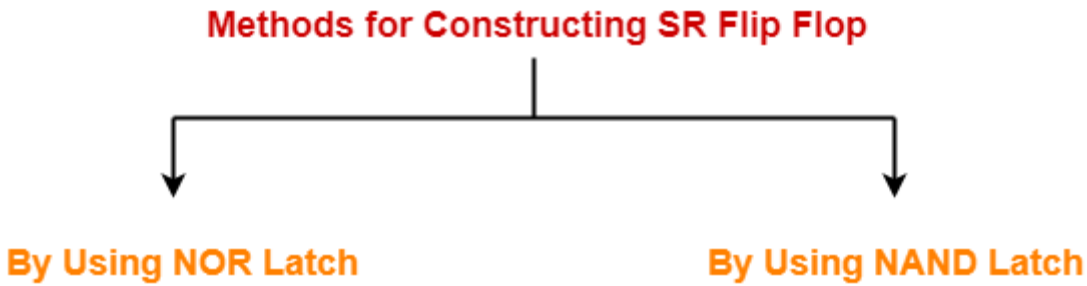
SR Latch Truth table

S	R	Q	Q'
0	0	Invalid	
0	1	1	0
1	0	0	1
1	1	No change	

- **<u>Flip Flops Types-</u>**
- Flip flops are of different types depending on how their inputs and clock pulses cause transition between two states.
- There are 4 basic types of flip flops-



- **SR Flip Flop-**
- SR flip flop is the simplest type of flip flops.
- It stands for **Set Reset flip flop.**
- It is a clocked flip flop.
- **Construction of SR Flip Flop-**
- There are following two methods for constructing a SR flip flop-



SR Flip Flop:

- The SR flip flop is a 1-bit memory bistable device having two inputs, i.e., SET and RESET. The SET input 'S' set the device or produce the output 1, and the RESET input 'R' reset the device or produce the output 0. The SET and RESET inputs are labeled as **S** and **R**, respectively.
- The SR flip flop stands for "Set-Reset" flip flop. The reset input is used to get back the flip flop to its original state from the current state with an output 'Q'. This output depends on the set and reset conditions, which is either at the logic level "0"
- The NAND gate SR flip flop is a basic flip flop which provides feedback from both of its outputs back to its opposing input. This circuit is used to store the single data bit in the memory circuit. So, the SR flip flop has a total of three inputs, i.e., 'S' and 'R', and current output 'Q'. This output 'Q' is related to the current history or state. or "1".

The NAND Gate SR Flip-Flop

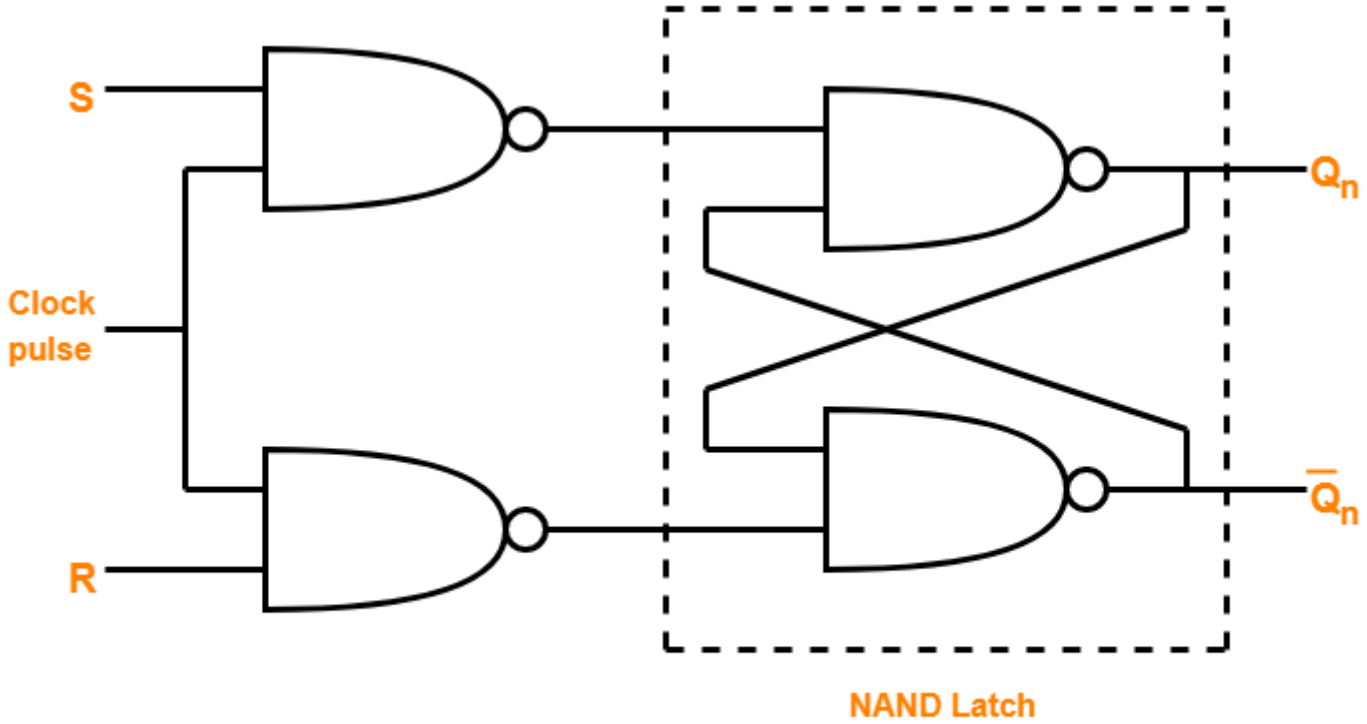
- We can implement the set-reset flip flop by connecting two cross-coupled 2-input NAND gates together.
- In the SR flip flop circuit, from each output to one of the other NAND gate inputs, feedback is connected. So, the device has two inputs, i.e., Set 'S' and Reset 'R' with two outputs Q and Q' respectively. Below are the block diagram and circuit diagram of the S-R flip flop.
- An important point about NAND gate is that its dominating input is 0 i.e., if any of its input is Logic ‘0’, the output is Logic ‘1’, irrespective of the other input. The output is 0, only if all the inputs are 1.

Logic Symbol-

The logic symbol for SR Flip Flop is as shown below-

Logic Symbol

The logic circuit for SR Flip Flop constructed using NAND latch is as shown below-



SR Flip Flop Using NAND Latch

The truth table for SR Flip Flop is as shown below-

INPUTS			OUTPUTS
S	R	Q_n (Present State)	Q_{n+1} (Next State)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	Indeterminate
1	1	1	Indeterminate

The above truth table may be reduced as-

INPUTS			OUTPUTS	REMARKS
S	R	Q_n (Present State)	Q_{n+1} (Next State)	States and Conditions
0	0	X	Q_n	Hold State condition S = R = 0
0	1	X	0	Reset state condition S = 0 , R = 1
1	0	X	1	Set state condition S = 1 , R = 0
1	1	X	Indeterminate	Indeterminate state condition S = R = 1

Truth Table

Latches Vs. Flip-Flop

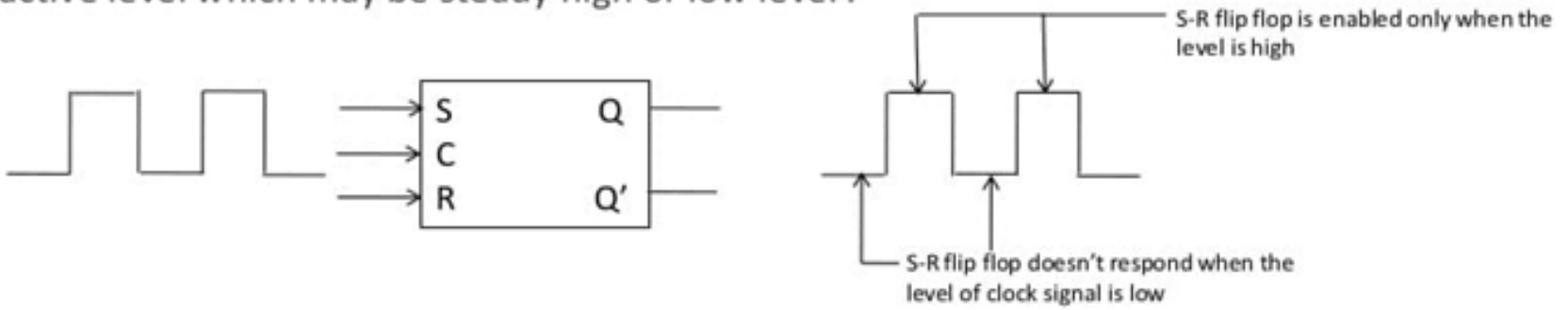
Triggering Methods

Depending on which portion of clock signal the latch or flip flop responds to, classify them into two types:-

1. Level Triggering.

2. Edge Triggering.

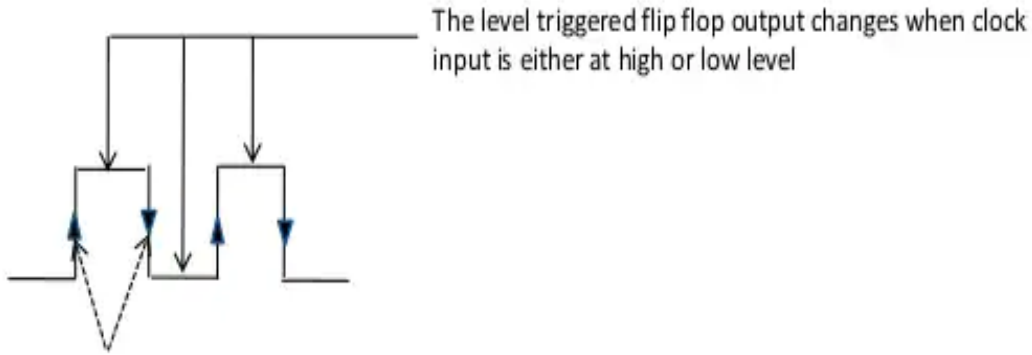
LEVEL TRIGGERING:-Circuit respond to change in their input, if their enable input(E) held at an active level which may be steady high or low level .



Types of Level Triggering Flip Flops

1. Positive Level Triggering :-Output of a flip flop respond to the input changes, only when its clock inputs are high (1) level.

2. Negative Level Triggering :-Output of a flip flop respond to the input changes, only when its clock inputs are low (0) level.



EDGE TRIGGERING

Flip flops which changes their outputs only corresponding to the positive (rising) or negative (falling) edge of the clock input.

Types of edge triggering:-

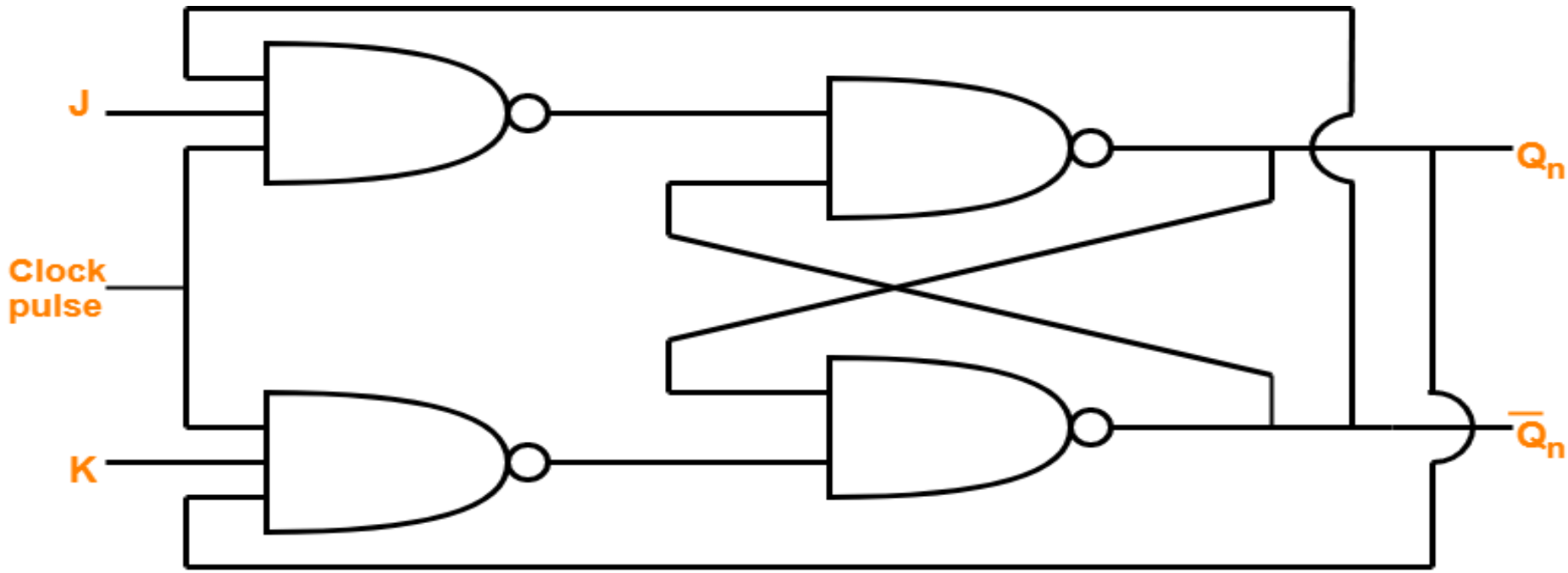
1. Positive edge triggering:-Flip flops which allows its output to change in response to its inputs only at the instants corresponding to the rising edge of clock(positive spikes).Its output will not respond to change in inputs at any other instant of time.
2. Negative edge triggering:-Flip flops which responds only to the falling edge of clock(negative spikes) of the clock.

JK Flip Flop-

- JK flip flop is a refined & improved version of SR Flip Flop that has been introduced to solve the problem of indeterminate state that occurs in SR flip flop when both the inputs are 1.

In JK flip flop,

- Input J behaves like input S of SR flip flop which was meant to set the flip flop.
- Input K behaves like input R of SR flip flop which was meant to reset the flip flop.



Logic Circuit For JK Flip Flop Using SR Flip Flop

(Constructed Using NAND Latch)

Truth table

INPUTS			OUTPUTS
J	**K**	**Q_n (Present State)**	**Q_{n+1} (Next State)**
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Logic Symbol

INPUTS			OUTPUTS	REMARKS
J	K	Q_n (Present State)	Q_{n+1} (Next State)	States and Conditions
0	0	X	Q_n	Hold State condition J = K = 0
0	1	X	0	Reset state condition J = 0 , K = 1
1	0	X	1	Set state condition J = 1 , K = 0
1	1	X	Q'_n	Toggle state condition

Points to Remember:

- Both JK flip flop and SR flip flop are functionally same.

The only difference between them is-

- In JK flip flop, indeterminate state does not occur.
- In JK flip flop, instead of indeterminate state, the present state toggles.
- In other words, the present state gets inverted when both the inputs are 1.

Excitation Table

- The excitation table of any flip flop is drawn using its truth table.

What is excitation table?

For a given combination of present state Q_n and next state Q_{n+1}, excitation table tell the inputs required.

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Excitation Table

JK Flip Flop-

JK flip flop is a refined & improved version of **SR Flip Flop**

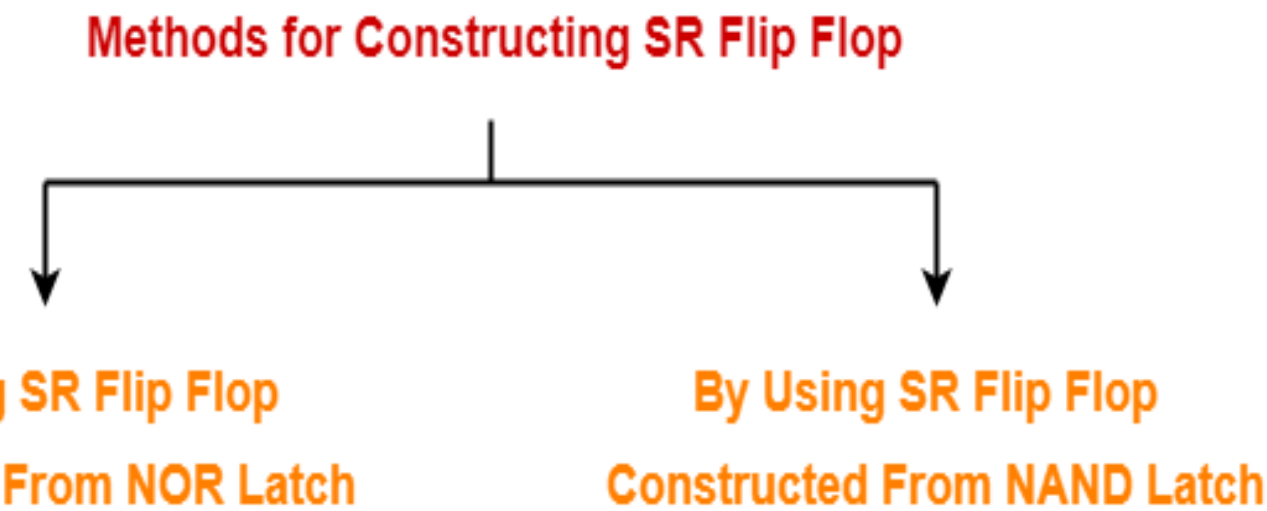
that has been introduced to solve the problem of indeterminate state

that occurs in SR flip flop when both the inputs are 1.

In JK flip flop,

- Input J behaves like input S of SR flip flop which was meant to set the flip flop.
- Input K behaves like input R of SR flip flop which was meant to reset the flip flop.

There are following two methods for constructing a JK flip flop-



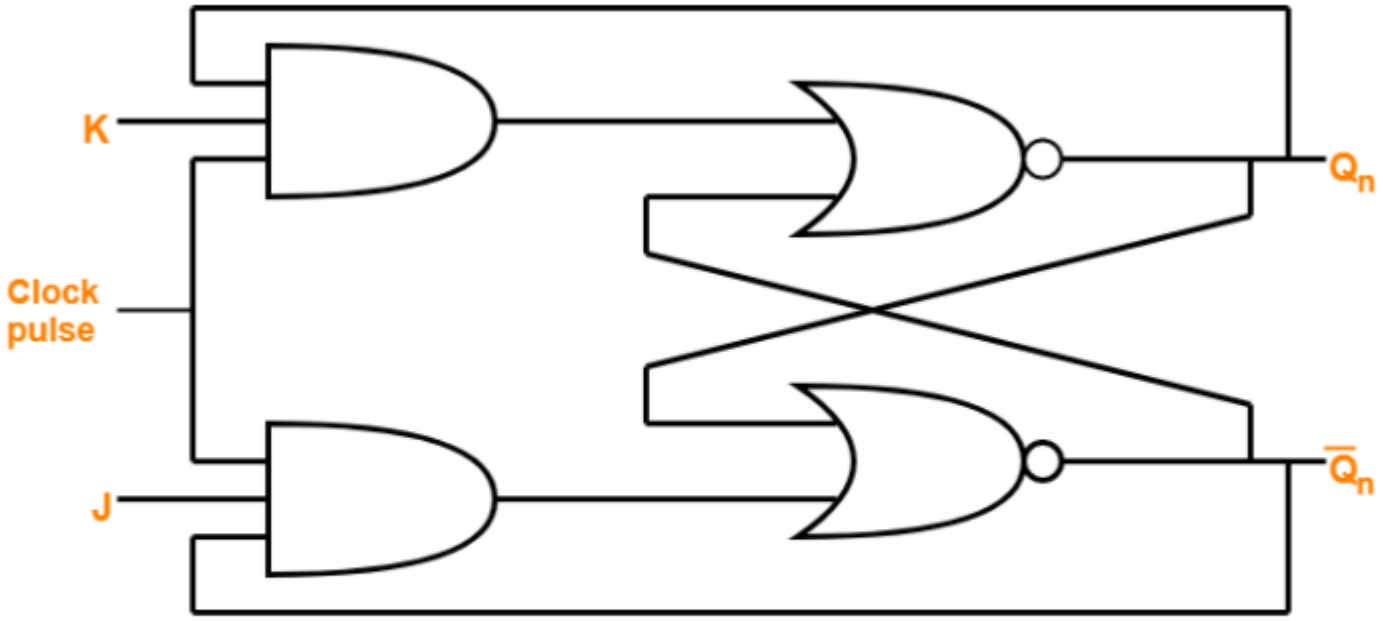
1. By using SR flip flop constructed from NOR latch
2. By using SR flip flop constructed from NAND latch

- **<u>Construction of JK Flip Flop By Using SR Flip Flop Constructed From NOR Latch-</u>**

- This method of constructing JK Flip Flop uses-
- SR Flip Flop constructed from NOR latch
- Two other connections

Logic Circuit-

The logic circuit for JK Flip Flop constructed using SR Flip Flop constructed from NOR latch is as shown below-



Logic Circuit For JK Flip Flop Using SR Flip Flop

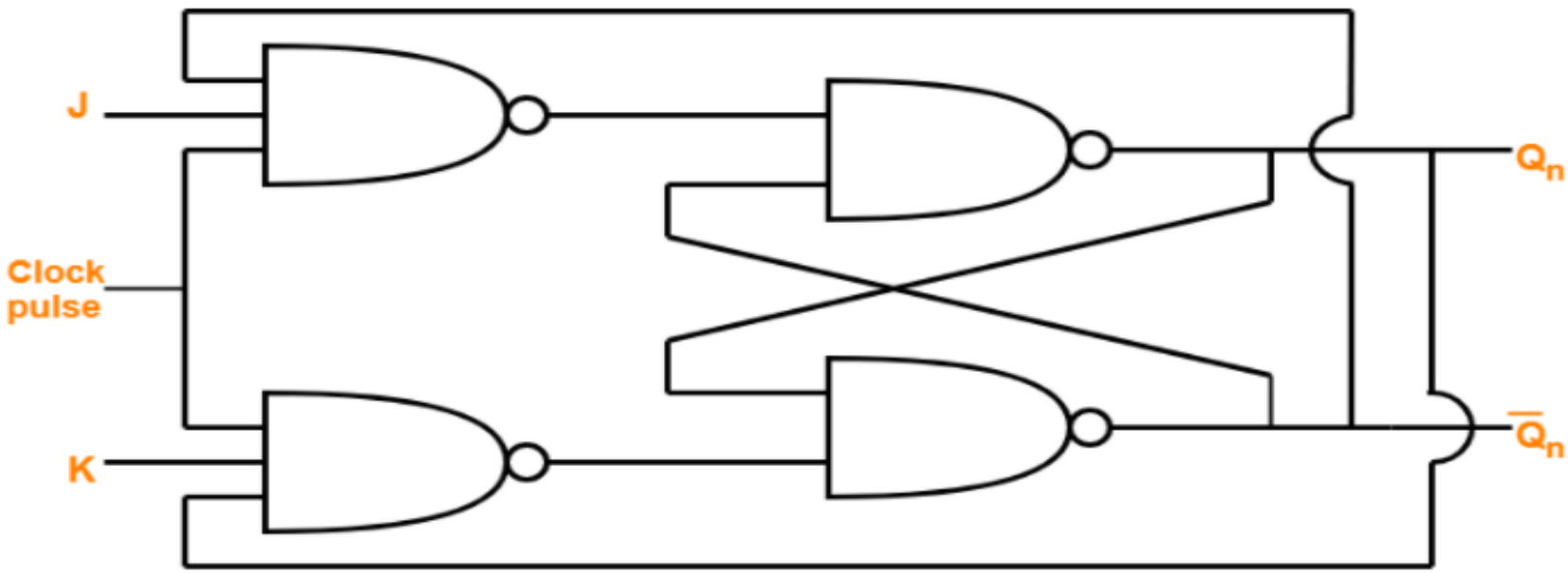
(Constructed From NOR Latch)

- **Construction of JK Flip Flop By Using SR Flip Flop Constructed From NAND Latch-**

- This method of constructing JK Flip Flop uses-
- SR Flip Flop constructed from NAND latch
- Two other connections

Logic Circuit-

The logic circuit for JK Flip Flop constructed using SR Flip Flop constructed from NAND latch is as shown below-



Logic Circuit For JK Flip Flop Using SR Flip Flop

(Constructed Using NAND Latch)

Logic Symbol-

The logic symbol for JK Flip Flop is as shown below-

Logic Symbol

The truth table for JK Flip Flop is as shown below-

INPUTS			OUTPUTS
J	K	Q_n (Present State)	Q_{n+1} (Next State)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Truth Table

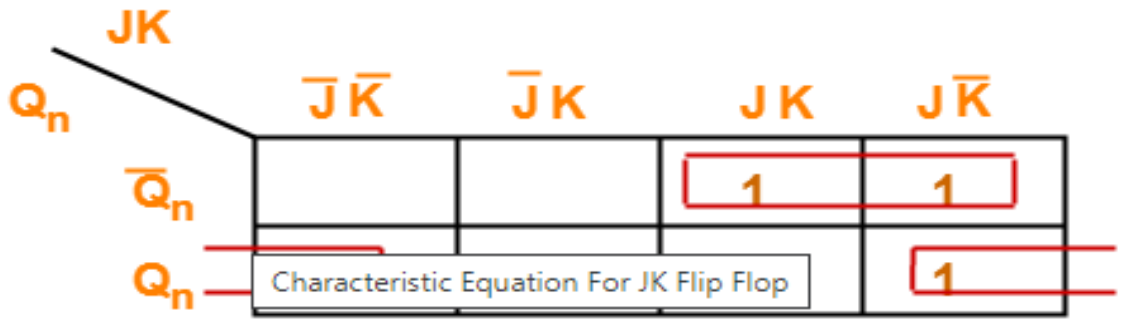
The above truth table may be reduced as-

INPUTS			OUTPUTS	REMARKS
J	K	Q_n (Present State)	Q_{n+1} (Next State)	States and Conditions
0	0	X	Q_n	Hold State condition J = K = 0
0	1	X	0	Reset state condition J = 0 , K = 1
1	0	X	1	Set state condition J = 1 , K = 0
1	1	X	Q'_n	Toggle state condition J = K = 1

Truth Table

Characteristic Equation-

Draw a k map using the above truth table-



K Map

From here-

$$Q_{n+1} = Q'_n (JK + JK') + Q_n (J'K' + JK')$$

$$\boxed{Q_{n+1} = Q'_n J + Q_n K'}$$

Excitation Table-

The excitation table of any flip flop is drawn using its truth table.

What is excitation table?

For a given combination of present state Q_n and next state Q_{n+1}, excitation table tell the inputs required.

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Excitation Table

SR Flip Flop Vs JK Flip Flop

Both JK flip flop and SR flip flop are functionally same.
The only difference between them is-

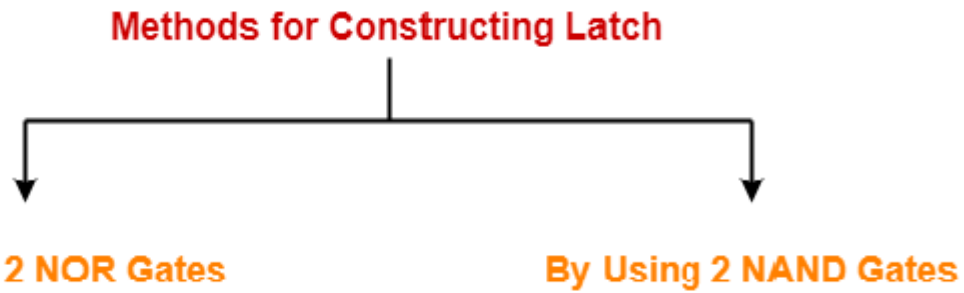
- In JK flip flop, indeterminate state does not occur.
- In JK flip flop, instead of indeterminate state, the present state toggles.
- In other words, the present state gets inverted when both the inputs are 1.

Latch-

- A latch is basically an unclocked flip flop or a latch is the basic building block using which clocked flip flops are constructed.

Latch Construction-

There are following two methods for constructing a latch-



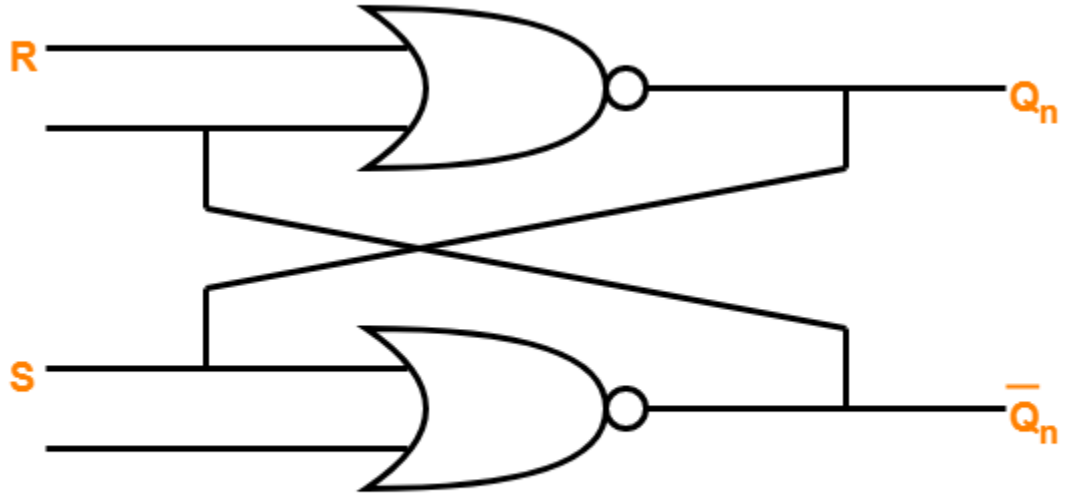
1. By using 2 NOR gates
2. By using 2 NAND gates

Construction Of Latch By Using 2 NOR Gates-

- **Logic Circuit-** The logic circuit for a latch constructed using NOR gates is as shown below-

While constructing a latch using NOR gates, it is compulsory to consider-

- Reset input R in normal output Q_n.
- Set input S in complemented output Q'_n.



Latch Construction Using NOR Gates

Logic Symbol-

- The logic symbol for a latch constructed using NOR gates is as shown below-

Logic Symbol

The truth table for a latch constructed using NOR gates is as shown below-

INPUTS			OUTPUTS
R	S	Q_n (Present State)	Q_{n+1} (Next State)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	Indeterminate
1	1	1	Indeterminate

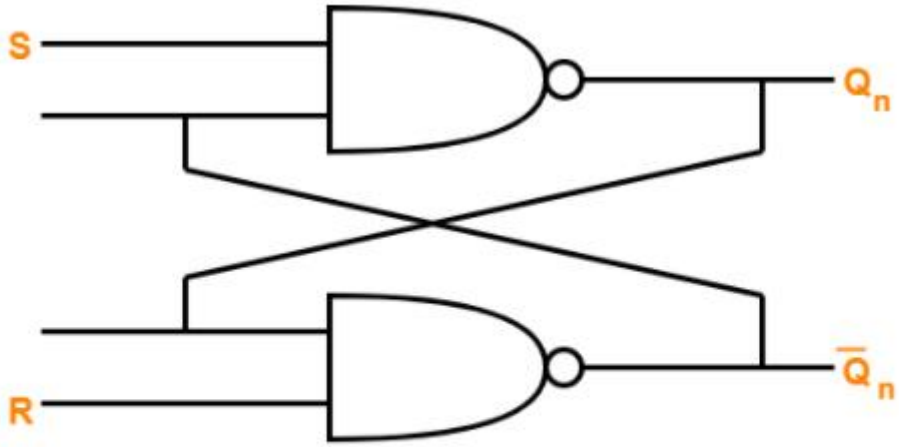
The above truth table may be reduced as-

INPUTS			OUTPUTS	REMARKS
R	S	Q_n (Present State)	Q_{n+1} (Next State)	States and Conditions
0	0	X	Q_n	Hold state condition R = S = 0
0	1	X	1	Set state condition R = 0 , S = 1
1	0	X	0	Reset state condition R = 1 , S = 0
1	1	X	Indeterminate	Indeterminate state condition R = S = 1

Truth Table

Construction Of Latch By Using 2 NAND Gates-

- **Logic Circuit-**
- The logic circuit for a latch constructed using NAND gates is as shown below-



Latch Construction Using NAND Gates

- While constructing a latch using NAND gates, it is compulsory to consider-
- Set input S in normal output Q_n.
- Reset input R in complemented output Q'_n.

Logic Symbol-

The logic symbol for a latch constructed using NAND gates is as shown below-

Logic Symbol

The truth table for a latch constructed using NAND gates is as shown below-

INPUTS			OUTPUTS
S	R	Q_n (Present State)	Q_{n+1} (Next State)
0	0	0	Indeterminate
0	0	1	Indeterminate
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Truth Table

The above truth table may be reduced as-

INPUTS			OUTPUTS	REMARKS
S	R	Q_n (Present State)	Q_{n+1} (Next State)	States and Conditions
0	0	X	Indeterminate	Indeterminate state condition S = R = 0
0	1	X	1	Set state condition S = 0 , R = 1
1	0	X	0	Reset state condition S = 1 , R = 0
1	1	X	Q_n	Hold State condition S = R = 1

Truth Table

D flip flops

- A D (or Delay) Flip Flop is a digital electronic circuit used to delay the change of state of its output signal (Q) until the next rising edge of a clock timing input signal occurs.