Registers

Shift Registers

- A register that is capable of shifting its binary data in one or both directions (left and right) is called a shift register.
- Shift registers are actually a type of sequential logic circuit, mainly for storage of digital data.
- They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop.
- Most of the registers possess no characteristic internal sequence of states.
- All the flip-flops are driven by a common clock, and all are set or reset simultaneously.

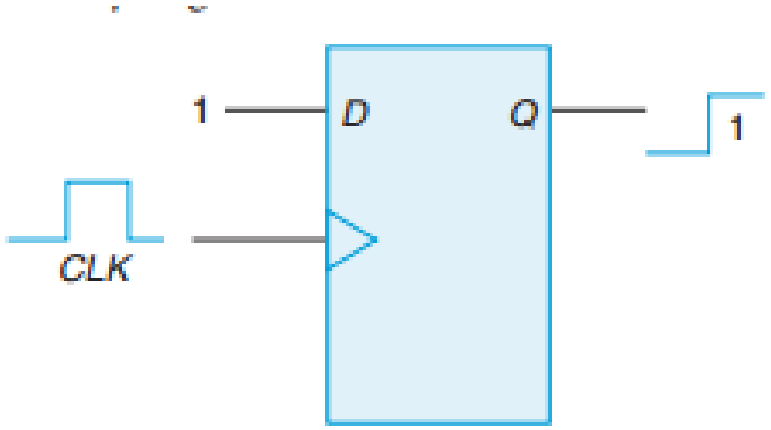
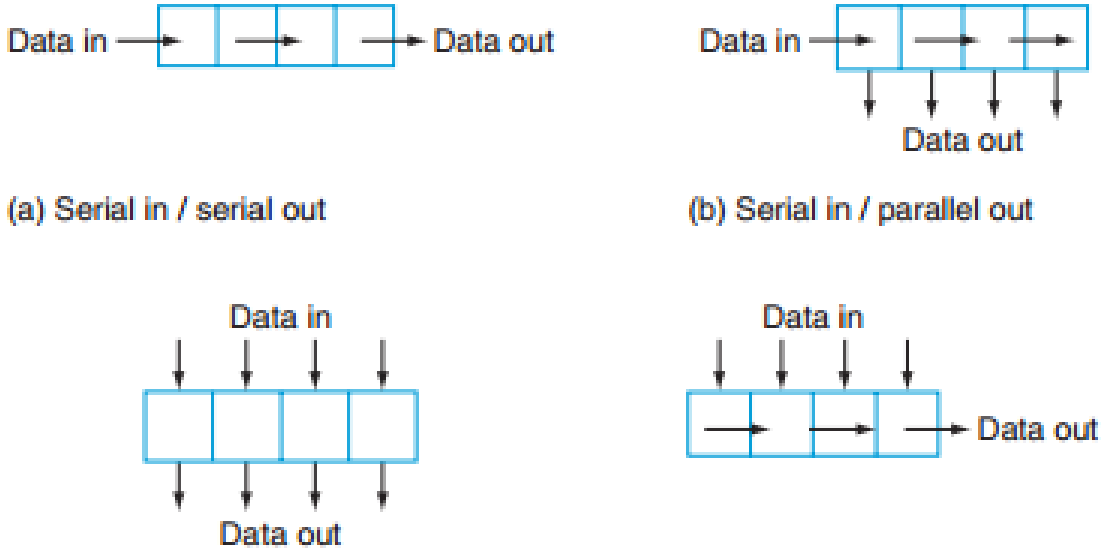


Figure 6.2 D flip-flop as a storage element



(a) Serial in / serial out

(b) Serial in / parallel out

(c) Parallel in /parallel out

(d) Parallel in / serial out

Figure 6.3 Four basic data movements in shift registers

Serial In/Serial Out Shift Register (SISO)

- In a SISO register, data is entered and read in serial fashion. Let's examine the basic 4-bit SISO implemented by D flip-flops as in Figure 6.4. Please note that with 4 flip-flops for 4 stages, this register can store up to four bits of data.

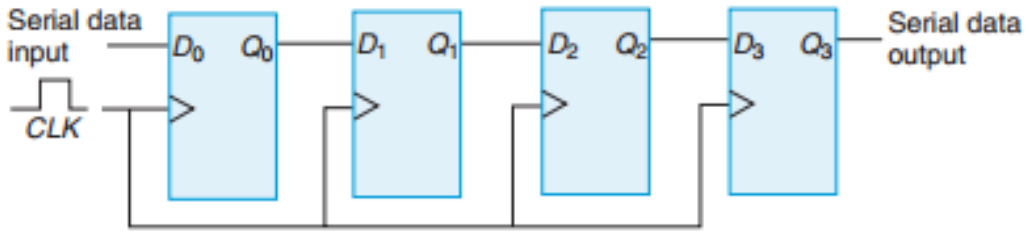
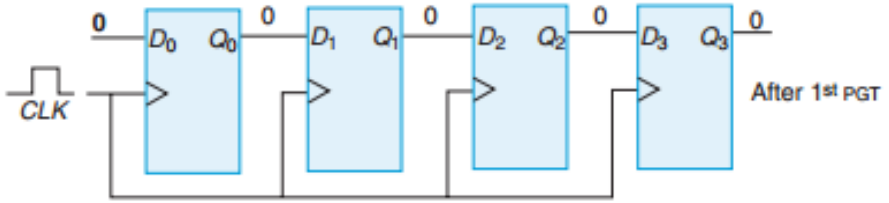


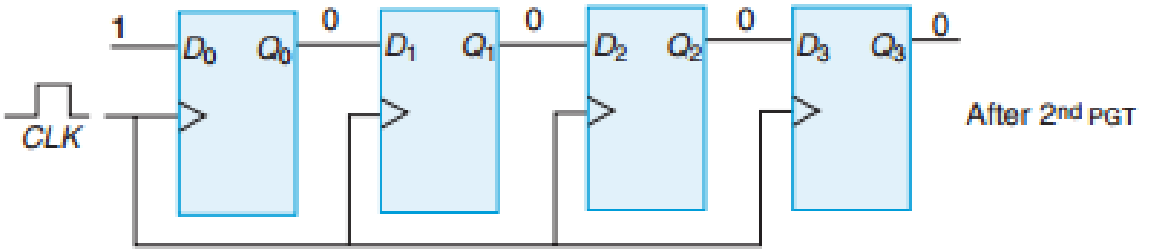
Figure 6.4 4-bit SISO shift register

Initially, the shift register is cleared. For example, the input applied is 0110.

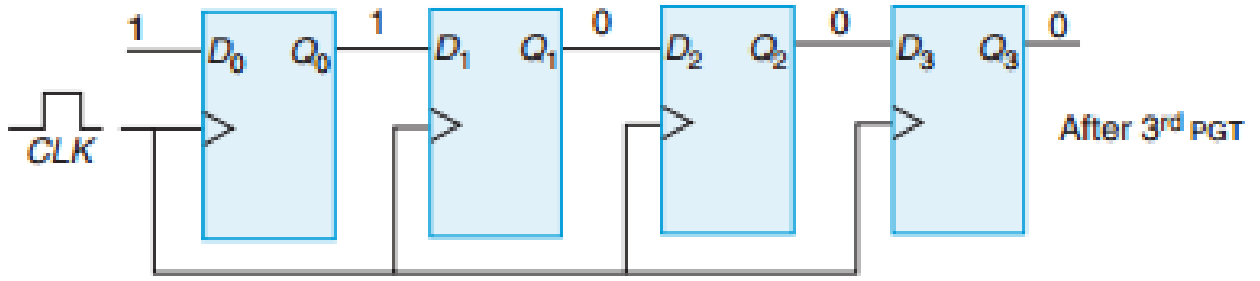
1. At the first positive edge (PGT) of the clock, the input data '0' enters the first flip-flop.



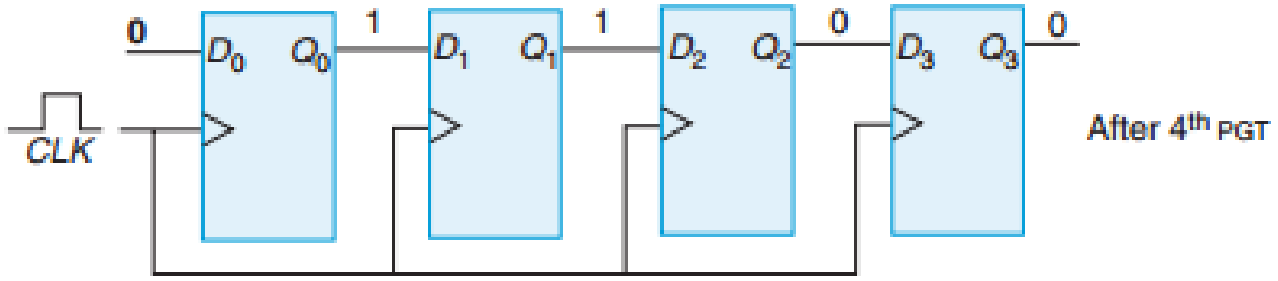
2. At the 2nd PGT, the input '1' is entered.



3. At the 3rd PGT, the next input '1' is entered.



4. At the 4th PGT, the last input '0' is entered.



Serial In/Parallel Out Shift Register (SIPO)

- In a SIPO shift register, the data is entered into a register in serial fashion, similar to SISO.
- The difference is only in the way in which the data is read or taken out from the register, which is parallel.
- Once all the data have been stored serially, each bit appears on its respective output line, and are all available simultaneously.
- The clock is not required to read the data and the data is retained even after the read operation.

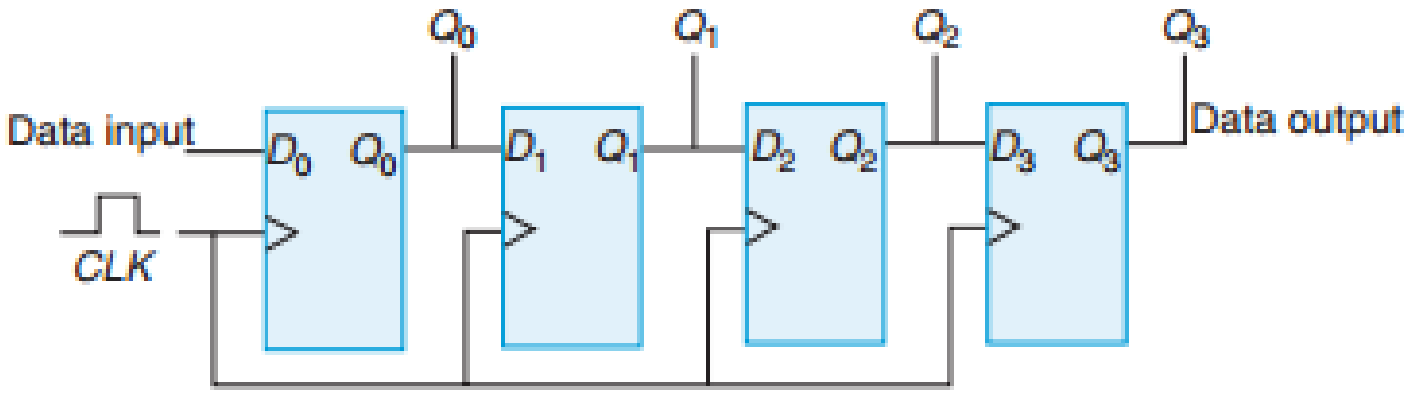


Figure 6.6 A SIPO shift register

Parallel In/Serial Out Shift Register (PISO)

- In a PISO shift register, all the data are entered simultaneously into their respective stages in parallel rather than bit-by-bit.
- After that, the data is shifted out serially from the register.

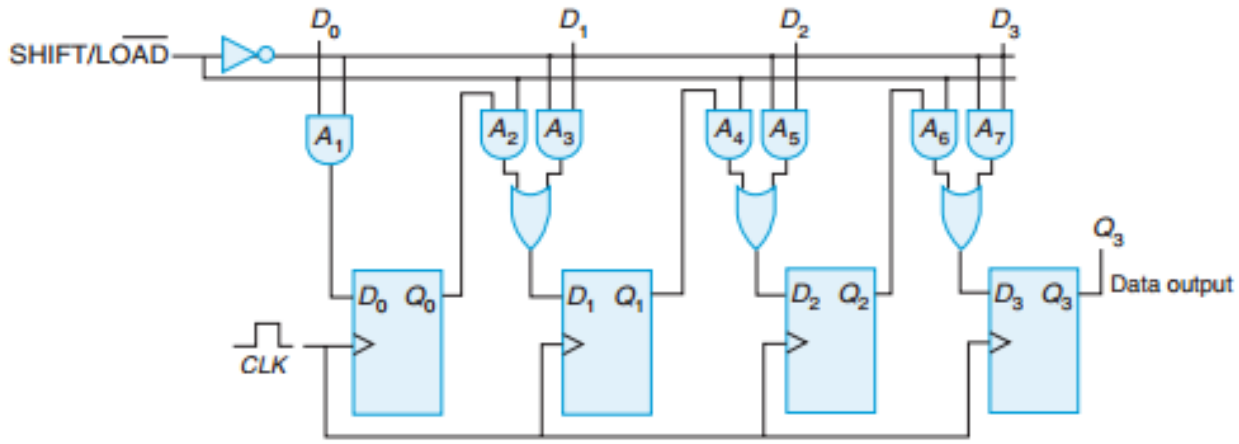


Figure 6.7 PISO shift register

Parallel In/Parallel Out Shift Register (PIPO)

- In a PIPO shift register, the data is entered and read in parallel fashion.
- Both enter and read style has been discussed previously.

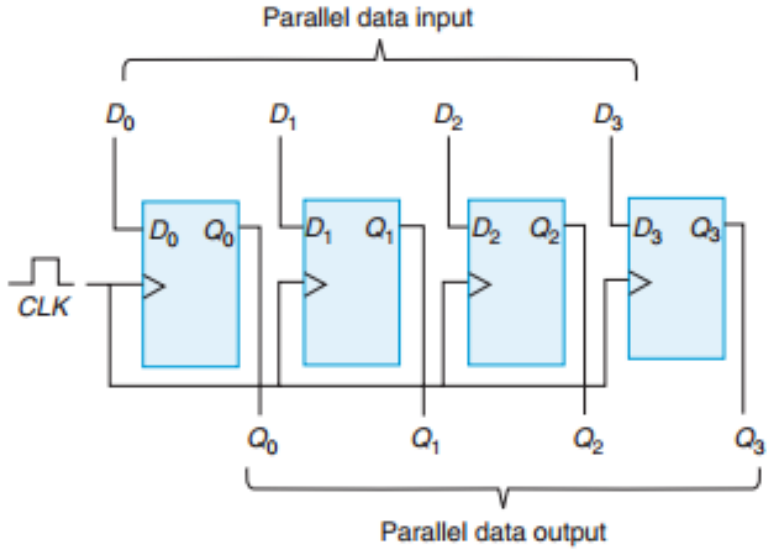


Figure 6.8 A PIPO shift register

Bidirectional Shift Register

- In a bidirectional shift register, the data is shifted in both directions, left and right.
- The direction is controlled by the control input R/L’ .

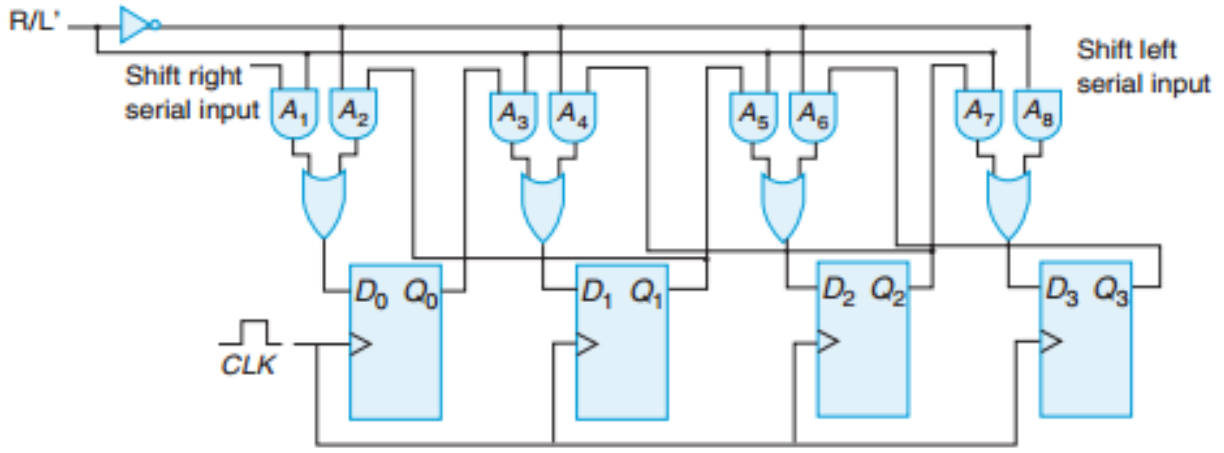


Figure 6.9 A 4-bit bidirectional shift register