FULL SUBTRACTOR

AIM:

To write the verilog program for full subtactor circuit using the software.

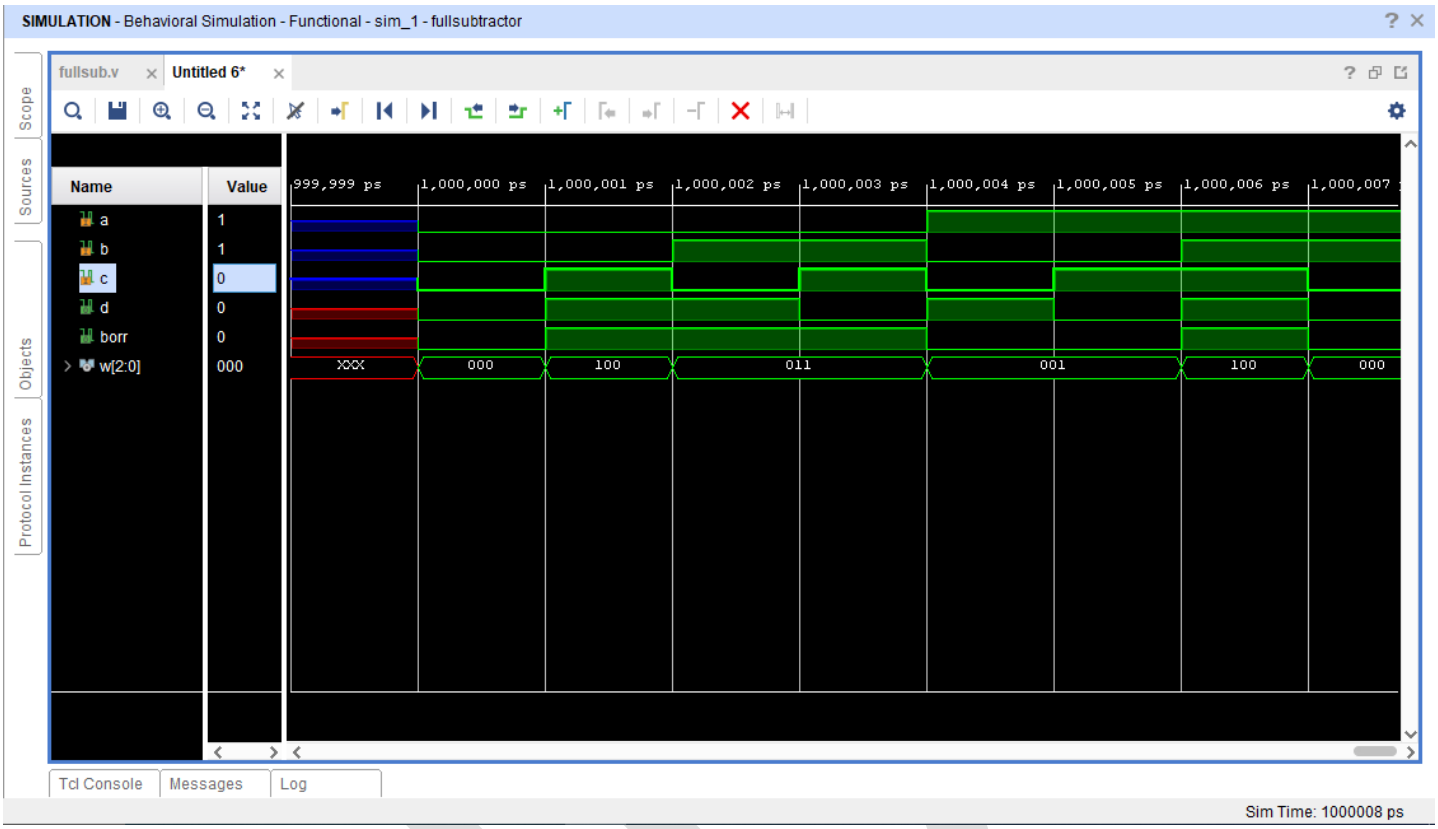
SOFTWARE REQUIRED:

- Amd vivoda 2023.2
- Simulation tools

PROGRAM:

```
module fullsubtractor(a,b,c,d,borr);

input a,b,c;

output d,borr;

wire [2:0]w;

xor g1(w[0],a,b);

and g2(w[1],~a,b);

xor g3(d,w[0],c);

and g4(w[2],~w[0],c);

or g5(borr,w[1],w[2]);

endmodule
```

OUTPUT:


SIMULATION - Behavioral Simulation - Functional - sim_1 - fullsubtractor
fullsub.v
Untitled 6*
Scope
Sources
Objects
Protocol Instances
Name
Value
a
1
b
1
c
0
d
0
borr
0
w[2:0]
000
999,999 ps
1,000,000 ps
1,000,001 ps
1,000,002 ps
1,000,003 ps
1,000,004 ps
1,000,005 ps
1,000,006 ps
1,000,007
XXX
000
100
011
001
100
000
Tcl Console
Messages
Log
Sim Time: 1000008 ps