

FULL ADDER

AIM:

To write the verilog program for full adder circuit using the software.

SOFTWARE REQUIRED:

- Amd vivoda 2023.2
- Simulation tools

PROGRAM:

```
module fulladder(a,b,c,s,cin);  
input a,b,c;  
output s,cin;  
wire [2:0]w;  
xor g1(w[0],a,b);  
and g2(w[1],a,b);  
xor g3(s,w[0],c);  
and g4(w[2],w[0],c);  
or g5(cin,w[1],w[2]);  
endmodule
```

OUTPUT:

