DECODER

AIM:

To write the verilog program for 2:4 decoder circuit using the software.

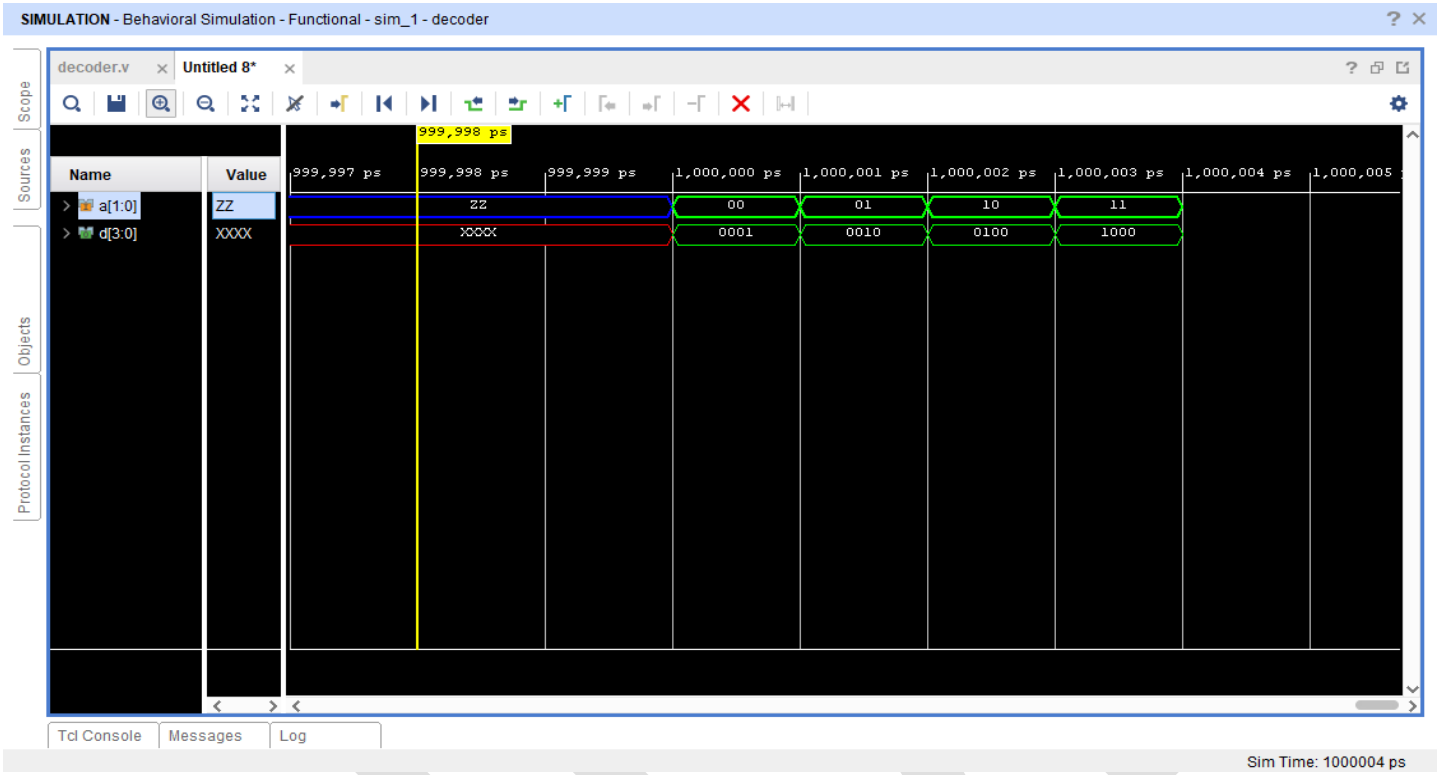
SOFTWARE REQUIRED:

- Amd vivoda 2023.2
- Simulation tools

PROGRAM:

```
module decoder(a,d);

input [1:0]a;

output [3:0]d;

assign d[0]=(~a[1])&(~a[0]);

assign d[1]=(~a[1])&a[0];

assign d[2]=a[1]&(~a[0]);

assign d[3]=a[1]&a[0];

endmodule
```

OUTPUT:


SIMULATION - Behavioral Simulation - Functional - sim_1 - decoder
decoder.v
Untitled 8*
Scope
Sources
Objects
Protocol Instances
Name
Value
a[1:0]
d[3:0]
ZZ
XXXX
999,998 ps
999,997 ps
999,998 ps
999,999 ps
1,000,000 ps
1,000,001 ps
1,000,002 ps
1,000,003 ps
1,000,004 ps
1,000,005
ZZ
00
01
10
11
XXXX
0001
0010
0100
1000
Tcl Console
Messages
Log
Sim Time: 1000004 ps