T FLIPFLOP

AIM:

To write the verilog program for Tflipflop circuit using the software.

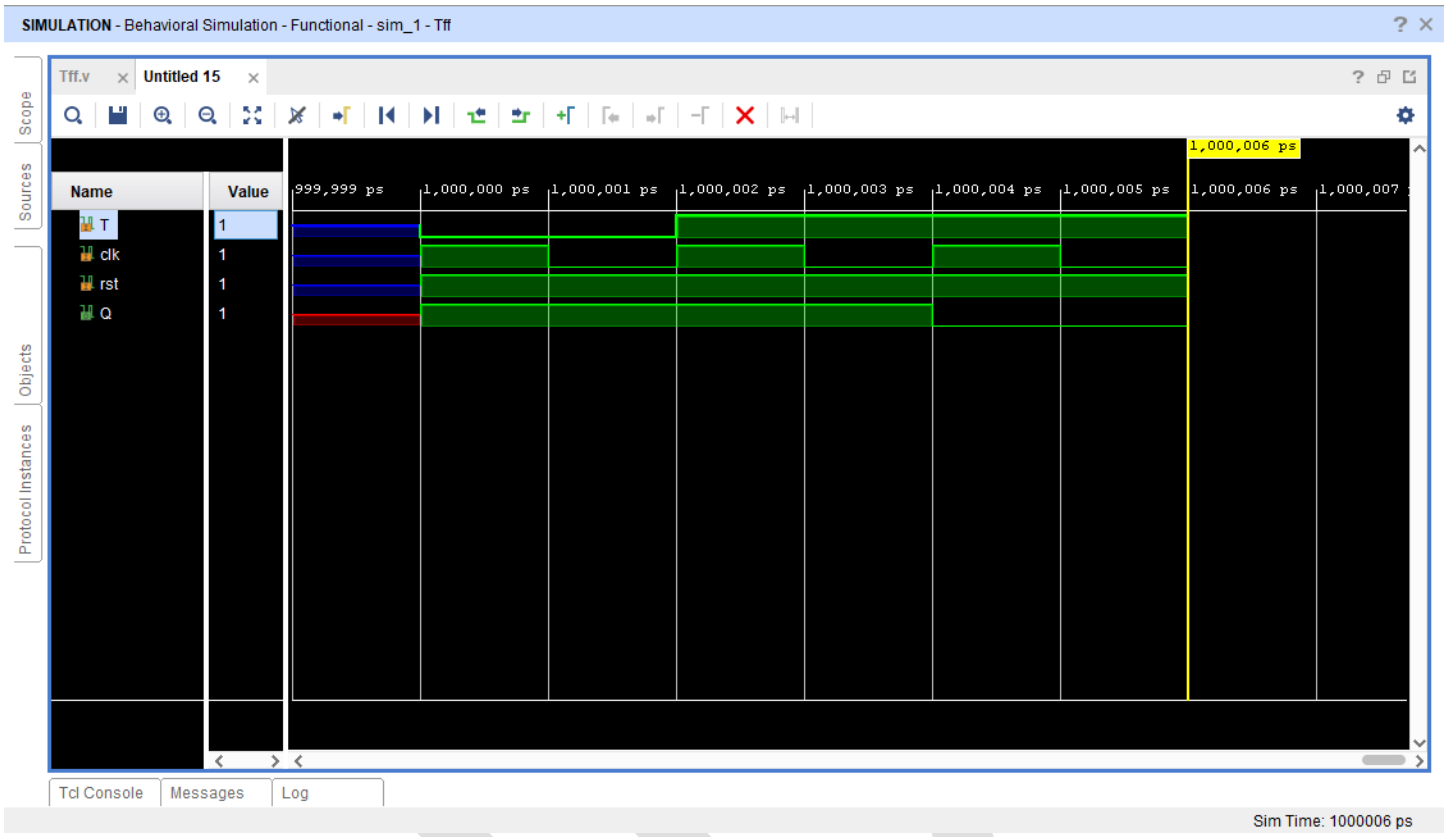
SOFTWARE REQUIRED:

- Amd vivoda 2023.2
- Simulation tools

PROGRAM:

```
module Tff(T,clk,rst,Q);

input T,clk,rst;

output reg Q;

always @(posedge clk or posedge rst)

begin

   if(T==0)

   Q=1'b1;

   else

   Q=~Q;

end

endmodule
```

OUTPUT:


SIMULATION - Behavioral Simulation - Functional - sim_1 - Tff
Tff.v
Untitled 15
Scope
Sources
Objects
Protocol Instances
Name
Value
T
clk
rst
Q
1
1
1
1
999,999 ps
1,000,000 ps
1,000,001 ps
1,000,002 ps
1,000,003 ps
1,000,004 ps
1,000,005 ps
1,000,006 ps
1,000,007
1,000,006 ps
Tcl Console
Messages
Log
Sim Time: 1000006 ps