JK FLIPFLOP

AIM:

To write the verilog program for JKflipflop circuit using the software.

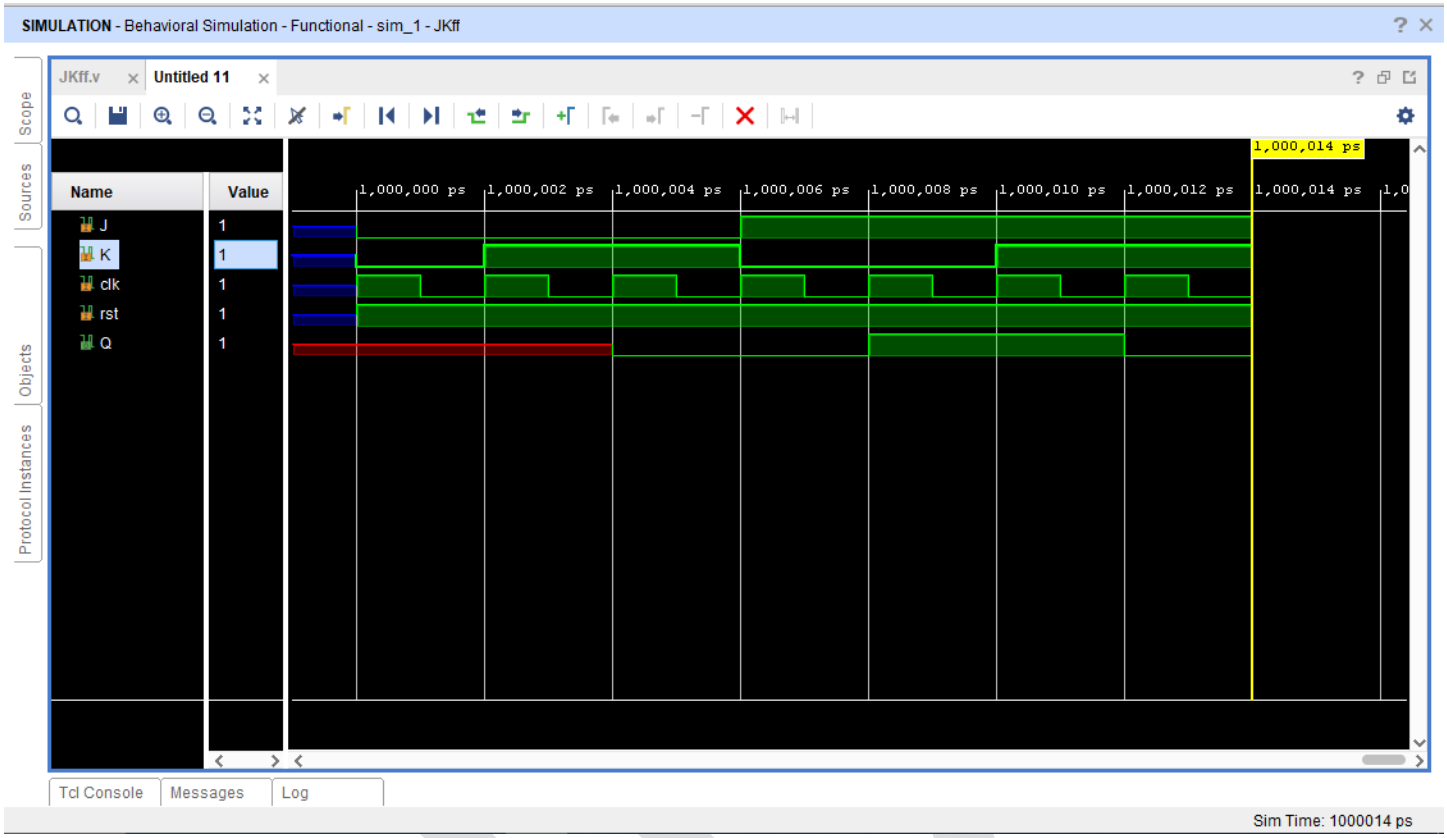
SOFTWARE REQUIRED:

- Amd vivoda 2023.2
- Simulation tools

PROGRAM:

```
module JKff(J, K, clk, rst, Q);
input J, K, clk, rst;
output reg Q;
always @(posedge clk or posedge rst)
begin
    case ({J, K})
      2'b00: Q <= Q;
      2'b01: Q <= 1'b0;
      2'b10: Q <= 1'b1;
      2'b11: Q <= ~Q ;
    endcase
end
endmodule
```

OUTPUT:


SIMULATION - Behavioral Simulation - Functional - sim_1 - JKff
JKff.v
Untitled 11
Scope
Sources
Objects
Protocol Instances
Name
Value
J
K
clk
rst
Q
1
1
1
1
1
1,000,000 ps
1,000,002 ps
1,000,004 ps
1,000,006 ps
1,000,008 ps
1,000,010 ps
1,000,012 ps
1,000,014 ps
1,000,014 ps
Tcl Console
Messages
Log
Sim Time: 1000014 ps