RIPPLE CARRY ADDER

AIM:

To write the verilog program for ripple carry adder circuit using the software.

SOFTWARE REQUIRED:

- Amd vivoda 2023.2
- Simulation tools

PROGRAM:

```
module fulladder(a,b,c,s,ca);

input a,b,c;

output ca,s;

assign s=a^b^c;

assign ca=(a&b)|(b&c)|(c&a);

endmodule


module RCA(a,b,cin,s,ca);

input [3:0]a,b;

input cin;

output [3:0]s;

output ca;

wire [3:1]c;

fulladder f1 (a[0],b[0],cin,s[0],c[1]);

fulladder f2 (a[1],b[1],c[1],s[1],c[2]);
```

```
fulladder f3 (a[2],b[2],c[2],s[2],c[3]);

fulladder f4 (a[3],b[3],c[3],s[3],ca);

endmodule
```

OUTPUT: