SR FLIPFLOP

AIM:

To write the verilog program for SRflipflop circuit using the software.

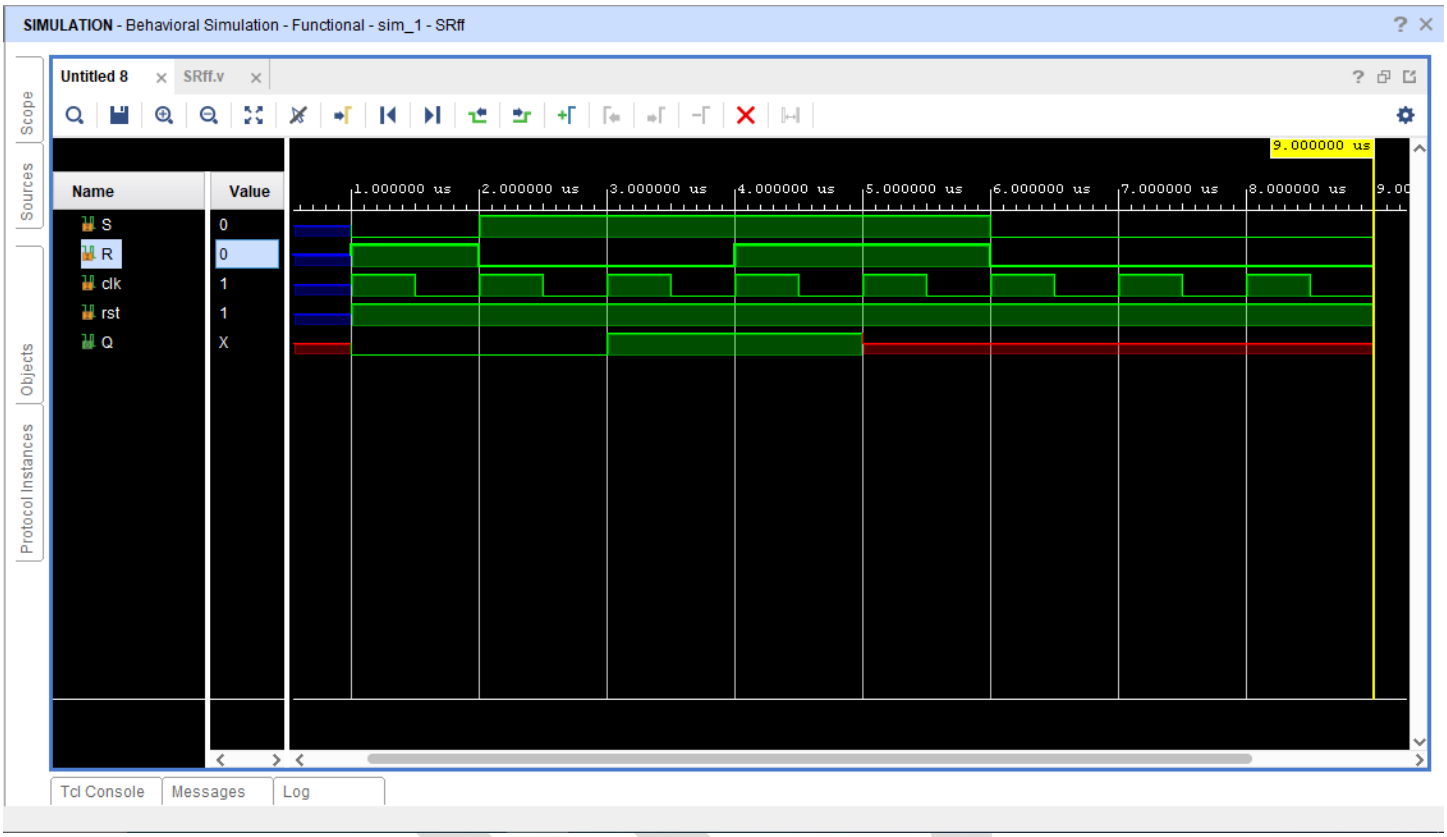
SOFTWARE REQUIRED:

- Amd vivoda 2023.2
- Simulation tools

PROGRAM:

```
module SRff(S, R, clk,rst,Q);
input S,R,clk,rst;
output reg Q;
always @(posedge clk or posedge rst)
begin
    case ({S, R})
      2'b00: Q <= Q;
      2'b01: Q <= 1'b0;
      2'b10: Q <= 1'b1;
      2'b11: Q <= 1'bx;
    endcase
end
endmodule
```

OUTPUT:


SIMULATION - Behavioral Simulation - Functional - sim_1 - SRff
Untitled 8
SRff.v
Scope
Sources
Objects
Protocol Instances
Name
Value
S
R
clk
rst
Q
0
0
1
1
X
1.000000 us
2.000000 us
3.000000 us
4.000000 us
5.000000 us
6.000000 us
7.000000 us
8.000000 us
9.000000 us
Tcl Console
Messages
Log