CLASS 9 HOMEWORK

1. Interrupts vs. polling:

PROS	CONS
• Eliminates nested loops required for interrupts.	• You may require additional documentations like data sheets to keep track of how the SFRs work.
• Much fewer lines of assembly languages.	• Requires special non-cacheable memory allocation for SFRs.
• Removes ambiguities in the code like using counters for calculation or hard coded delays.	• Concept of using SFRs may be difficult to grasp.

4.

(a.) The CPU attends to that ISQ.
(b.) The CPU first attends to the priority 4, sub priority level 2 then resumes back to attending priority 2, sub priority level 3 ISR.
(c.) It continues to attend to priority 4, sub priority level 0 ISR.
(d.) It continues to attend to priority 6, sub priority level 0 ISR.

5.

(a.) Every time an interrupt is generated, the first thing the CPU does is save the contents of the internal CPU registers (called 'contexts') to the stack (in the RAM).
The last thing the CPU does is it restores the contexts back from the RAM into the registers and the CPU reverts to its initial state before the ISR was executed.

(b.) The shadow register set is an extra set of registers, when called upon a particular priority level, the CPU uses these set of registers instead of performing 'context save and restore' and hence saving the time need for it.

8.

(a.) Enabling the Timer2 interrupt: **IEC0SET = 0x100**
Setting flag status to 0: **IFS0CLEAR = 0x100**
Clear IPC2 Register: **IPC2CLEAR = 0x1F**
Setting priority level to 5 and sub priority level to 2: **IPC2SET = 0x16**

(b.) Enabling the Real-Time Clock and Calendar interrupt: **IEC1SET = 0x8000**
Setting flag status to 0: **IFS1CLEAR = 0x8000**
Clear IPC8 Register: **IPC8CLEAR = 0x1F000000**
Setting priority level to 6 and sub priority level to 1: **IPC8SET = 0x19000000**

(c.) Enabling the UART4 Receiver interrupt: **IEC2SET = 0x10**
Setting flag status to 0: **IFS2CLEAR = 0x10**
Clear IPC2 Register: **IPC12CLEAR = 0x1F00**
Setting priority level to 7 and sub priority level to 3: **IPC12SET = 0x1F00**

(d.) Enabling the INT2 external input interrupt: **IEC0SET = 0x800**
Setting flag status to 0: **IFS0CLEAR = 0x800**
Clear IPC2 Register: **IPC2CLEAR = 0x1F**
Setting priority level to 3 and sub priority level to 2: **IPC2SET = 0xE000000**
Configuring to trigger on rising edge: **INTCON = 0x4**

9. Please find attached code.

13. SFR INTCON value (in hex) when it is configured for single vector mode using shadow register set and external interrupt input INT3 is:

INTCON = 0x10008

16. **Please find the attached code.**

17. Please find the attached code.