📄 Authenticated Logic-Zero Encoding via Passive Current Signature for Robust Low-Voltage Signaling

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🧠 Abstract

We propose a novel signaling protocol for digital logic systems, wherein logic ‘0’ is validated not solely by voltage level (0 V), but by the presence of a one-time passive current signature (~12 μA) at the source. The current is governed by a calibrated resistor (termed the Logic-R cell), ensuring intentional logic-zero transmission while downstream logic remains voltage-based and CMOS-compatible. This hybrid symbolic architecture introduces semantic authentication at the physical layer, enabling increased noise resilience, improved fault tolerance, and potential application in secure and low-power digital systems.

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1. Introduction

Traditional binary signaling uses voltage thresholds to encode 1s and 0s, with logic 0 often represented by 0 V. However, in scaled nodes and noisy environments, unintentional zeroes caused by charge leakage or cross-talk can compromise logic integrity.

We introduce Authenticated Logic-Zero Encoding (ALZP), where 0 V is considered valid only when accompanied by a current signature detected at the transmission origin. This

12 µA current, generated passively through a precision resistor, functions as a symbolic signature—ensuring every logic-zero has purpose behind it.

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2. Encoding Specification

Truth Table

Logic State	Voltage	Authenticator Current	Interpretation
Logic ‘1’	0.5 V	—	Standard logic high
Logic ‘0’	0 V	≈12 µA at source only	Authenticated logic low

• Receiver logic only detects voltage.

• Current validation is done once at the source node.

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3. Authenticator Implementation

The authenticator pulse is generated passively:

• When V = 0 V is asserted,

• A resistor of defined value allows a passive current (I) to flow:

{FBEEB710-LaTeX-opener} R = \frac{V_{bias}}{I} \quad \Rightarrow \quad R = \frac{0.5,\text{V}}{12,\mu\text{A}} \approx 41.67,\text{kΩ} {EA1D9CB0-LaTeX-closer}

This current is sensed locally by a verification circuit before allowing the signal to propagate.

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4. Logic-R Standard Cell Specifications

Parameter	Value
Target Resistance (R)	41.67 kΩ ±2%
Material Candidates	Tantalum Nitride (TaN), NiCr, Graphene
Temperature Coefficient	≤ ±10 ppm/°C
Calibration	Optional digital trimming matrix
Area Overhead	≤ 3× standard inverter cell
EDA Compatibility	Requires analog-aware verification pass

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5. Advantages Over Conventional Signaling

Benefit	Description
Noise Immunity	Prevents false 0s due to leakage or crosstalk
Thermal Stability	Passive component avoids switching spikes
Security	Authenticator acts as physical watermark
CMOS Compatibility	Downstream logic remains unmodified
Energy Efficiency	0.5 V swing, low current, minimal toggling

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6. Use Cases

• Secure low-power microcontrollers

• Radiation-tolerant or safety-critical SoCs

• Analog-digital bridge interfaces

• Symbolic logic systems for post-CMOS architectures

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7. Challenges & Mitigations

Challenge	Solution Strategy
Resistor stability at nanoscale	Use low-TCR materials with post-fab trimming
Process drift	Include calibration pulse routines
EDA toolchain limitations	Abstract into source-side IP or verification block
Clock alignment with validation	Gated sampling within a defined strobe window

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8. Conclusion

This architecture transforms logic-zero into an active participant in digital meaning, authenticated at origin and trusted downstream. By assigning symbolic certainty through a passive physical signature, we redefine low-power logic design around intentionality, resilience, and elegant simplicity.