	R	W	A_1	A_2	A_3	D_3	T_1	T_2	alu-a	alu-b	ALU	PC	ts	M-add	RF RW	C	Z	IR	T_4
HKt	1	0	X	X	XX	XX	X	X	0	1	00	1	11	01	X	0	0	00	0	0	1	X
bring-regdata	0	0	1	1	X	X	0	0	0	0	00	0	00	00	X	X	X	10	0	0	0	X
ALU-op-cz	0	0	X	X	XX	XX	X	X	1	0	01	0	10	00	X	X	X	00	1	1	0	X
write-back	0	0	X	X	00	01	X	X	0	0	00	0	00	00	X	X	X	01	0	0	0	X
write-back_rb	0	0	X	X	01	01	X	X	0	0	00	0	00	00	X	X	X	01	0	0	0	X
bring-imm	0	0	1	X	XX	XX	0	1	0	0	00	0	00	00	X	X	X	10	0	0	0	X
store-mem	0	1	1	X	XX	XX	X	X	0	0	00	0	00	00	X	0	1	00	0	0	0	X
load-from mem	1	0	X	X	10	11	X	X	0	0	00	0	00	00	X	0	1	01	0	0	0	X
ALU-op-cz	0	0	X	X	XX	XX	X	X	1	0	01	0	10	00	X	X	X	00	0	1	0	X
store-PC	0	0	X	X	10	10	X	X	0	1	00	1	01	00	X	X	X	01	0	0	0	X
dec-PC	0	0	X	X	XX	XX	X	X	0	1	00	1	01	01	X	X	X	00	0	0	0	X
PC-offset-6	0	0	X	X	XX	XX	X	X	0	1	01	1	11	01	X	X	X	00	0	0	0	X
PC-offset-9	0	0	X	X	XX	XX	X	X	0	1	10	0	11	01	X	X	X	00	0	0	0	X
t_2-PC	0	0	X	X	XX	XX	X	X	0	0	00	0	00	10	X	X	X	00	0	0	0	X
LM-load reg	1	0	X	X	11	11	X	X	0	0	00	0	00	00	1	1	0	01	0	0	0	1
check-z2	0	0	X	X	XX	XX	X	X	0	0	00	0	00	00	0	X	X	00	0	0	0	0
SM-store mem	0	1	0	X	XX	XX	X	X	0	0	00	0	00	00	1	1	0	10	0	0	0	1
priority_out	0	0	X	X	XX	XX	X	X	0	0	00	0	00	00	X	X	X	00	0	0	0	1
data_out	0	0	X	X	10	00	X	X	0	0	00	0	00	00	X	X	X	01	0	0	0	X
bring_imm2	0	0	X	1	XX	XX	1	1	0	0	00	0	00	00	X	X	X	10	0	0	0	X