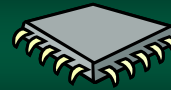




## Processors

Part 2

1



## Processors

What are they? Besides awesome!

2

### Computer Processors

- The *Central Processing Unit (CPU)* is the most complex part of a computer
- In fact, it is the computer!
- It works far different from a high-level language
- *Thousands* of processors have been developed



Fall 2024

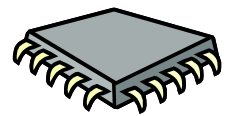
Seaverick Stein - CS66 - CS66.01

3

3

### Some Famous Computer Processors

- RCA 1802
- Intel 8086
- Zilog Z80
- MOS 6502
- Motorola 68000
- ARM



Fall 2024

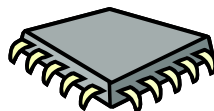
Seaverick Stein - CS66 - CS66.01

4

4

### Computer Processors

- Each processor functions differently
- Each is designed for a specific purpose – *form follows function*



Fall 2024

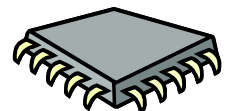
Seaverick Stein - CS66 - CS66.01

5

5

### Computer Processors

- But all share some basic properties and building blocks...
- Computer hardware is divided into two "units"
  1. Control Logic Unit
  2. Execution Unit



Fall 2024

Seaverick Stein - CS66 - CS66.01

6

6

## Control Logic Unit (CLU)

- *Control Logic Unit (CLU)* controls the processor
- Determines when instructions can be executed
- Controls internal operations
  - fetch & decode instructions
  - invisible to running programs



Fall 2024

Secretariat State - Cook - CSU 35

7

7

## Execution Unit

- *Execution Unit (EU)* contains the hardware that **executes** tasks (your programs)
- Different in many processors
- Modern processors often use multiple execution units to execute instructions in parallel to improve performance

Fall 2024

Secretariat State - Cook - CSU 35

8

8

## Execution Unit – The ALU

- *Arithmetic Logic Unit* is part of the Execution Unit and performs all calculations and comparisons
- Processor often contains special hardware for integer and floating point



Fall 2024

Secretariat State - Cook - CSU 35

9

9

## Registers

Where the work is done

10

## Registers

- In high level languages, you put active data into variables
- However, it works quite different on processors
- All computations are performed using *registers*



Fall 2024

Secretariat State - Cook - CSU 35

11

11

## What – exactly – is a register?

- A *register* is a location, on the processor itself, that is used to store temporary data
- Think of it as a special global "variable"
- Some are accessible and usable by a programs, but **many are hidden**



Fall 2024

Secretariat State - Cook - CSU 35

12

12

## What are registers used for?

- Registers are used to store anything the processor needs to keep track of
- Designed to be fast!
- Examples:
  - the result of calculations
  - status information
  - memory location of the running program
  - and much more...

Fall 2024

Secrecy: State - Cook - CS50.10

13

13

## General Purpose Registers

- *General Purpose Registers (GPR)* don't have a specific purpose
- They are designed to be used by programs – however they are needed
- Often, you must use registers to perform calculations

Fall 2024

Secrecy: State - Cook - CS50.10

14

14

## Special Registers

- There are a number of registers that are used by the Control Logic Unit and cannot be accessed by your program
- This includes registers that control how memory works, your program execution thread, and much more.

Fall 2024

Secrecy: State - Cook - CS50.10

15

15

## Special Registers

- *Instruction Pointer (IP)*
  - also called *the program counter*
  - keeps track of the address of your running program
  - think it as the "line number" in your Java program – the one is being executed
  - it can be changed, but only indirectly (*using control logic – which we will cover later*)

Fall 2024

Secrecy: State - Cook - CS50.10

16

16

## Special Registers

- *Status Register*
  - contains Boolean information about the processors current state
  - we will use this later, indirectly
- *Instruction Register (IR)*
  - stores the current instruction (being executed)
  - used internally and invisible to your program

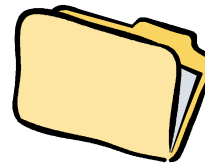
Fall 2024

Secrecy: State - Cook - CS50.10

17

17

## Register Files



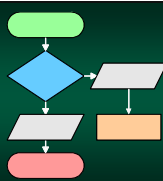
- All the related registers are grouped into a *register file*
- Different processors access and use their register files in very different ways
- Sometimes registers are implied or hardwired

Fall 2024

Secrecy: State - Cook - CS50.10

18

18



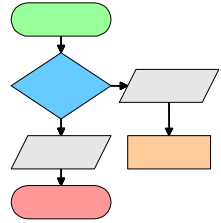
## Instructions

It's all just a bunch of bytes

19

## Instructions

- You are used to writing programs in high level programming languages
- Examples:
  - C#
  - Java
  - Python
  - Visual Basic

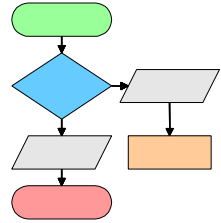


Fall 2024 Sacramento State - CSIS - CSIS 35 20

20

## High-Level Programming

- These are *third-generation languages*
- They are designed to isolate you from architecture of the machine
- This layer of abstraction makes programs "portable" between systems



Fall 2024 Sacramento State - CSIS - CSIS 35 21

21

## Instructions

- Processors do not have the constructs you find in high-level languages
- Examples:
  - Blocks
  - If Statements
  - While Statements
  - ... etc

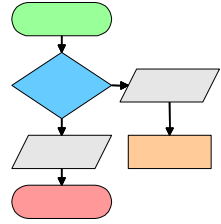


Fall 2024 Sacramento State - CSIS - CSIS 35 22

22

## Instructions

- Processors can only perform a series of simple tasks
- These are called *instructions*
- Examples:
  - add two values together
  - copy a value
  - jump to a memory location

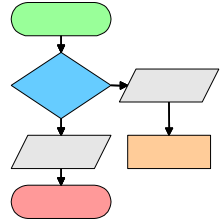


Fall 2024 Sacramento State - CSIS - CSIS 35 23

23

## Instructions

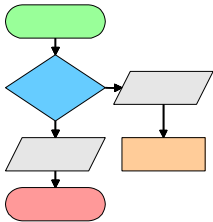
- These instructions are used to create all logic needed by a program
- We will cover how to do this during the semester



Fall 2024 Sacramento State - CSIS - CSIS 35 24

24

## Processor Instruction Set



- A processor's *instruction set* defines all the available instructions
- The instructions and their respective formats are very different for each processor

Fall 2024

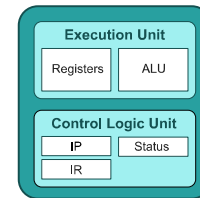
Secomware, Bonn - C&C - CSU 35

25

25

## Components of a Processor

### Processor



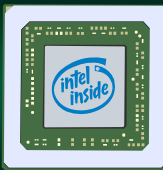
Fall 2024

Secomware, Bonn - C&C - CSU 35

26

26

## The Intel 8086



It was simple at first...

Fall 2024

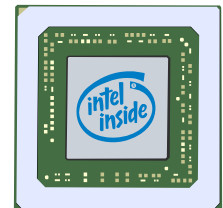
Secomware, Bonn - C&C - CSU 35

27

27

## The Intel 8086

- The Intel x86 is the main processor used by servers, laptops, and desktops
- It has evolved continuously over a 40+ year period



Fall 2024

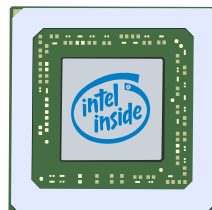
Secomware, Bonn - C&C - CSU 35

28

28

## The Original x86

- First "x86" was the 8086
- Released in 1978
- Attributes:
  - 16-bit registers
  - 16 registers
  - could access of 1MB of RAM (in 64KB blocks using a special "segment" register)



Fall 2024

Secomware, Bonn - C&C - CSU 35

29

29

## Original x86 Registers

- The original x86 contained 16 registers
- 8 can be used by your programs
- The other 8 are used for memory management



Fall 2024

Secomware, Bonn - C&C - CSU 35

30

30

## Original x86 Registers

- The x86 processor has evolved continuously over the last 4 decades
- It first jumped to 32-bit, and then, again, to 64-bit
- This has resulted in many of the registers have strange names

Fall 2024

Segmentation: Base - Code - CS: 32

31

31

## Original x86 Registers

- 8 Registers can be used by your programs
  - Four General Purpose: **AX, BX, CX, DX**
  - Four pointer index: **SI, DI, BP, SP**
- The remaining 8 are restricted
  - Six segment: CS, DS, ES, FS, GS, SS
  - One instruction pointer: IP
  - One status register – used in computations

Fall 2024

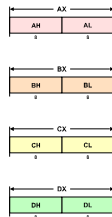
Segmentation: Base - Code - CS: 32

32

32

## Original General-Purpose Registers

- However, back then (and now too) it is very useful to store 8-bit values
- So, Intel chopped 4 of the registers in half
- These registers have generic names of A, B, C, D



Fall 2024

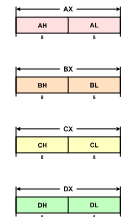
Segmentation: Base - Code - CS: 32

33

33

## Original General-Purpose Registers

- The first and second byte can be used separately or used together
- Naming convention
  - high byte has the suffix "H"
  - low byte has the suffix "L"
  - for both bytes, the suffix is "X"



Fall 2024

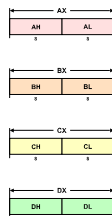
Segmentation: Base - Code - CS: 32

34

34

## Original General-Purpose Registers

- This essentially doubled the number of registers
- So, there are:
  - four 16-bit registers or
  - eight 8-bit registers
  - ...and any combination you can think off



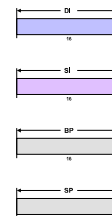
Fall 2024

Segmentation: Base - Code - CS: 32

35

35

## Last the 4 Registers



- The remaining 4 registers were not cut in half
- Used for storing indexes (for arrays) and pointers
- Their purpose
  - DI – destination index
  - SI – source index
  - BP – base pointer
  - SP – stack pointer

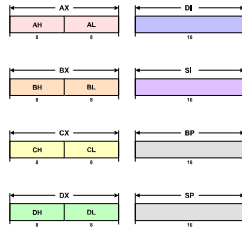
Fall 2024

Segmentation: Base - Code - CS: 32

36

36

## Original 16-Bit Registers



Fall 2024

Segmentation: Base - Cx86 - CS:32

37

37

## Evolution to 32-bit

- When the x86 moved to 32-bit era, Intel expanded the registers to 32-bit
  - the 16-bit ones still exist
  - they have the prefix "e" for extended
- New instructions were added to use them



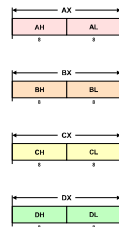
Fall 2024

Segmentation: Base - Cx86 - CS:32

38

38

## Original Registers



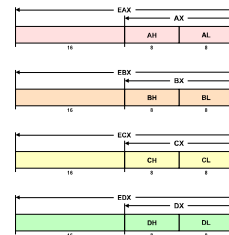
Fall 2024

Segmentation: Base - Cx86 - CS:32

39

39

## Expansion to 32-bit



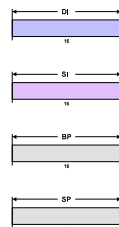
Fall 2024

Segmentation: Base - Cx86 - CS:32

40

40

## Original Registers



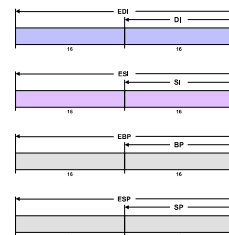
Fall 2024

Segmentation: Base - Cx86 - CS:32

41

41

## Expansion to 32-bit

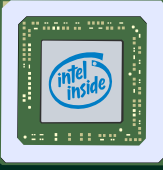


Fall 2024

Segmentation: Base - Cx86 - CS:32

42

42



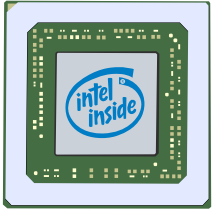
## Chaotic Move to 64-Bit

Intel vs. AMD

43

## The Move to 64-Bit


- By the year 2000, Intel needed to move to 64-bit
- Intel could have, yet again, extended the x86
- However, Intel decided to abandon the x86 in lieu of new design



44

## The Itanium


- The Itanium was a radically different from the 8086.
- However, it was completely incompatible with existing x86 programs
- Old programs would have to run through an emulator



45

## AMD's Response to the Itanium


- Advanced Micro Devices (AMD), to Intel's chagrin, decided to – *once again* – extend the x86
- It could run old programs without emulation



46

## Itanium's Problems

- The AMD-64 could run existing programs without emulation
- The Itanium design made it difficult for compilers to make optimized machine code



47

## Itanium's Downfall

*“The Itanium approach...was supposed to be so terrific until it turned out that the wished-for compilers were basically impossible to write.”*

– Donald Knuth

48



## The Result

- The AMD-64 was a huge commercial *success*
- The Itanium was a huge commercial *failure*
- Intel, dropped the Itanium and started making 64-bit x86 using AMD's design



Fall 2004

Secretariat State - Cook - CSU 35

49

49



## The 64-bit Era

Intel vs. AMD

50

## The 64-bit Era

- After the Itanium's disastrous flop – Intel resorted to making AMD-64 compatible processors.
- The classic term "x86" refers to the 32-bit and 16-bit processor family



Fall 2004

Secretariat State - Cook - CSU 35

51

51

## The 64-bit Era

- The term "x64" is used to refer to the AMD's 64-bit extension
- However, the two terms, x86 and x64, are often used interchangeably



Fall 2004

Secretariat State - Cook - CSU 35

52

52

## x64 Registers

- Existing registers were extended by adding 32-bits
- 8 additional registers were added – needed by this era
- 64-bit registers have the prefix "*r*"



Fall 2004

Secretariat State - Cook - CSU 35

53

53

## x64 Simplified Hardware (best it could)

- It is now possible to get 8-bit values from all registers
- This makes the hardware simpler and more consistent
- Also, many, many archaic, x86 instructions were dropped



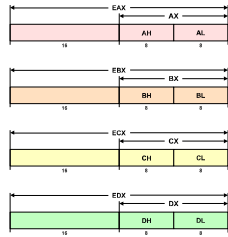
Fall 2004

Secretariat State - Cook - CSU 35

54

54

## Expansion to 64-bit

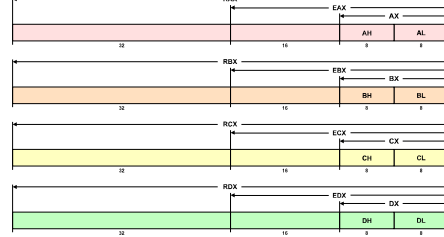


Fall 2024

Segmentation State - Cook - CS: 32

55

## Expansion to 64-bit

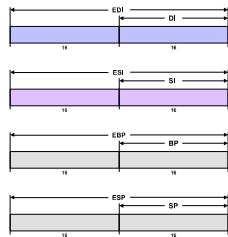


Fall 2024

Segmentation State - Cook - CS: 32

56

## Expansion to 64-bit

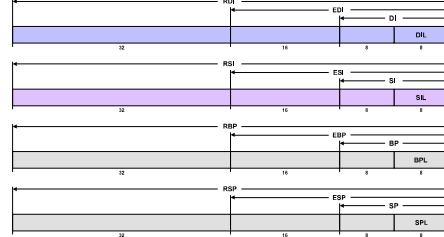


Fall 2024

Segmentation State - Cook - CS: 32

57

## Expansion to 64-bit

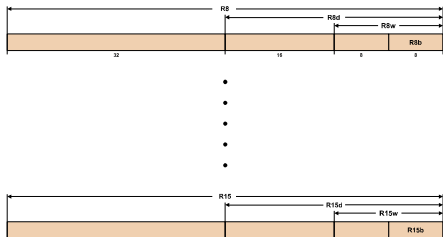


Fall 2024

Segmentation State - Cook - CS: 32

58

## New 64-bit Registers: R8...R15



Fall 2024

Segmentation State - Cook - CS: 32

59

## 64-Bit Register Table

Register	32 bit	16-bit	8 bit High	8 bit Low
<b>rax</b>	<b>eax</b>	<b>ax</b>	<b>ah</b>	<b>al</b>
<b>rbx</b>	<b>ebx</b>	<b>bx</b>	<b>bh</b>	<b>bl</b>
<b>rcx</b>	<b>ecx</b>	<b>cx</b>	<b>ch</b>	<b>cl</b>
<b>rdx</b>	<b>edx</b>	<b>dx</b>	<b>dh</b>	<b>dl</b>
<b>rsi</b>	<b>esi</b>	<b>si</b>		<b>sil</b>
<b>rdi</b>	<b>edi</b>	<b>di</b>		<b>dil</b>
<b>rbp</b>	<b>ebp</b>	<b>bp</b>		<b>bpl</b>
<b>rsp</b>	<b>esp</b>	<b>sp</b>		<b>spl</b>

Fall 2024

Segmentation State - Cook - CS: 32

60

## 64-Bit Register Table

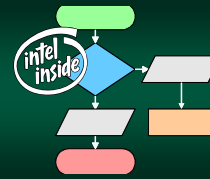
Register	32-bit	16-bit	8-bit High	8-bit Low
r8	r8d	r8w		r8b
r9	r9d	r9w		r9b
r10	r10d	r10w		r10b
r11	r11d	r11w		r11b
r12	r12d	r12w		r12b
r13	r13d	r13w		r13b
r14	r14d	r14w		r14b
r15	r15d	r15w		r15b

Fall 2024

Sebastien Sené - Cosh - CS50 SE

61

61



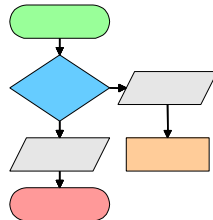
## Basic Intel x86 Instructions

Feel the pow-wah of the x86!

62

## Basic Intel x86 Instructions

- Each x86 instruction can have up to 2 operands
- Operands in x86 instructions are very versatile
- Each operand can be either a memory address, register or an immediate value



Fall 2024

Sebastien Sené - Cosh - CS50 SE

63

63

## Types of Operands

- Registers
- Address in memory
- Register pointing to a memory address
- Immediate

Fall 2024

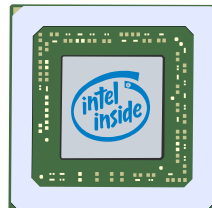
Sebastien Sené - Cosh - CS50 SE

64

64

## Intel x86 Instruction Limits

- There are some limitations...
- Some instructions must use an immediate
- Some instructions require a specific register to perform calculations



Fall 2024

Sebastien Sené - Cosh - CS50 SE

65

65

## Intel x86 Instruction Limits

- A register must always be involved
  - processors use registers for all activity
  - both operands cannot access memory at the same time
  - the processor has to have it at some point!*
- Also, obviously, the receiving field cannot be an immediate value

Fall 2024

Sebastien Sené - Cosh - CS50 SE

66

66

## Instruction: Move

- The Intel *Move Instruction* combines transfer, load and store instructions under one name
- ... well, that's something the assembler does for us – but, we'll cover that soon
- "Move" is a tad confusing – it copies data

Fall 2024

Securities State - Cook - CSU 35

67

## Instruction: Move

**MOV** *destination, source*

Immediate, Register, Memory

Register, Memory

Fall 2024

Securities State - Cook - CSU 35

68

67

68

## Example: Move immediate

**MOV** *rax*, 42

Source is a immediate constant

Same as Java  
*rax* = 42;

Destination is *rax*

Fall 2024

Securities State - Cook - CSU 35

69

69

## Example: Transfer

**MOV** *rbx*, *rax*

Source is *rax*

Same as Java  
*rbx* = *rax*;

Destination is *rbx*

Fall 2024

Securities State - Cook - CSU 35

70

70

## Example: Load

**MOV** *rax*, *total*

"total" is memory location

Destination is *rax*

Fall 2024

Securities State - Cook - CSU 35

71

71

## Example: Store

**MOV** *counter*, *rax*

Source is *rax*

Memory location named 'Counter'

Fall 2024

Securities State - Cook - CSU 35

72

72

## Example: "A" Register

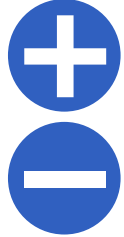
# So many options!

```
mov al, 42      #low byte
mov ah, 13      #high byte
mov ax, 1947    #both bytes
```

73

## Instruction: Add & Subtract

- The Add and Subtract instructions take two operands and store the result in the first operand
- This is the same as the **+=** and **-=** operators used in Visual Basic .NET, C, C++, Java, etc...



74

## Instruction: Add

**ADD** *target* , *value*

Immediate, Register, Memory

Register, Memory

75

## Example: Move register to memory

Move memory into rax

```
MOV rax, counter
ADD rax, 2
```

Same as Java  
`rax += 2;`

76

## Instruction: And & Or

- The Bitwise And & Bitwise Or instructions take two operands and stores the result in the second operand
- This is the same as the **&=** and **|=** operators used in C, C++, Java, etc...



77

## Instruction: Logical And

**AND** *target* , *value*

Immediate, Register, Memory

Register, Memory

78

## Example: Logical Or

```
#Convert 5 to ASCII '5'  
MOV  rax, 5  
OR   rax, 0x30
```

0011 0000

79

## Call Instruction

- The *Call Instruction* causes the processor to start running instructions at a specified memory location (a subroutine)
- Subroutines are analogous to the functions you wrote in Java
- Once it completes, execution returns from the subroutine and continues after the call

80

## Call Instruction

**CALL** *address*

Usually a label – a constant that holds an address

81

## Example: Print an integer

```
#Using the CSC35 library
```

```
MOV  rdx, 1846  
CALL PrintInteger
```

This name is an address

82