

### Practical: 4

#### Aim: To implement various 4-bit arithmetic Micro-operations using arithmetic unit.

#### Theory:

Arithmetic micro operation of the form  $L: R_A \leftarrow (R_A + R_B)$  refers to two data items contained in  $R_A$  and  $R_B$  input to a parallel adder with the result begin stored back in  $R_A$  (Fig.). Loading of the result in  $R_A$  is subject to the availability of the control signal designed as  $L$  (that is load control of  $R_A$ ). Note that adder begin a combinational logic, the adder output is available providing AND word gates on the data paths from  $R_A$  and  $R_B$  to the adder under the control signal  $C$  (Fig.) the control signal 'C' and 2's complement are at logic '0' for add operation.

The subtract micro operation  $L: R_A \leftarrow (R_A - R_B)$  in 2's complement arithmetic has the form  $L_A: R_A \leftarrow R_A + R_B + 1$  where  $R_B$  is 1's complement of  $R_B$  the hardware implementing both Add/Subtract operation is shown if Fig. Where the control signals 'C' and 2's complement are at logic '1' for subtract operation and '0' for add operation. The EX-OR word gate inverts the content of  $R_B$  circuit in Fig. is so designed that it can support both 1's and 2's complement of  $R_B$  as input to the adder.

The other common arithmetic micro operations are increment, decrement, 1's complement, 2's complement etc. Each of these operations can be implemented with the help of multiple micro operations on the structure of Fig.

Prepare a table for above operations and write micro operation and control signal for given fig.

For Example:

**Operation**  
Increment

**Micro-operation**  
 $R_B \leftarrow 1$   
 $R_A \leftarrow R_A + R_B$

**Control signal**  
Set  $R_B$  to 1  
Set  $C$  to 0  
 $L_A$  at  $R_A$

#### Circuit Diagram:

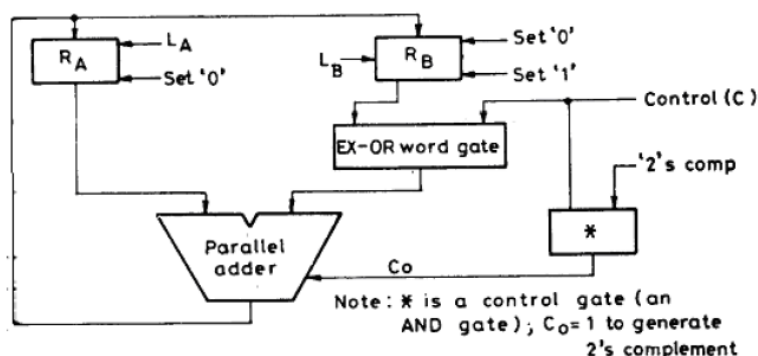


Table of Micro-operation:

Operations	Input										Output			
	$R_{A0}$	$R_{A1}$	$R_{A2}$	$R_{A3}$	$R_{B0}$	$R_{B1}$	$R_{B2}$	$R_{B3}$	C	2'S	$R_{Y0}$	$R_{Y1}$	$R_{Y2}$	$R_{Y3}$
ADD $R_A, R_B$	0	1	0	1	1	0	1	0	0	0	1	1	1	1
SUB $R_A, R_B$	1	0	1	0	0	1	0	1	1	1	0	1	0	1
Increment $R_A$	0	1	0	1	0	0	0	0	0	1	0	1	1	0
Decrement $R_A$	0	1	0	1	0	0	0	0	1	0	0	1	0	0
Increment $R_B$	0	0	0	0	1	0	1	0	0	1	1	0	1	1
Decrement $R_B$	0	0	0	0	1	0	1	0	-	-	-	-	-	-
1's complement $R_A$	0	1	0	1	0	0	0	0	-	-	-	-	-	-
2's complement $R_A$	0	1	0	1	0	0	0	0	-	-	-	-	-	-
1's complement $R_B$	0	0	0	0	1	0	1	0	1	0	0	1	0	1
2's complement $R_B$	0	0	0	0	1	0	1	0	1	1	0	1	1	0
Transfer $R_A$	0	1	0	1	0	0	0	0	0	0	0	1	0	1
Transfer $R_B$	0	0	0	0	1	0	1	0	0	0	1	0	1	0

Practical Circuit Diagram:

