Practical-5

Aim: To implement various 4-bit arithmetic Micro-operations using arithmetic unit.

Theory:

Arithmetic micro operation of the form L: $R_A \leftarrow (R_A + R_B)$refers to two data items contained in R_A and R_B input to a parallel adder with the result being stored back in R_A (Fig.). Loading of the result in R_A is subject to the availability of the control signal designated as L (that is load control of R_A). Note that adder being a combinational logic, the adder output is available after a delay of the associated combinational circuit. Input to adder may be also controlled by providing AND word gates on the data paths from R_A and R_B to the adder under the control signal C (Fig.). the control signals `C' and 2's complement are at logic `0' for add operation.

The subtract micro operation L: $R_A \leftarrow (R_A - \underline{R_B})$ in 2's complement arithmetic has the form $L_A : R_A <-- R_A + R_B + 1$ where R_B is 1's complement of R_B the hardware implementing both Add/Subtract operation is shown in Fig. Where the control signals `C' and 2's complement are at logic `1' for subtract operation and `0' for add operation. The EX-OR word gate inverts the content of R_B for C = 1 which also makes input carry $C_O = 1$ to make 2's complement of R_B circuit in Fig. is so designed that it can support both 1's and 2's complement of R_B as input to the adder.

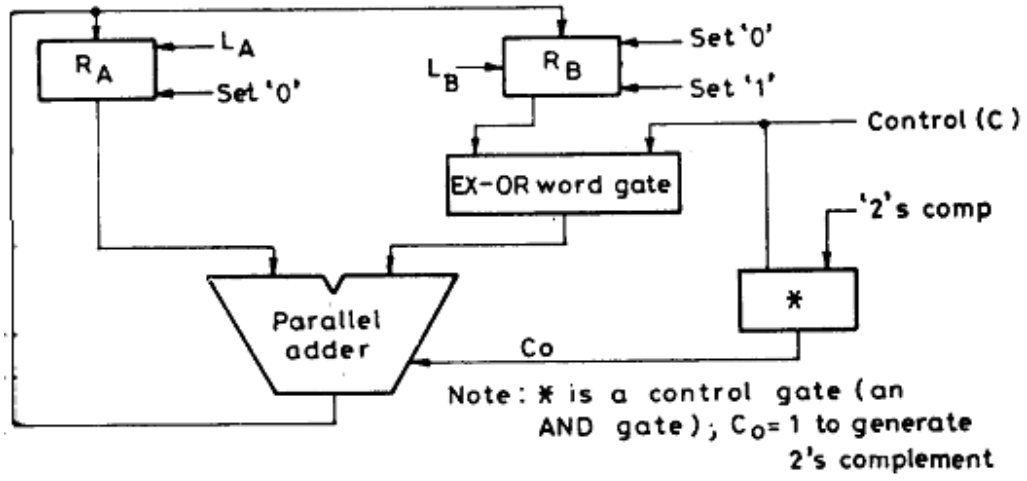
The other common arithmetic micro operations are increment, decrement, 1's complement, 2's complement etc. Each of these operations can be implemented with the help of multiple micro operations on the structure of Fig.

Prepare a table for above operations and write micro operation and control signal for given fig.

For Example:

Operation	**Microoperation**	**Control signal**
Increment	$R_B \leftarrow 1$	1.Set R_B to 1
	$R_A \leftarrow R_A + R_B$	2.Set C to 0
		3. L_A *at* R_A

Circuit Diagram:



Circuit Diagram:

TABLE: MICROOPERATION

Operation	R_{A0}	R_{A1}	R_{A2}	R_{A3}	R_{B0}	R_{B1}	R_{B2}	R_{B3}	C	2'S
ADD R_A,R_B	0	1	0	1	1	0	1	0	0	0
SUBTRACTION R_A, R_B	0	1	0	1	1	0	1	0	1	1
INCREMENT R_A	0	1	0	1	0	0	0	0	0	1
DECREMENT R_A	0	1	0	1	0	0	0	0	1	0
INCREMENT R_B	0	0	0	0	1	0	1	0	0	1
DECREMENT R_B	0	0	0	0	1	0	1	0		
1'S COMPLEMENT R_A	0	1	0	1	0	0	0	0		
2'S COMPLEMENT R_A	0	1	0	1	0	0	0	0		
1'S COMPLEMENT R_B	0	0	0	0	1	0	1	0	1	0
2'S COMPLEMENT R_B	0	0	0	0	1	0	1	0	1	1
TRANSFER A	0	1	0	1	0	0	0	0	0	0
TRANSFER B	0	0	0	0	1	0	1	0	0	0