GANPAT UNIVERSITY

FACULTY OF ENGINEERING & TECHNOLOGY

Programme	Bachelor of Technology	Branch/Spec.	Computer Engineering / Information Technology
Semester	V	Version	2.0.0.0
Effective from Academic Year	2020-21	Effective for the batch Admitted in	July 2018
Subject code	2CEIT501	Subject Name	Computer Architecture & Organization

Teaching scheme						Examination scheme (Marks)			
(Per week)	Lecture (DT)		Practical (Lab.)		Total		CE	SEE	Total
	L	TU	P	TW					
Credit	3	0	1	-	4	Theory	40	60	100
Hours	3	0	2	-	5	Practical	30	20	50

Pre-requisites:

Digital Electronics

Objectives of the course:

1. To understand the structure, function and characteristics of computer systems.
2. To understand the design of the various functional units and components of computer.
3. To understand the basic concepts of pipeline and vector processing.
4. To understand the memory hierarchy.
5. To learn the assembly language programming.

Theory syllabus

Unit	Content	Hrs
1	**Overview of Register Transfer and Micro Operations:** Register Transfer Language, Register Transfer, Bus & Memory Transfer, Arithmetic Micro-Operations, Logic Micro-Operations, Shift Micro Operations, Arithmetic Logic Shift Unit.	05
2	**Basic Computer Organization and Design:** Instruction Codes, Computer Registers, Computer Instructions, Timing & Control, Instruction Cycle, Memory-Reference Instructions, Input-Output & Interrupt, Complete Computer Description, Design of Basic Computer, Design of Accumulator Unit.	05
3	**Micro Programmed Control:** Control Memory, Address Sequencing, Micro Program Example, Design of Control Unit.	03
4	**Central Processing Unit:** Introduction, General Register Organization, Stack Organization, Instruction Format, Addressing Modes, Data Transfer & Manipulation, Program Control, Reduced Instruction Set Computer (RISC).	05
5	**Pipeline and Vector Processing:** Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction, Pipeline, RISC Pipeline, Vector Processing, Array Processor.	04
6	**Input – Output Organization:** Input-Output Interface, Asynchronous Data Transfer, Modes Of Transfer, Priority Interrupt, DMA, Input-Output Processor (IOP), CPUIOP Communication, Serial Communication.	04
7	**Memory Organization:** Memory Sub System, Memory Hierarchy, Main Memory, Auxiliary Memory, Flash Memory, Associative Memory, Cache Memory, Virtual Memory, Memory Management Hardware.	05
8	**Microprocessor Architecture:** 8085 Architecture, Instruction Set, Instruction Types & Formats, Instruction Execution,	14

	Instruction Cycles, Different Types of Machine Cycles & Timing Diagram, 16-Bit Microprocessors, 8086 Architecture, Registers, Memory Segmentation & Addressing, 32-Bit/64-Bit Microprocessor Families.	

Practical content	
Experiments/Practical/Simulations would be carried out based on syllabus	
Text Books	
1	Computer System Architecture: By M. MorrisMano, Pearson Publication
2	Microprocessors and Interfacing: By D.V.Hall, Tata McGrawHill.
Reference Books	
1	Structured Computer Organization: By Tanenbaum, PHI Publication
2	Computer Organization and Architecture: By Stallings, Pearson Publication
3	The Intel Microprocessors: By B.B. Brey, Pearson Education.
ICT/MOOCs Reference	
1	https://www.geeksforgeeks.org/computer-organization-and-architecture-tutorials/
2	https://nptel.ac.in/courses/106/105/106105163/

Course Outcomes:

After successful completion of this course, student will be able to

1. Understand the organization of a Computer system.
2. Apply the knowledge of combinational and sequential logical circuits to design computer architecture.
3. Understand the input / output and Memory related concepts.
4. Apply the concepts of architecture of a processor and machine level programming.
5. Apply the digital principles in modelling and designing of computer based systems.
6. Write assembly language programming for computing and engineering practice.