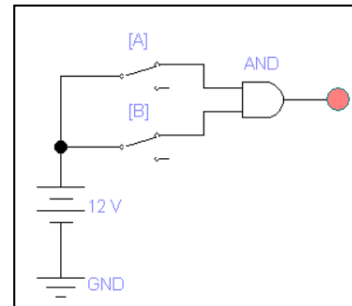
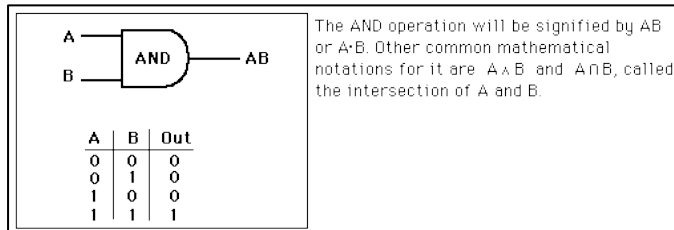
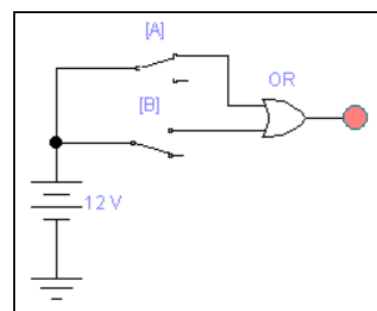
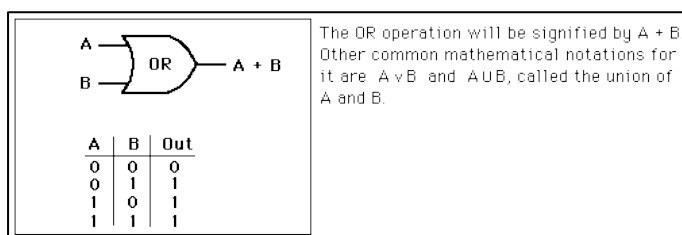


**Practical: 1****Aim: To Implement following logic gates Electronics Work Bench (EWB).****1. AND Gate**

The output is high only when both inputs A and B are high.

**Practical Figure:****2. OR Gate**

The output is high when either or both of inputs A or B is high. This is logically different from the exclusive OR.

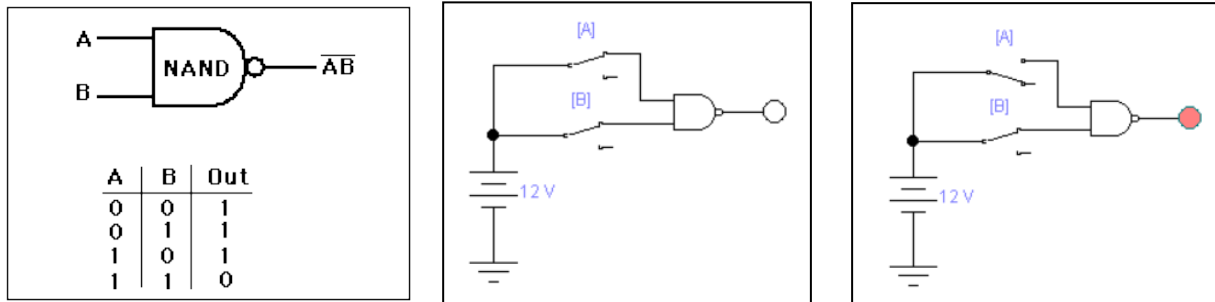
**Practical Figure:**

### 3. NAND Gate

The output is high when either of inputs A or B is high, or if neither is high. In other words, it is normally high, going low only if both A and B are high.

The NAND gate and the NOR gate can be said to be universal gates since combinations of them can be used to accomplish any of the basic operations and can thus produce an inverter, an OR gate or an AND gate. The non-inverting gates do not have this versatility since they can't produce an invert.

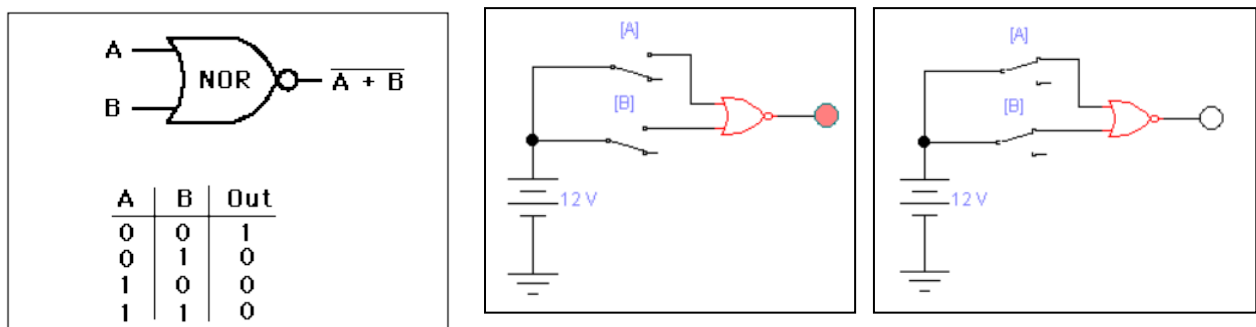
#### Practical Figure:



### 4. NOR Gate

The output is high only when neither A nor B is high. That is, it is normally high but any kind of non-zero input will take it low.

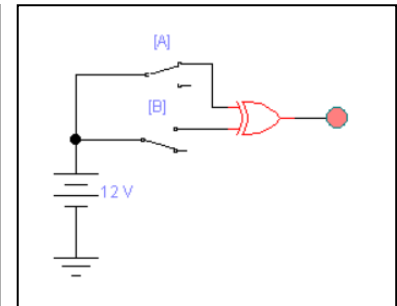
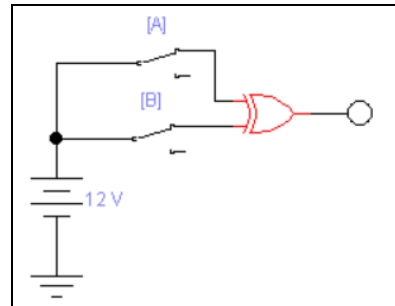
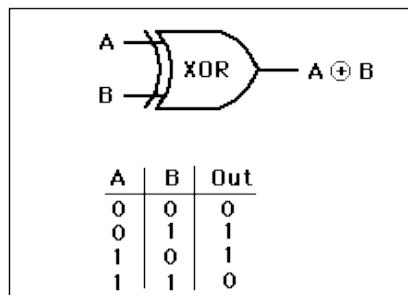
#### Practical Figure:



### 5. Exclusive OR Gate

The output is high when either of inputs A or B is high, but not if both A and B are high.

**Practical Figure:**

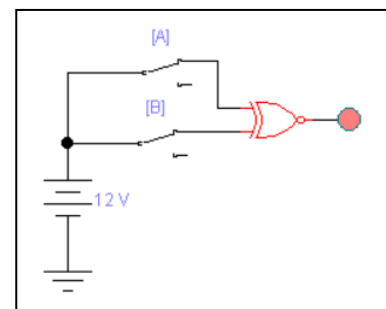
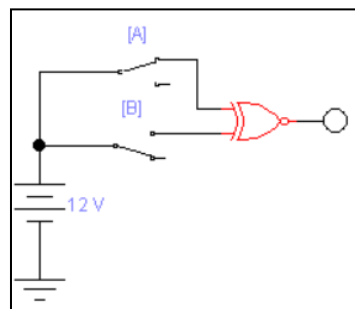
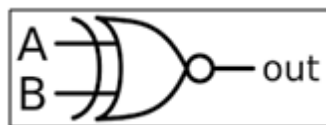


### 6. XNOR Gate

The output is high when both inputs A and B are high and when neither A nor B is high.

The NOR gate and the NAND gate can be said to be universal gates since combinations of them can be used to accomplish any of the basic operations and can thus produce an inverter, an OR gate or an AND gate. The non-inverting gates do not have this versatility since they can't produce an invert.

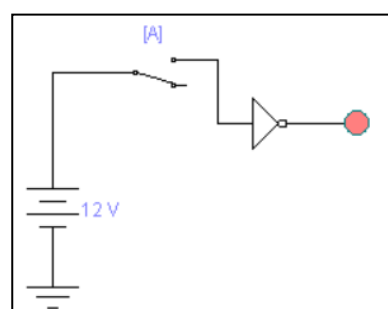
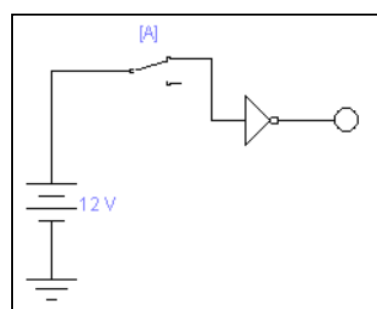
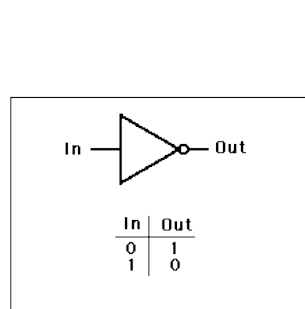
**Practical Figure:**



### 7. NOT gate (Inverting Buffer)

The inverting buffer is a single-input device which produces the state opposite the input. If the input is high, the output is low and vice versa. This device is commonly referred to as just an inverter or NOT gate.

**Practical Figure:**



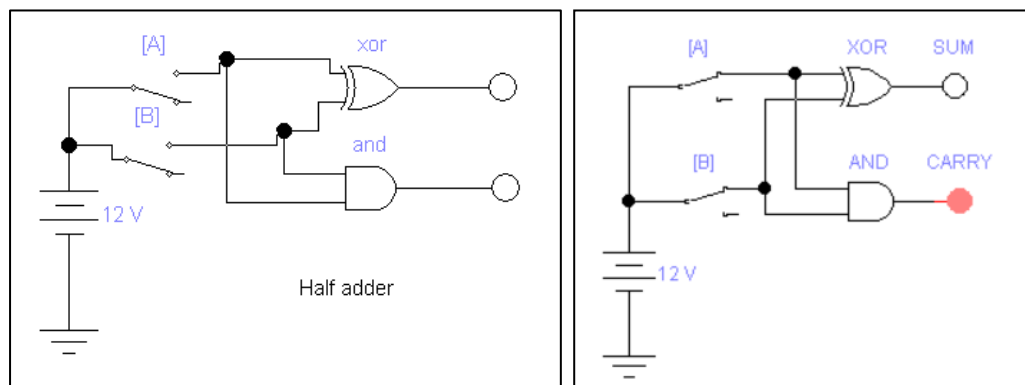
## 8. HALF ADDER

A Combinational circuit that perform the arithmetic addition of two bits is called half adder in figure we assign two symbol X and Y are two input variables and S(sum) and C(carry) are two output variables. Truth table for half adder is shown in fig.

Here  $S = X \oplus Y$  ||  $C = X \cdot Y$

X	Y	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

### Practical Figure:



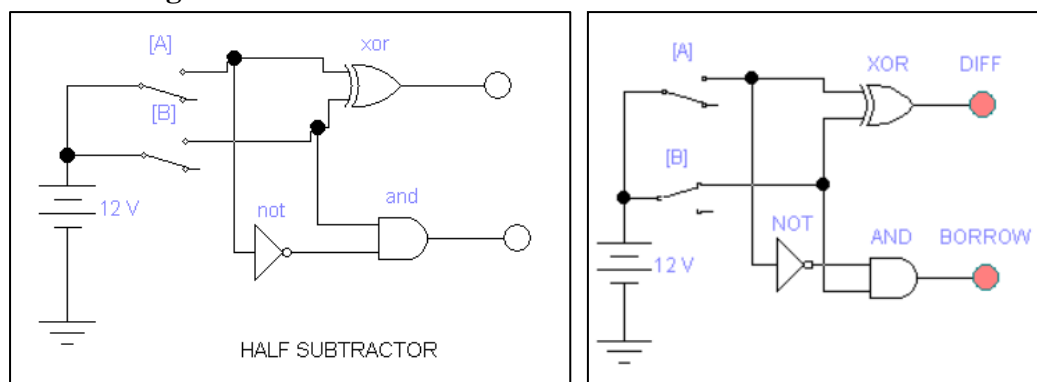
## 9. HALF SUBTRACTOR

A Combinational circuit that perform the arithmetic subtraction of two bits is called half subtractor in figure we assign two symbol X and Y are two input variables and Diff.(D) and Borrow(B) are two output variables. Truth table for half Subtractor is shown in fig.

Here  $D = X \oplus Y$  ||  $B = X \cdot Y$

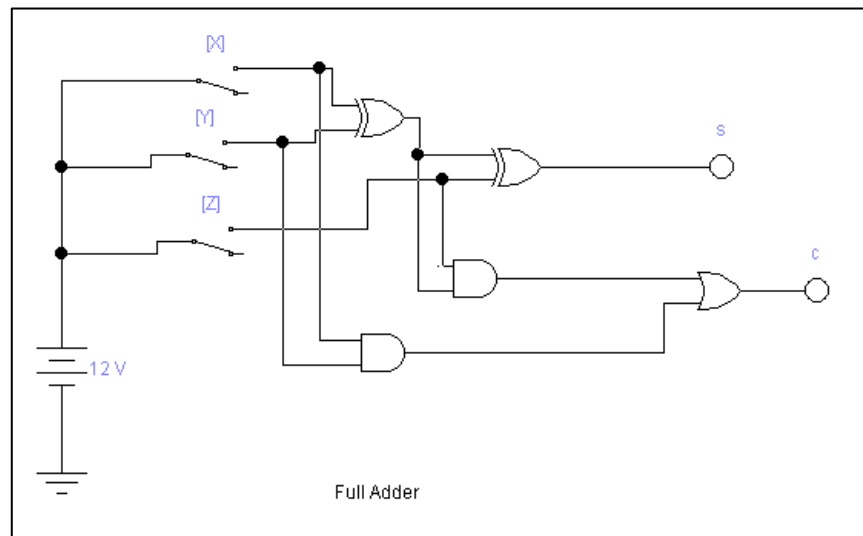
X	Y	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

### Practical Figure:



**10. Full Adder****Truth Table:**

x	y	z	c	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

**Practical Figure:**