Practical: 3
Aim: Implement common bus system of four 4-bit register using 2x4 decoder and three state buffer.

Theory:

A bus system can be constructed with three-state gates instead of multiplexers.
A three-state gate is a digital circuit that exhibits three states. Two of the states are signals equivalent to logic 1 and 0 as in a conventional gate. The third state is a high-impedance state. The high-impedance state behaves like an open circuit, which means that the output is disconnected and does not have logic significance. Three-state gates may perform any conventional logic, such as AND or NAND. However, the one most commonly used in the design of a bus system is the buffer gate. The graphic symbol of a three-state buffer gate is shown in below figure.

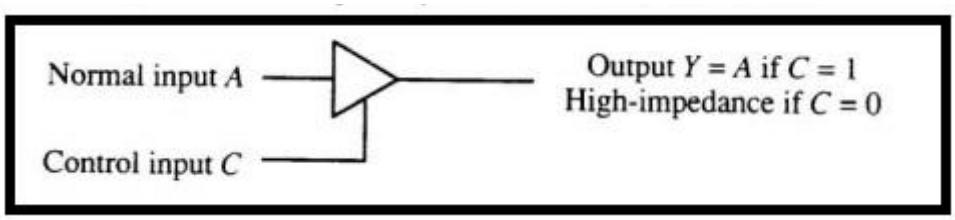
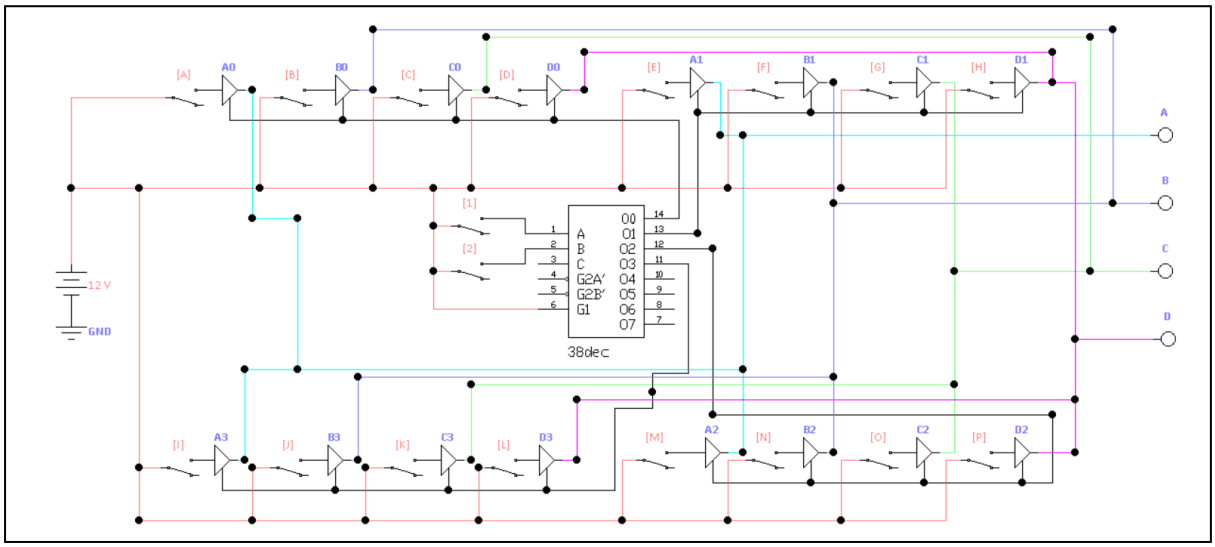


Figure.2 Three-state buffer gate

It is distinguished from a normal buffer by having both a normal input and a control input. The control input determines the output state. When the control input is equal to 1, the output is enabled and the gate behaves like any conventional buffer, with the output equal to the normal input. When the control input is0, the output is disabled and the gate goes to a high-impedance state, regardless of the value in the normal input. The high-impedance state of a three-state gate provides a special feature not available in other gates. Because of this feature, a large number of three-state gate outputs can be connected with wires to form a common bus line without endangering loading effects. The construction of a bus system with three-state buffers is demonstrated in Figure.1. The outputs of four buffers are connected together to form a single
bus line. (It must be realized that this type of connection cannot be done with gates that do not have three-state outputs.) The control inputs to the buffers determine which of the four normal inputs will communicate with the bus line. No more than one buffer may be in the active state at any given time. The connected buffers must be controlled so that only one three-state buffer has access to the bus line while all other buffers are maintained in a high impedance state.
One way to ensure that no more than one control input is active at any given time is to use a decoder, as shown in the diagram. When the enable input of the decoder is 0, all of its four outputs are 0, and the bus line is in a high-impedance state because all four buffers are disabled. When the enable input is active, one of the three-state buffers will be active, depending on the
binary value in the select inputs of the decoder. Careful investigation will reveal that Figure.1 is another way of constructing a 4 X 1 multiplexer since the circuit can replace the multiplexer in previous practical. To construct a common bus for four registers of n bits each using three-state buffers, we need n circuits with four buffers in each as shown in

Figure.1.Each group of four buffers receives one significant bit from the four registers, each common output produces one of the lines for the common bus for a total of n lines. Only one decoder is necessary to select between the four registers.

Circuit:



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