

SIMULATION SOLUTIONS FOR POWER GAN TECHNOLOGIES

by

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Dissertation submitted in fulfilment of the requirements

for the degree of

DOCTOR OF PHILOSOPHY

Department of Engineering
Faculty of Science
Macquarie University
Sydney, Australia

November 2020

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ABSTRACT

AlGaN/GaN HEMTs are now being realized as the future of semiconductor industry post Silicon. The RF modeling of III-V HEMTs in general has been a research topic since 1980's, however, to author's knowledge, High Voltage (HV) modeling of III-V power HEMTs has hitherto been a relatively uncharted territory. Although, various companies manufacturing these power III-V HEMTs do provide compact models with their PDKs for integrated devices or as standalone models for packaged (discrete) devices, they were found to be heavily influenced by the Low Voltage (LV) or RF modeling procedures that have been established over the years. The aim of this thesis is to venture into the compact modeling of both power (HV) and LV AlGaN/GaN HEMTs, at times using the excellence of methods and strategies that have been developed and frequently used for LV and RF compact modeling, i.e. not dropping them altogether, and then adding improvisations on top of it to produce a robust modeling approach towards power III-V HEMTs, with power AlGaN/GaN HEMTs as an example.

In particular, the work done in this thesis covers DC, pulsed DC, part RF (*S*-parameter), large-signal, statistical, trap, extreme environment (temperature and radiation) and p-GaN layer charge modeling of both HV/LV AlGaN/GaN HEMTs. This work can be treated either as a research output, guiding the design and modeling of newer AlGaN/GaN HV/LV HEMTs or as a general guiding principle for future HV/LV FET compact modeling, i.e., the models and methods developed in this work can be further applied to other HV devices such as LD-

MOS, HV MOSFETs and HV HEMTs/FETs present in various upcoming power semiconductor technologies such as SiC.

STATEMENT OF CANDIDATE

I certify that the work in this thesis has not previously been submitted for a degree nor has it been submitted as part of the requirements for a degree to any other university or institution other than Macquarie University.

I also certify that the thesis is an original piece of research and it has been written by me.

In addition, I certify that all information sources and literature used are indicated in the thesis.

Dhawal Dilip Mahajan

ACKNOWLEDGMENTS

Firstly, I would like to acknowledge the strong spiritual backing of my Guru, the 15th president of Ramakrishna Math and Ramakrishna Mission (RKM) - Swami Atmasthanandji. I am also grateful to the loving grace showered on me by Swami Sridharanandji, the current head of RKM's Sydney centre. I am eternally indebted to my parents Mr. Dilip and Mrs. Suhasini Mahajan for the upbringing that they gave me, which resulted in a scientific inclination of my mind. A special thanks goes to my aunt Mrs. Anjali Mahajan, who painted Fig. 10.1 which summarizes my work in a single allegorical picture.

The research work performed in this thesis has primarily been supported by the Australian Government's international Research Training Program (iRTP) Scholarship and thus I would like to thank the commonwealth of Australia and Macquarie university for awarding me this scholarship for a period of three years. Most importantly, my supervisor Prof. Sourabh Khandelwal has played a very significant role in my PhD - from regular "day to day" mentoring to ensuring that I give my best in each research output, he has done it all. He has always supported my aspirations and is a researcher par excellence. My teammates from the Emerging Devices And Circuits (EDAC) laboratory - Hossein Eslahi, Jason Hodges and Sayed Ali Albahrani too have played a key role in my research through their constant and untiring support. Special mention goes to Ali, with whom I have had rounds and rounds of tireless discussions and philosophical debates on physics and metaphysics in general and I must say that I have truly enjoyed

them! Ali has also been a mentor to me, given that he was a post-doc in our group and I was fresh to academia after a long hiatus of ten years in industry after my Master's degree.

Over the course of my PhD, I have published journal papers with three very prestigious groups working on AlGaN/GaN HEMTs:

1. Keysight's compact modeling team from USA and Japan, headed by Raj Sodhi. I would like to thank Raj for the funding and constant encouragement and support which resulted in the work described in chapters 2, 3 and 4. Additionally, I would like to thank Takashi Eguchi from Keysight Japan with whom I performed all the measurements for the Panasonic's power AlGaN/GaN HEMT - PGA26E19BA.
2. Stanford's XLab group headed by Prof. Debbie G. Senesky. I worked with her post-doc student Saleh Kargarazzi whose constant support resulted in the work on extreme temperature modeling which has been covered in chapt.8.
3. Fraunhofer IAF's Dr. Dirk Schwantuschke, with whom we were able to publish the work "Modeling of the Impact of the Substrate Voltage on the Capacitances of GaN-on-Si HEMTs" in *IEEE Transactions on Electron Devices*, which has not been included in this thesis.

I would like to acknowledge my wife Devika, whose loving and unshakable support during the entire three years of my PhD gave the moral boost required to carry through thick and thin of the research process. Last but not the least, I consider my son Vivaan, who was born during the second year of my PhD, as the best gift that I have received in my entire life hitherto.

*Dedicated at the holy feet of Shri Sarada Ma, the Divine Mother & Consort of
Shri Ramakrishna and Spiritual Mother of Swami Vivekananda*

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1

Introduction

“Knowledge is nothing but finding unity in the midst of diversity.”

– Swami Vivekananda

1.1 Knowledge And Models

HUMAN mind has been trying perpetually to accumulate knowledge ever since the dawn of civilization. From the esoteric theories of Aristotle to the most complex mathematical formulation of String theory, we have evolved our understanding and eventually our knowledge of the universe. Every pursuit of knowledge can be regarded as a combination of three fundamental aspects - first is observation or experimentation or imagination, i.e. any process by which we interact and perceive the surrounding world; the second aspect is the analysis or processing of the acquired perception or data from the first step using a set of axioms or a proposed theory; while the third aspect would be creation of a model that “stitches”, so to speak, the perception or data gathered in first step using the analysis devised in second step. Thus, the very nature of knowledge is that it is a set of all the different models painted by different scientific theories expounded till present. Thus,

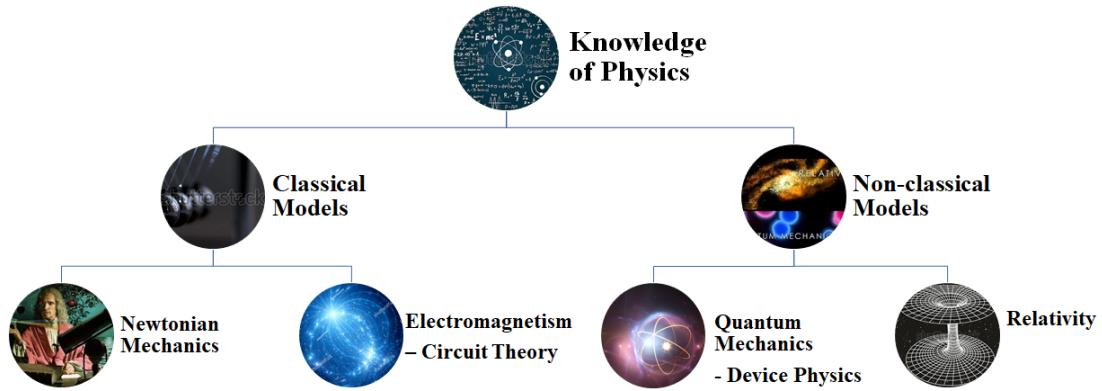


Figure 1.1: A chart depicting some of the models of physics, which themselves are well established & complete theories. Circuit theory and device physics are depicted as engineering models created out of classical electromagnetism and non-classical quantum mechanics respectively.

knowledge and models are intricately related, the later being a subset of the former.

Take, for example, the various established theories of physics, some of which are depicted in Fig. 1.1. Each of these theories can be interpreted as constructor of a model that is valid for certain scale (ex: microscopic vs macroscopic) or certain types of forces (gravitational, electromagnetic, weak and strong nuclear) etc. Another way of putting the same thing will be that each of these constructed models are valid for certain boundary conditions as defined by the problems which they ended up solving. For example, the theory of quantum mechanics paints a model that describes the behavior of electrons, atoms, molecules, but fails to explain the gravitation at cosmic scale, where we have to invoke another theory or model - theory of relativity. This is the reason why most of the physicists are pursuing a unified model of physics which will encompass all the current theories and will explain all the predictions and outcomes of various experiments, which the current theories explain with adequate precision.

Fortunately, most of the engineering problems do not require an entire theory to be constructed! It is sufficient to use established scientific theories (or the models that they have created) to come up with another subset of models, which can be called engineering

models, such as circuit theory and device physics (semiconductors, superconductors etc), derived from classical electromagnetism and non-classical quantum mechanics respectively as shown in Fig. 1.1. These engineering models are especially useful in designing practical systems, such as design of ICs/MMICs/PCBs for LNAs, PAs, mixers and plethora of mixed signal circuits for a mobile phone or a DC-DC converter used in a power electronic application. A typical circuit designer will use circuit theory model i.e. a combination of laws like KVL ($\oint_{line} \vec{E} \cdot d\vec{l} = 0$, for boundary condition of $\frac{\partial \vec{B}}{\partial dt} = 0$, i.e law of conservation of energy contained in an electric field) & KCL ($\sum_i \frac{dq_i}{dt} = 0$, for all i branches at a node, i.e. law of conservation of charge when applied to a node in a circuit) applied to a material system which can be approximated by lumped components like R's, L's, C's and active devices like FETs. For active devices like FETs in an IC/MMIC process, models created using semiconductor device physics are typically used. Semiconductor device physics, which is an established theory in itself, consists of different models created using various approximations by assuming ideal conditions, some involving quantum mechanics (such as Bloch's theorem which is used to solve the electron wave-function in a periodic potential which exists in a crystal lattice), others involving drift-diffusion transport, continuity equation, Poisson's equation etc, which have been taken out of electromagnetism. Thus, an engineering design involves usage of a tiny subset of engineering models, which themselves have been taken out of well established theories (see Fig. 1.1).

Once the paper design of a circuit is done, the next step will typically be circuit simulation using commercial/non-commercial IC design tools such as Cadence ADE, ADS, AWR etc. These tools use various types of circuit simulators such as Spectre, HSPICE etc that will perform various types of simulations such as DC, transient, ac, harmonic balance (hb) etc on the designed circuit using various compact models that have been created for a particular semiconductor Process Design Kit (PDK), which a designer chooses based on his/her needs. Next, the simulated circuit which meets the design IOS (Initial Objective

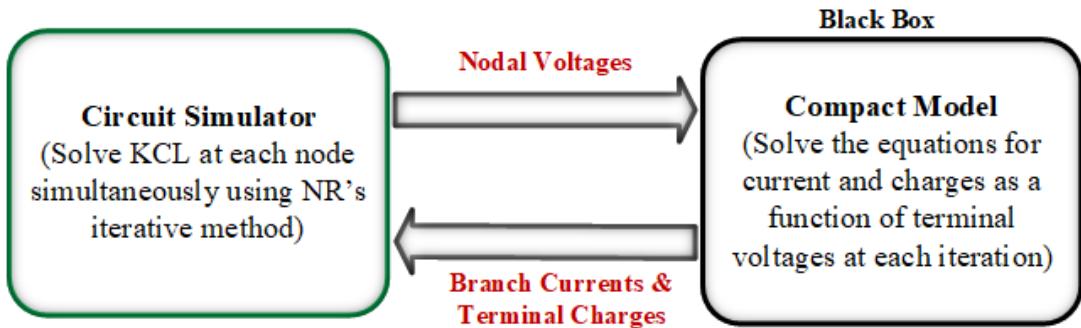


Figure 1.2: A figure depicting the relation between circuit simulator and a compact model, which is a ‘black box’ when seen from simulator’s point of view.

Specifications) is converted into a layout which is then verified for ERC (Electrical Rule Checks), DRC (Design Rule Checks), LVS (Layout Vs Schematic) & re-simulation using parasitic (back) extraction i.e. adding all the existing parasitic elements (usually R’s & C’s) from the cross-section as defined in a given IC/MMIC fabrication process. This (back) extracted parasitic circuit is added back to the main circuit and then the whole circuit is simulated and compared against the IOS. Furthermore, other types of simulations such as temperature sweep, corner and statistical simulations, noise simulation etc are optionally performed in order to check the robustness of the designed circuit. Finally, after successful verification of all the steps described above, the circuit is certified fit to be taped out - either in the given IC/MMIC fabrication process for integrated power devices or for a given PCB layout in case of discrete power devices. At this juncture, we will delve into the meaning of the term ‘compact models’, which will be the topic of next section.

1.2 Compact Models And Power Device Modeling

A compact model can be defined as a concise mathematical description of terminal characteristics (charges and their derivatives w.r.t time and bias) of a device as function of the input bias, temperature, geometry and process parameters. Compact models of FETs

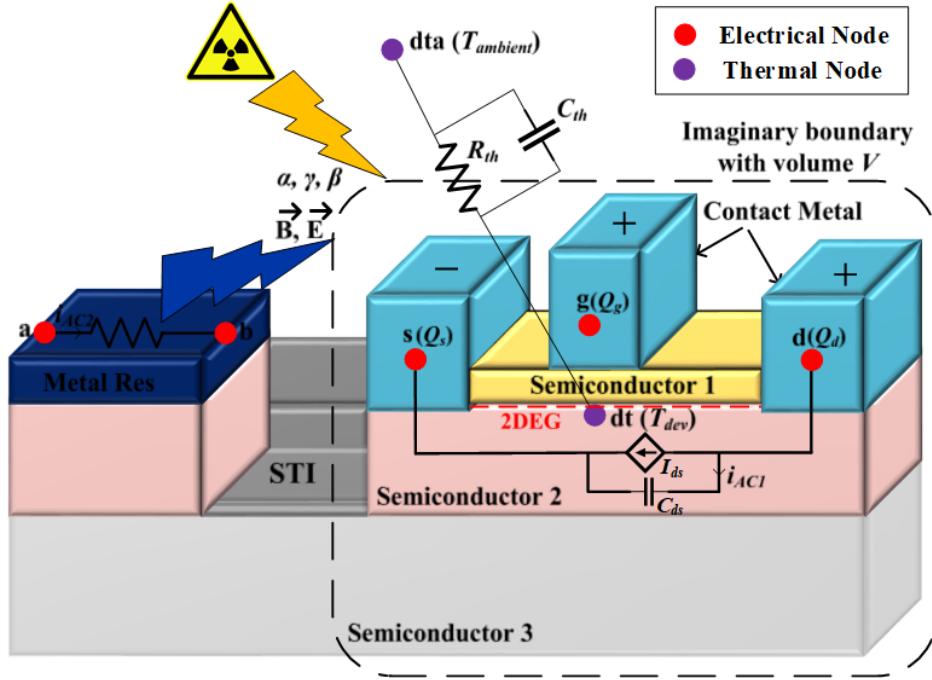


Figure 1.3: A 3D section of a general compound semiconductor process, with electrically & magnetically neutral imaginary boundary isolating the HFET (Hetero-structure Field-Effect Transistor) device from outer sources of various types of fields such as a AC conducting metal resistance in proximity, separated by STI (Shallow Trench Isolation) & radiation sources. Both the electromagnetic fields generated by the AC conducting metal resistance (EMI coupling fields) and various radiations that can cause secondary effects in the device such as impact ionization in the channel are assumed to have no effect on the operation of the device. Note that, except for the possible heat transfer between the two thermal nodes, one located in the channel (dt), while the other located in ambient (dta), through a parallel network of thermal resistance R_{th} (K/W) & thermal capacitance C_{th} (sW/K), the device is assumed to be perfectly isolated thermally. The only electric fields that can exist are internal to the device which are generated due to the applied DC/AC voltage/current sources and various internal potential drops such a surface potential which are not shown. A static channel current I_{ds} flows through 2DEG (2-Dimensional Electron Gas), with the relative polarity of voltages on the various nodes as shown, while a dynamic current branch can be defined for displacement current i_{AC1} through small-signal capacitance C_{ds} between nodes d & s as shown. The source and gate field plates which are an integral part of a power HFET because of their role in increasing the breakdown voltage (BV) of the device and reducing gate resistance and trapping effects respectively are not shown for brevity.

(Field Effect Transistors) are a further subset of engineering models, typically derived from the underlying semiconductor device physics, e.g. models such as BSIM, EKV & PSP [1–3], or in some cases created using empirical relations such as Angelov’s models for GaAs & GaN HEMTs [4–6], or still in some other cases created using look-up table based approach [7, 8]. The word ‘compact’ perhaps refers to the close packing of various formulations for various branch currents and terminal charges that a compact model, as a part of circuit simulator, endeavours to achieve (see Fig. 1.2). Almost all the compact models of FETs that have been developed till now [1–8] are primarily quasi-static, small-signal models in their basic formulation. Such formulation aims to model the output behavior as a response to the applied small-signal perturbation at the input (typically gate of a FET or base of a BJT), with assumptions that require the quiescent point, i.e. a single point DC/steady-state solution ($I_{ds(q)}$, $V_{gs(q)}$, $V_{ds(q)}$) of a given circuit, that is given by the intersection of I-V characteristics with the load line, doesn’t change with the variation of the input and output signals and that a non-linear device can be linearized around this quiescent point. Thus, these models aren’t necessarily formulated keeping in view the requirements of a power device, which usually experiences a large signal, quiescent bias changing, switching input such as a rectangular pulse with very high rise and fall times when used as a power electronic switching element, or a large signal sinusoidal input when used as an input/output matched amplifying element in a power amplifier, which is used as the final output stage in a RF block driving an antenna. In both the cases, the circuit doesn’t have a quiescent point, but a set of quiescent points, which defines a dynamic load line.

A quasi-static model doesn’t take into consideration the finite transit time TT (average time required for a charge carrier to travel from source to drain in FET or emitter to collector in a BJT). This results in the model not being able to predict the input-output phase relation, which can be important for many RF circuits that rely on the correct

relation of this phase, for an applied signal frequency greater than one over transit time ($f_i \geq \frac{1}{TT}$). Thus, quasi-static models are problematic for simulating long channel lengths (FET) or base widths (BJT) or at very high frequencies. This problem can be solved by solving for a bias dependent distributed R-C transmission line in the channel [9]. Some models like BSIM do have a non quasi-static model implemented based on Elmore equivalent RC circuit approximation to the distributed R-C network in the channel [9], but that model has been reported to have a lot of convergence issues [36]. In order to simulate a power semiconductor device, quasi-static effects might not be an issue because the highest reported switching frequencies that these circuits use (from few hundreds of KHz to few tens of MHz) are still way lower than those used in typical RF circuits (in GHz range), where non-quasi-static models might be required for some specific applications. The longer channel lengths in addition to source/drain access regions of these devices, too, do not seem to make any difference in simulation because of the lower switching frequencies which are way less than $\frac{1}{TT}$, i.e. the quasi-static assumption that the input signal is so slow that the channel charge follows it as if each instantaneous solution for channel current is a superposition of steady-state (DC) and dynamic (transient or $C \cdot \frac{dV}{dt}$ charging current) is valid. Thus, for power electronic circuit simulation, large-signal switching behavior must be captured using the quasi-static, small-signal compact model. In chapt.3, we have shown that a quasi-static, small-signal model can indeed capture the switching losses along-with transient wave-forms, provided that various non-linear OFF-state capacitances such as C_{oss} are modeled correctly.

In order to understand the role that compact models play in circuit design and how they work, we need to first take a look at how a circuit simulator works. A detailed explanation about the basic algorithms used in circuit simulation, along-with various steps to be followed while simulating power electronic circuits in Cadence environment are given in appendix. A. Fig. 1.2 depicts the nature of interaction between a circuit

simulator and a compact model, with later being a ‘black box’ for the former. This is because the simulator doesn’t have any direct access to the inner workings of a compact model except for the branch currents and the terminal charges and perhaps the rise in temperature due to self-heating, if a thermal node is defined in the model. On the other hand, we can access and use the simulator defined variables such as nominal temperature TNOM etc from the simulator and use it anywhere in the compact model.

The most important practical aspect, while implementing compact models, is the choice of coding language that one adopts. A collection of all the flavours of BSIM’s source code [10] could be the best example that illustrates this point. If you look at the source codes of BSIM3/4, then it is verily possible that you will be stuck up with a quagmire of different pieces of ‘*.c’ files, because these models have been written in C, which is a sequential language by design, i.e. code lines gets executed one by one, thus requiring the model developer to create numerous headers and sub-routines (functions) for various tasks such as explicit hand-coding of derivatives with respect to the system unknowns (generally node voltages, since according to Fig. 1.2, node voltages are the independent variables in KCL equations solved by a circuit simulator), which is a tedious and error-prone task, and further gel them together into one single cohesive model. On the other hand, if you take a look at the source code of a model such as BSIM-CMG or BSIM-SOI, you see only one ‘model_name.va’ file that contains all the code, containing approximately one tenth the number of lines that were used for coding BSIM3/4 in C. This is because Verilog-A, the analog only subset of Verilog-AMS [11], which is now a standard for writing compact models [12–14], allows a user to write his/her compact model in a truly compact way! Although, another viable option such as VHDL-AMS [15] is also available, but perhaps due to the overwhelming popularity of Verilog-A’s counterpart in digital circuit design in the commercial space, its closeness with ever popular C language and availability of compilers in many commercial circuit simulators such as Spectre, HSPICE, ADS etc, it

was Verilog-A that got finally adopted as a standard for compact modeling. The compact modeling specific constructs were added to Verilog-A in the year 2004 [14], which is the most probable reason why BSIM3/4, whose development dates back to 1990's and early 2000's, are coded in C. The downside of using Verilog-A over C is that in-spite of the compact code, the run times of Verilog-A coded compact models are at the best 5-20 % slower than the C coded models, thanks to the advances in the efficiency of Verilog-A compilers in both proprietary and commercial simulators [12].

The various features of a hardware description language (HDL) such as Verilog-A that allows us to construct these compact models are:

1. *Concurrency*: This is, perhaps the most important feature of a HDL that separates it from other programming languages, in that we don't need to worry about the fact that the hardware (circuit) that we want to represent in a code, is concurrent in nature, i.e. all of the following: application of stimuli in the form of voltage & current sources, transport of charge carriers across wires, passive and active devices occur simultaneously. This simultaneity is implemented in Verilog-A in the form non-blocking assignments, which can be identified by non-blocking assignment symbol '`<+`', which is also called as contribution operator. The other assignment operator, which is a blocking assignment, is sequential and is represented by '`=`' symbol. Whenever a compiler encounters the '`<+`' operator, it will evaluate the RHS but will not assign it to LHS immediately, that is to say the assignment execution will be 'scheduled' without blocking the execution of following statements, till all the inter-dependencies of inputs (signals such as voltages or currents) in the RHS get settled down to a stable value. Whereas, in case of sequential assignment '`=`', the RHS is assigned to LHS immediately, i.e. it doesn't allow the next line to get executed till the time it is executed completely and hence its alternative name - blocking assignment.

2. *Flexible & reliable coding using functions/macros and operators:* The codes written in C require the mathematical operators such as derivative ($\frac{d}{dx}$) to be hand coded for a given compact model. This is a highly error prone task. However, the whole idea of a HDL is to get rid of all these steps which are time consuming in addition to being unreliable in the first place. The availability of built-in functions for various tasks and of analog functions and macros makes the model code modular and reusable. Additionally, the analog functions and macros, when instantiated in the code, are concurrent blocks themselves, with internal sequential assignments that get executed one by one when a macro or function call is instantiated in the model code.

Finally, a discussion on compact models won't be complete without defining the various boundary conditions and assumptions, which form their problem definition. A detailed 3D section, explaining the problem definition of a HFET (Hetero-structure Field-Effect Transistor) device in a compound semiconductor process is shown in Fig. 1.3. The first step in defining a compact modeling problem for this device is the recognition that circuit simulators do not solve Maxwell's equations; they solve Kirchhoff's current law (KCL) with the assumption that all circuit components interact via perfectly conducting wires, with no fields internal to one component directly interacting with the fields internal to another component. If we apply Gauss's Law to electrically & magnetically neutral imaginary boundary (i.e. no surface charges or surface currents respectively) in Fig. 1.3, we get

$$\iint_{\vec{\mathbf{S}}} \vec{\mathbf{E}} \cdot d\vec{\mathbf{A}} = \iiint_V \frac{\rho}{\varepsilon} dV, \quad (1.1)$$

where $\vec{\mathbf{S}}$ is the closed surface encompassing a volume V , $\vec{\mathbf{E}}$ is electric field, ρ is the charge density per unit volume, which can vary with position within V , and ε is the permittivity. Because fields external to a device are assumed not to affect the internal state of a device, the integral on the left hand side of (1.1) is zero; therefore the right hand side must also

be zero. But, integrating the charge density on the right hand side gives the total charge within a region, therefore, from Fig. 1.3 we get

$$Q_D + Q_G + Q_S = 0, \quad (1.2)$$

where Q_D , Q_G & Q_S are the total charges associated with terminals d, g & s of the HFET respectively. Thus, the device as a whole behaves as a charge conserving node and electromagnetically neutral under our ideal assumptions. If we divide both the sides of (1.2) by cross-sectional area, then we get the charge neutrality expression for charge per unit areas as

$$Q_d + Q_g + Q_s = 0, \quad (1.3)$$

where the smaller subscripts are per area counterparts of various terminal charges. This charge conservation can be easily implemented in Verilog-A. Furthermore, we can define static branch currents such as channel current I_{ds} in Fig. 1.3 by using the contribution operator (' $I(d, s) < + f(\text{Bias}, T_{dev}, \text{Model parameters});$ ') in Verilog-A as explained earlier. The dynamic branch currents, which define the capacitances between two electrical nodes, are given by assigning the time derivative of the various terminal charges between appropriate nodes, e.g. ' $I(d, s) < + \text{ddt}(Q_d);$ ' will result in addition of a small-signal capacitance per unit area, C_{ds} , in between nodes d and s in Fig. 1.3. Other ways of coding the same capacitance between two nodes are ' $I(d, s) < + C \cdot \text{ddt}(V(d, s));$ ' & ' $I(d, s) < + \text{ddt}(C \cdot V(d, s));$ '. However these two methods are not recommended because for a non-linear capacitance ($C(V)$), the first formulation leads to a numerical drift over time in transient simulation, while the second one doesn't drift but predicts the amplitude wrong for both transient and ac simulations [12, 13]. A detailed description on how the nine non-reciprocal capacitances between three terminals d, g & s can be calculated is given in sub-section 2.2.6 of chapt.2.

The reason why we do not use voltage drop as a function of various currents while

defining a branch between two nodes is that, as already explained, circuit simulators are based on nodal analysis using node voltages as independent variables, due to which it makes sense to define various internal branches inside a compact model as voltage controlled current sources. Furthermore, the changes in currents between successive iterations during NR's (Newton Raphson's) iterative method in a typical circuit simulation can be orders of magnitude higher (e.g. from pA to mA the change in order is 9), while voltages change within one or two orders of magnitude, thus requiring less precision in terms of decimal places in representing these voltages in a computer system on which circuit simulation is run, which in turn favours formulating branch currents as a function of voltages.

Once a compact model's code is generated using the above approach and verified for convergence and robustness, next crucial step is either the process of model parameter extraction for device library generation in a PDK along with the process and technology files for integrated devices (see Fig. 10.2) or standalone device model library generation for discrete devices. Parameter extraction is a process by which a modeler extracts the coefficients or constants of an empirical or physical equation, depending upon the approach used, using various measurements performed on a Device Under Test (DUT). In order for the extracted parameters to be consistent, the measurements must have following qualities:

1. The measurement bias, temperature and environment should be applied to a DUT in such a manner so that except for the known electrical or thermal phenomenon, no outer source of electromagnetic or thermal or radiation sources (as shown in Fig. 1.3) can exist. For this reason, a fabricated wafer containing various test structures for compact modeling is kept inside an electromagnetically and thermally isolated and temperature controlled probe station for various types of measurements.
2. Especially for RF measurements such as *S*-parameter measurements performed on

wafer, the reference plane from where the S -parameters are measured might not coincide with the DUT plane because of the interconnecting CPWs (Co-Planer Wave-guide is a Ground - Signal - Ground micro-strip line connecting various active or passive devices in a RF IC). In such cases, additional open and short test structures must be incorporated, measured and then used to shift the reference plane to the DUT plane. This process of arriving at the measurement boundary condition closest to the intrinsic device is called as RF de-embedding.

3. In addition to the RF de-embedding due to interconnects or backend of a given semiconductor process, which was described in the last point, de-embedding can also be necessary in certain measurements where contact probe resistance of the external probes used to contact the device pads might affect the measured voltage across the device. This type of de-embedding is due to the contact voltages developed across the ‘probe - pad’ contacts when high currents pass through the power FET and is a very important aspect of measuring the power FETs because their ON-state resistances might be comparable to the contact probe resistances used in the measurements. This de-embedding of on resistance for power FETs on wafer can be achieved either by using specialized Kelvin test structures or by using VMUs (Voltage Measure Units) instead of SMUs (Source Measure Units) of a semiconductor parameter analyzer. The addition of packaging is in fact proven to add no significant resistance between the package leads and the die and hence typically requires de-embedding due to the source impedance of the testing equipment, which is generally taken care of by the firmware of such testing equipments.
4. The chosen bias and temperature for each measurement should be such that the device exists in a particular region of operation, where a limited set of model parameters can be extracted from the measured data. For example, in FET modeling,

a transfer characteristic ($I_{ds} - V_{gs}$) for $V_{ds} = V_{ds(lin)}$ can be used to extract the threshold voltage and mobility related parameters, while a transfer characteristic for $V_{ds} = V_{ds(sat)}$ can be used exclusively to extract model parameters related to shift in the threshold voltage due to DIBL (Drain Induced Barrier Lowering) in short channel FETs and saturation velocity.

5. Certain equipments such as C-V meters, parameter and network analyzers etc are required to be calibrated before any measurement can begin. A detailed information in their data-sheets generally documents these calibration details. A clean data can only be measured with carefully calibrated measurement equipments.
6. Parameter extraction should not begin before the data is carefully measured with calibrated equipments, de-embedded and classified as per the above criteria for all the specific regions of operation of the particular type of DUT (FET, BJT etc).

Furthermore, the ideal assumption of a perfectly isolated system as shown in Fig. 1.3 can be broken in case of following scenarios:

1. *Change in environmental conditions:* This happens when the normal operation of a DUT gets affected by the surrounding phenomenon such as a metal resistance in proximity to the DUT between nodes a & b, conducting a large time varying current i_{AC2} or the DUT is subjected to an intense source of radiation in applications such as space or nuclear plants as shown in Fig. 1.3. In such non-ideal cases, we can allow the external fields such as \vec{B} , \vec{E} (EMI fields) or one or more types of radiation such alpha (α) particles, gamma (γ) or beta (β) rays etc to interact with the device via the imaginary boundary as shown in Fig. 1.3. In such cases, a first order model can be created out of measurements of the degradation in device's performance when it is subjected to any of the non-idealities discussed above and then using model parameters that are most sensitive to those measurements to fit the measured data.

If the model parameters used are physically relevant, then a physical model of the phenomenon can be created. This can be seen in the modeling of degradation due to extreme temperature or radiation exposure to proton radiation in chapt.8, where it turns out that the acceptor type traps present in AlGaN/GaN HEMTs degrade the electron mobility and access carrier densities, when these devices are subjected to such extreme environment conditions.

2. *Modeling of known phenomenon involving the imaginary boundary in Fig. 1.3:* Another scenario is when there is a known interaction of the device with its surroundings, such as heat generation due to Joule heating and exchange of that heat between the channel of HFET and ambient occurring through the thermal network between thermal nodes dt and dta, containing thermal resistance R_{th} (K/W) & thermal capacitance C_{th} (sW/K) as shown in Fig. 1.3, which is the reason for self-heating in the device when the channel is conducting very high current (at high gate overdrive or $(V_{gs} - V_{th})$). Thus, thermal modeling becomes necessary when the heat generation and flow from the channel to the ambient through the thermal network can no longer be neglected. Note that if there is no self heating in the device, which can happen during pulsed DC measurements, where pulse ON time is much less than the thermal response time constant ($= R_{th}C_{th}$), then there won't be self-heating because the heat generated during the ON time of the pulse and the time scale for heat exchange are both not enough due to short pulse width. In such cases, the device can be considered to be perfectly isolated thermally and the thermal network in Fig. 1.3 is no longer needed in the model.

This completes the definition of compact modeling problem of HFETs. However, this definition comes with a caveat - we have defined this problem for an intrinsic device (considered in detail for power AlGaN/GaN HEMTs in chapters 2 & 3), i.e. we have neglected the electrode parasitics which can originate from the back-end of a semiconductor pro-

cess such as interconnects, vias, top level metalization or package level parasitics such as inductance, capacitance and resistance of bond wires & package leads. The modeling of these extrinsic parasitic elements for power AlGaN/GaN HEMTs is considered in chapt.4.

The problem definition of power device compact modeling needs some extra inputs in addition to the discussion above. A power device must model large-signal switching behaviour by using the same topology as a small-signal model, due to various reasons discussed earlier while explaining small-signal, quasi-static models. This can be achieved by using additional sub-circuit elements or model equations. Present thesis discusses these extra elements or model equations that are required to capture various effects that are specific to power AlGaN/GaN HEMTs (High Electron Mobility Transistor is an alias for HFET or MODFET).

1.3 Power GaN Technologies

Power electronics industry is currently in a state of evolution, with newer and better power semiconductor devices being invented and implemented in semiconductor foundries, for use in various established and upcoming technologies such as photo-voltaic and wind energy systems, electrical vehicles (EVs) and automobile power trains, smart power grids, wireless chargers and various carbon footprint reduction technologies such as power supply size reduction (e.g. Google's little box challenge for shrinking 2 KW sized inverter to a size of pizza box with resulting power density greater than 50 W/in³ [16]), DC-DC converter size reduction for PC/industrial power supplies etc. Some of the key enablers of the above technologies, that require better and robust power semiconductor devices than the present generation of devices, are 'beyond the Moore' technologies, so called because they don't have to scale their device feature lengths as aggressively as conventional Silicon technologies. Examples of 'beyond the Moore' technologies for power electronic applica-

Table 1.1: Table comparing some important material properties at room temperature of various contenders for High Power, High Frequency Power Electronic Applications

Material Property	Si	SiC	GaAs	GaN	High Value Enables
Dielectric Constant, ϵ_r	11.4	9.7	13.1	9.5	<i>High Gain but Lower Bandgap</i>
Bandgap, E_g (eV)	1.12	2.9	1.4	3.4	<i>High Power/Unit Width, High Temperature Operation</i>
Electron Mobility, μ_e (cm ² /V · s)	1300	260	5000	1500	<i>High Gain, Low R_{on}, Low Noise</i>
Electron Saturation Drift Velocity, v_{sat} ($\times 10^7$ (cm/s))	1	2	1	2.2	<i>High Frequency Switching</i>
Critical Electric Breakdown Field, E_c (KV/cm)	300	2500	400	3300	<i>High Voltage Operation, High Efficiency, Low R_{on}</i>
Thermal Conductivity, χ (W/cmK)	1.5	4.9	0.46	1.3	<i>High Temperature Operation via Better Thermal Management</i>
$BFOM = \epsilon_r \epsilon_0 \mu_e E_c^3$	1	98.48	10.48	1279.81	<i>Baliga's FOM for Power Devices Normalized to Silicon's value</i>

tions are compound semiconductor processes such as GaAs, GaN and SiC. Table. 1.1 shows a comparison of different semiconductor materials starting from the conventional and industry favoured material - Silicon (Si), which has enabled the Moore's law of doubling the number of transistors for a given size of die approximately every two years, with wide band gap compound semiconductor materials such as SiC (Silicon Carbide) and III-V compounds such as GaAs (Gallium Arsenide) and GaN (Gallium Nitride). The table clearly highlights the advantage of wide band gap compound semiconductors for high voltage applications because of their high critical breakdown field (E_c) which is due to their wide band gap. Furthermore, the ideal specific on resistance of a drift region

$(R_{\text{on,sp}})$ in a power FET with breakdown voltage BV is given by [17]

$$R_{\text{on,sp}} = \frac{4\text{BV}^2}{\varepsilon_r \varepsilon_0 \mu_e E_c^3} \quad [\Omega \text{ cm}^2], \quad (1.4)$$

where ε_r is the relative permittivity of the drift region and μ_e is the electron mobility. (1.4) implies that greater the critical electric field and/or mobility, lower is the on resistance and hence lesser the ON-state conduction losses in a switching transistor. The improvement in $R_{\text{on,sp}}$ for GaAs in comparison with Silicon is largely due to its much greater mobility for electrons, while the improvement in $R_{\text{on,sp}}$ for SiC and GaN in comparison with Silicon is largely due to their much larger critical electric field for breakdown. Thus, the factor in the denominator in (1.4) - $(\varepsilon_r \varepsilon_0 \mu_e E_c^3)$ is called as Baliga's figure of merit for power devices, whose values for the different compound semiconductors normalized to Silicon are given in Table. 1.1. The values establish GaN as the clear winner with its **BFOM** almost 13 times that of the nearest competitor - SiC.

The high switching frequency is possible in SiC and GaN, because of high saturation velocities, which are almost twice that of Silicon, and high mobilities in case of GaAs and GaN. This is because higher values of both saturation velocity and mobility increase the current carrying capacity of a FET, which in turn decreases the average transit time of the device ($TT = \frac{|Q_{inv}|}{I_{ds}}$ for DC operation in transistor and $> \frac{L}{v_{sat}}$ for a transistor in velocity saturation [52]).

High temperature operation is enabled by a high value of band gap [18], due to which the intrinsic carrier concentration (n_i in $1/\text{cm}^3$) is lower in wide band gap devices, i.e.

$$n_i = \sqrt{N_c N_v} e^{-\frac{E_g}{2kT_{dev}}}, \quad (1.5)$$

where is T_{dev} the device temperature (in Kelvin), k is the Boltzmann constant (8.62×10^{-5} eV/K), E_g is the energy band gap of the semiconductor measured in electron-volts, and N_c & N_v ($1/\text{cm}^3$) are the effective electron and hole density of states for the semiconductor respectively. E_g , N_c & N_v are fundamental crystal properties that have

substantially less temperature dependence compared to the explicit temperature exponential ($e^{-\frac{E_g}{2kT_{dev}}}$) term of (1.5). At room temperature, the n_i of Silicon is around 10^{10} 1/cm^3 , which is negligible compared to the 10^{14} to 10^{17} 1/cm^3 doping levels in the nwell-s/pwells fabricated on Silicon devices. However, as the ambient temperature is increased well beyond 300°C , there can be as many or more intrinsic carriers present than dopant carriers in a given Silicon device. Thus, the electrical conductivity of lighter doped regions of Silicon devices become undesirably influenced by intrinsic carriers instead of the designed doping needed for proper electrical operation. Thus, the maximum limit for Silicon based devices (MOSFET's) from (1.5) is around 300°C with the use of SOI (Silicon On Insulator) technology, which reduces the junction leakage by a factor of 100 when compared to MOSFET's fabricated in bulk technologies. It can be easily verified that SiC and GaN have much lower intrinsic carrier concentrations than Silicon and, thus, do not run into intrinsic carrier conductivity difficulties until much higher temperatures, beyond 600°C (from (1.5)). Furthermore, the inherent ability of wide band gap semiconductor junctions to properly rectify with low reverse leakage (which is again possible primarily due to low n_i) at junction temperatures as high as 600°C enables power-device operation at higher ambient temperatures. Thus, a lower intrinsic carrier concentration and subsequently lower junction leakage currents enable SiC and GaN devices to operate effectively at high temperatures. We have modeled the physics of high temperature operation in AlGaN/GaN HEMTs upto 500°C in chapt.8.

The first large area GaN grown epitaxially on sapphire substrate was achieved in 1968 by using Hydride Vapour Phase Epitaxy (HVPE) [19, 20]. It took more than two decades after this initial success to fabricate a structure close to FET, when in 1991 Khan et al. reported the first evidence of two-dimensional electron gas (2DEG) formation at an AlGaN/GaN hetero-junction grown by metal organic chemical vapour deposition (MOCVD) on sapphire [21]. The first GaN metal semiconductor field-effect transistor

(MESFET) and HFET/HEMT grown by MOCVD on sapphire substrates were reported in 1993 and 1994, respectively by the same team [22, 23].

Since most of the current IC industry is based on Silicon as the first choice for substrate or starting layer because of low cost and better quality, HEMTs grown on Silicon substrates was a technological challenge due to huge crystal mismatch between Si and GaN layers. This was overcome in the year 2000, when Kaiser et al. [24] successfully fabricated AlGaN/GaN HEMTs on Si(111) substrate by using MOCVD. Subsequent developments in HEMT technology have gone into making the normally ON HEMT (depletion type or d-mode) to normally OFF (enhancement type or e-mode). Gate recess technique [25], treatment by fluorine ion implantation in the AlGaN layer [26] and additional Mg doped p-GaN layer between the metal and AlGaN layer in a technique pioneered by Panasonic [27, 28] are some of the successfully explored techniques in order to make e-mode HEMTs. We have modeled the charge characteristics of p-GaN HEMT devices and its impact on switching characteristics of power p-GaN HEMTs in chapt.9.

1.4 Thesis Organization And Contribution

This ‘thesis by publication’ is organized into ten chapters. The first chapter gives introduction to the theme of this thesis which is compact modeling of power (HV) AlGaN/GaN HEMTs (chapters 2, 3, 4, 5, 6, 9), while the remaining chapters (7 & 8) focus on compact modeling of both LV and HV AlGaN/GaN HEMTs. Following is a synopsis of remaining nine chapters (please note that my supervisor’s role in all the projects included in these chapters has been that of a chief mentor and overall coordinator):

- Chapters 2, 3 and 4 describe a new model for packaged or discrete power AlGaN/-GaN HEMTs, which has been used to model the measured I-V, C-V and OFF-state S-parameter data in order to extract the model parameters of both - intrinsic and

extrinsic components of the overall device model. Chapt.2, in particular, describes the reformulation of various modeling equations of ASM-GaN model in order to model the intrinsic device of a power HEMT. Chapt.3 proposes an extraction flow for the intrinsic model described in chapt.2 and performs such extraction on Panasonic's packaged power HEMT - PGA26E19BA as an example. Furthermore, it gives a circuit design strategy that can be used for designing a switching converter circuit using the model card generated after extracting the intrinsic device. This model card is still not perfect because it doesn't include the effects of the package parasitics and hence chapt.4 gives a package parasitic extraction strategy with the underlying rationale behind it, by using OFF-state *S*-parameter measurements i.e. from Cold-FET measurements. The above three chapters thus complete a major portion of the work done on power AlGaN/GaN HEMT modeling. The entire work for these three chapters was conceptualized, measured (with creation of relevant ICCAP setups), coded (created a completely new Verilog-A code - ‘asmhemt_power.va’ of ASM-GaN, which can be downloaded from [76]), analyzed and eventually published as a journal paper in *IEEE Transactions on Power Electronics* titled “Physics-Oriented Device Model for Packaged GaN Devices”, with myself as the first author. Additionally, an international conference paper in *2018 Australasian Universities Power Engineering Conference (AUPEC)* titled “A Study of Hard Switching Characteristics of GaN-based DC-DC Boost Power Converter using ASM-GaN Compact Model” was published with myself as the first author.

- Chapt.5 presents a detailed analysis of large-signal Sawyer-Tower measurements on a power GaN HEMT device in OFF-state. The measurements show hysteresis which results in an energy loss in the range of sub- μ J's. We model this important phenomenon in this chapter using a previously calibrated model of the same device
 - Panasonic's PGA26E19BA, whose model parameters are extracted in chapters 3

and 4. We propose two models, one with linear Effective Series Resistance (ESR) and another using non-linear ESR (*NLESR*). It is found that to model the non-linear profile of hysteretic curve from Sawyer-Tower measurements, non-linear ESR and output capacitance are needed. The similarities and differences between these two models have been explained in detail. While linear ESR is shown to be a simple model for modeling the hysteretic losses, non-linear ESR and output capacitance model the dynamics of charging and discharging process more accurately. The work done in this chapter has been entirely planned, coded, executed, analyzed and submitted to *Solid State Electronics* journal with title “Analysis and modeling of OFF-state hysteretic losses in GaN power HEMTs”, with myself as the first author.

- In chapt.6, we have used electrical specifications from the data-sheet of a commercially available GaN HEMT power device (Panasonic’s PGA26E19BA) and its well calibrated physical model derived from chapters 3 and 4 as a starting point to arrive at corner and statistical models of that device using Backward Propagation of Variance (BPV). Both DC (V_{th} , $R_{DS(on)}$) and AC (C_{iss} , C_{oss} , C_{rss} & R_G) electrical specifications are used to derive the models. Furthermore, the generated statistical model is used to perform Monte Carlo simulations for the gate charge and switching transients in order to determine the distribution of circuit level electrical specifications from the underlying variations in the statistical model. All of the above work has been envisaged, investigated and simulated by me and furthermore accepted by the conference *2020 Power Electronics Drives and Energy System (PEDES)*, with paper’s title “Statistical Modeling of GaN Power Devices with ASM-GaN Model”, with myself as the first author.
- Chapt.7 combines the ASM-GaN model with a Shockley-Reed-Hall based trap model, yielding a comprehensive FET model for GaN HEMTs which can accurately model

GaN devices exhibiting trapping-related dispersion effects. Modeling of such effects are important because the DC characteristics of these devices are not representative of high-frequency operation due to trapping effects. Measurement results of the DC and pulsed output and transfer characteristics of a commercially available GaN HEMT are presented, trapping in the device is modeled, and excellent fit to the measured data is shown. This chapter presents an accurate model of trapping which is validated for eight different quiescent bias points of pulse measurements, with quiescent drain voltage ranging from 5 V to 20 V and quiescent gate voltage ranging from -2.8 V to -3.8 V, and a large range of gate and drain voltages to which the device was pulsed in the pulse measurements and at which the device was measured in the DC measurements, with gate voltage ranging from -4 V to 0.4 V and drain voltage ranging from 0 V to 40 V. The chapter also presents high frequency (10 GHz) large-signal RF validation of the model for optimal complex load condition. The above work was implemented, simulated, verified and analyzed by me along-with my colleague Ali, with a resulting invited journal paper in *IEEE Transactions on Electron Devices* titled “ASM GaN: Industry Standard Model for GaN RF and Power Devices—Part-II: Modeling of Charge Trapping”, with Ali as the first author and myself as second author.

- Chapt.8 applies the trapping model developed and implemented in Chapt.7 and further enhances it to model GaN HEMTs at extreme temperature conditions. In particular, the temperature dependence of the trapping behavior has been taken into account and a simplifying approximation in the temperature modeling of the saturation voltage and the eventual effective mobility calculation due to lateral electric field in the ASM-GaN model has been relaxed. The enhanced temperature model has been validated by comparing the simulation results of the model with the DC I-V measurement results of a GaN HEMT fabricated at XLab, Stanford, measured

with chuck temperatures ranging from 22 °C to 500 °C. A detailed description of the modeling approach is presented. Furthermore, two different AlGaN/GaN HEMTs subjected to proton radiation with varying doses are modeled for their degradation using ASM-GaN with the same modeling strategy (i.e. by varying the same model parameters) that was used for modeling extreme temperature conditions. Thus, the above formulations of ASM-GaN compact model, based on same set of model parameters, can be used to simulate circuits designed for extreme environments. A part of the work done in this chapter on extreme temperature modeling was done in collaboration with Stanford’s XLab group with myself contributing to the data-sorting, coding into ASM-GaN using the trap model developed in Chapt.7 and various simulations to extract the model parameters. This work resulted in a journal publication in *IEEE Transactions on Electron Devices* titled “Extreme Temperature Modeling of AlGaN/GaN HEMTs” with me and Ali as equal contribution authors. The remaining part of the work on degradation modeling of AlGaN/GaN HEMTs due to proton radiation exposure was envisaged, executed, simulated and published with myself as the first author in the international conference *2018 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)* with the paper’s title “Robust Circuit Model for GaN-Based Radiation-Hard Electronics”.

- Enhancement type p-GaN HEMT devices are desirable in power converter circuits for a fail-safe operation. The gate capacitance of these devices decreases for higher gate bias due to junction capacitance of the Schottky metal/p-GaN junction. It is important to capture this effect in simulation model. To this end, for the first time, in chapt.9, we present a depletion approximation based analytical model which effectively models this effect in the device. Using device electrostatics at the p-GaN/AlGaN junction in conjunction with physics-based core of ASM-GaN, we model the effect of doping in p-GaN layer. Furthermore, we use the developed

model to study the effects of the doped p-GaN layer on the performance of the switching characteristics of enhancement mode (e-mode) power GaN devices. The work done in this chapter is based on derivation of an equation for V_{gseff} based on the electrostatics of the problem. The derivation, identification and collection of the required data, implementation in ASM-GaN's Verilog-A code and all the simulations were performed by me, resulting in a conference paper titled "Impact of p-GaN layer Doping on Switching Performance of Enhancement Mode GaN Devices," in the prestigious conference on power electronics - *IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Padua, 2018.

- Finally, chapt.10 summarizes the work and talks about future challenges in the area of modeling both power (HV) and LV AlGaN/GaN HEMTs.
- Appendix. A gives various tips for simulating power electronic circuits, which have been derived from personal experience of the author, while simulating various circuits/setups present in this thesis.
- Appendix. B gives a detailed model card that has been used to simulate various kinds of circuits/setups in this thesis with Panasonic's power AlGaN/GaN e-mode HEMT - PGA26E19BA.
- Appendix. C contains Curriculum Vitae (CV) of the author.
- Appendix. D lists all the publications - journal and conference proceedings, that the author has published during his tenure as a PhD scholar at the engineering department of Macquarie university. The current thesis is based on these publications.

1.5 Chapter Structure

The chapters of this thesis are structured as follows. The first section of any chapter will introduce the main topic with a detailed literature survey, giving an idea of the problem to be solved, showing comparison with previous literature and proposal of an innovative solution to the problem definition which can be inferred from the discussion. This will be generally followed by a model description section or section on the proposed solution or the method of data collection for the given problem. Next section will be on the results and the ensuing discussion on various implications of those results. The final section will either conclude the topic with a brief discussion or summary of the results or will point to the next chapter which might continue on the work, with the current chapter's work as its foundation.

2

Modeling Of Power AlGaN/GaN HEMTs: Intrinsic Device

“In our description of nature the purpose is not to disclose the real essence of the phenomena but only to track down, as far as possible, relations between the manifold aspects of our experience.”

– Niels Bohr

2.1 Introduction

Commercial power AlGaN/GaN HEMT transistors are emerging as very promising devices for various power electronic applications, such as high switching frequency DC-DC power converters. Their key advantages include higher breakdown voltage, low on resistance, and in-turn low switching losses [29–33]. These devices have a favorable Baliga’s figure of merit because of the exceptionally high critical electric field of GaN [34]. Accurate and fast circuit design using such devices will require reliable circuit simulations using extracted compact models of these devices.

There are different types of compact models. Empirical or measurement-based compact models [35] directly make use of the measured data for modeling a device. Physics-based compact models [36–39] take information about the device process, geometry and derive their formulations from the underlying semiconductor physics. Both approaches have some pros and cons. Empirical models are easy to create but lose meaning when simulating the device under conditions that are outside of the measurements. Physics-based models are better in this regard but these models need information about device features which may not always be available.

Another approach to model the devices is to use Technology Computer Aided Design (TCAD) tools. These tools use Finite Element Method (FEM) to solve the electromagnetic (EM) equations on top of basic semiconductor physics for various regions of a given cross-section of device [40–42]. This approach is used in semiconductor foundries for modeling and designing new devices for a given process flow or for predicting the performance of a device by generating I-V and C-V characteristics for that device.

Industry standard physics-based compact models for MOSFETs [36–38] and GaN HFETs such as ASM-GaN [43–47], MVSG [48] and TCAD based models [40–42] need process parameters and detailed device dimensions as inputs. These details are usually not available to general users. This necessitates the need for new modeling formulation which preserves the advantages of a physics-based compact model but does not require process and device geometry details as inputs. Furthermore, the parameters of the model should be such that they can be extracted from a finite set of device measurements. We present such a new hybrid model which has been developed from the ASM-GaN compact model by reformulating this model to have process and geometry independent model parameters. New model equations still have some parameters directly related to physical effects and others which can be extracted from measurements.

2.2 Model Development Of Intrinsic Device

For modeling the overall packaged power device, we divided the problem into two parts, one corresponding to modeling of intrinsic device and other modeling of lumped (not distributed because we are still in a relatively low frequency range, where the minimum feature size in length is still very less than $\lambda/10$ of the applied signal) parasitic network around this intrinsic device, whose origin can be traced to the encapsulating package leads, bond wires, pads on the die etc. We will discuss the modeling of this parasitic network using Cold-FET technique in chapt.4. Following sub-sections describe the intrinsic FET modeling of a given packaged power device in detail. It must be noted that the model parameters of ASM-GaN other than the ones replaced in the following sub-sections have been kept the same and have the same implementation & interpretation in the new model.

2.2.1 2DEG Electron Density Model

In order to model the intrinsic HEMT device, we have to first consider the 2DEG (two Dimensional Electron Gas) formed at the $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ hetero-junction (without any source/drain structure). For such a material structure, Fig. 2.1 shows the band diagram [49] for gate voltage equal to zero with substrate grounded, so that the electron Fermi level E_f is above both the first and second energy sub-bands E_0 and E_1 of the quantum well formed in the conduction band at the hetero-junction. An analytical solution for this quantum well using triangular approximation with two sub-bands by solving for the coupled Poisson's and Schrödinger's equations, along-with Fermi-Dirac statistics has been given in [50, 51]. The analytical solution results in following transcendental

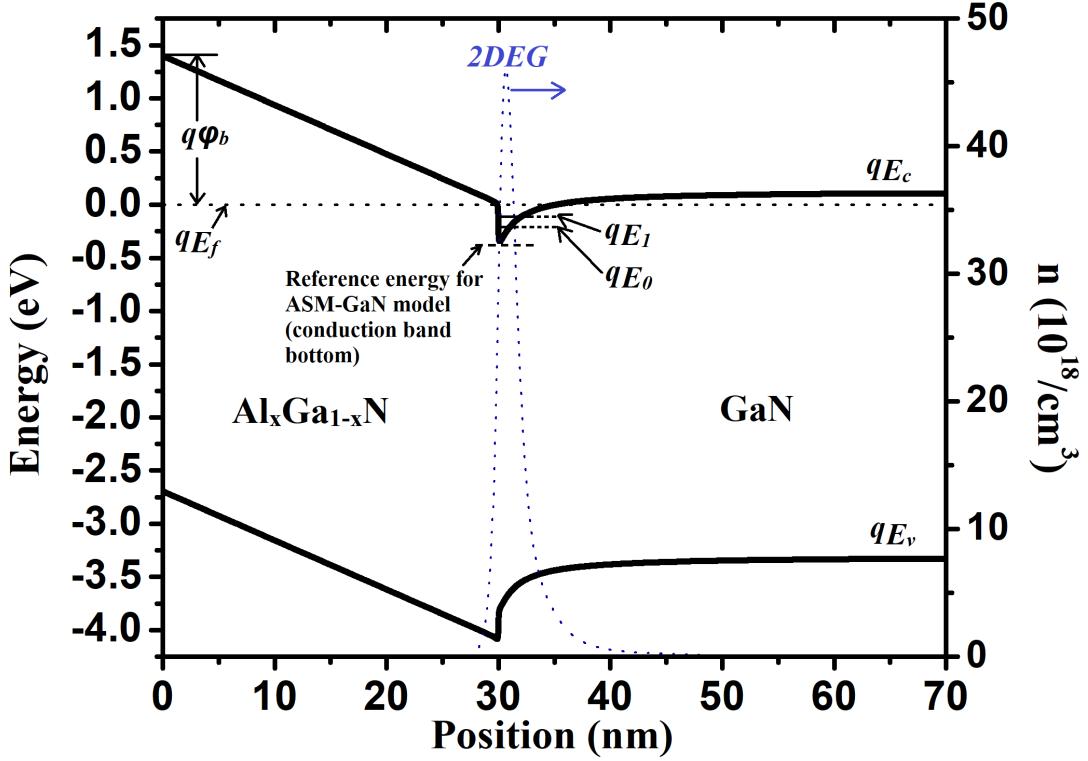


Figure 2.1: Band diagram of an AlGaN/GaN hetero-junction, for zero gate voltage created by solving Poisson's and Schrödinger's equations with electron Fermi level E_f as a reference. The tool used is nextnano*. The value of Al molar fraction x was taken as 0.3 for the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer. The thickness and Schottky barrier height at position = 0 of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ layer were taken as 30 nm and 1.4 eV respectively. The sub-band energy levels E_0 and E_1 in the quantum well are approximately shown. The final 2DEG density calculated in simulation is $8.39 \times 10^{12} \frac{1}{\text{cm}^2}$.

equations

$$n_s = \frac{DkT}{q} \left\{ \ln \left[\exp \left(\frac{q(E_f - E_0)}{kT} \right) + 1 \right] + \ln \left[\exp \left(\frac{q(E_f - E_1)}{kT} \right) + 1 \right] \right\}, \quad (2.1)$$

$$E_0 = \gamma_0 n_s^{2/3} \quad \& \quad E_1 = \gamma_1 n_s^{2/3}, \quad (2.2)$$

where D is the two-dimensional density of states in the quantum well, kT/q is the thermal-voltage, γ_0 and γ_1 are constants determined from cyclotron resonance experiments [51]. Furthermore, the charge control equation, which is essentially capacitive coupling from

*<https://www.nextnano.com/index.php>

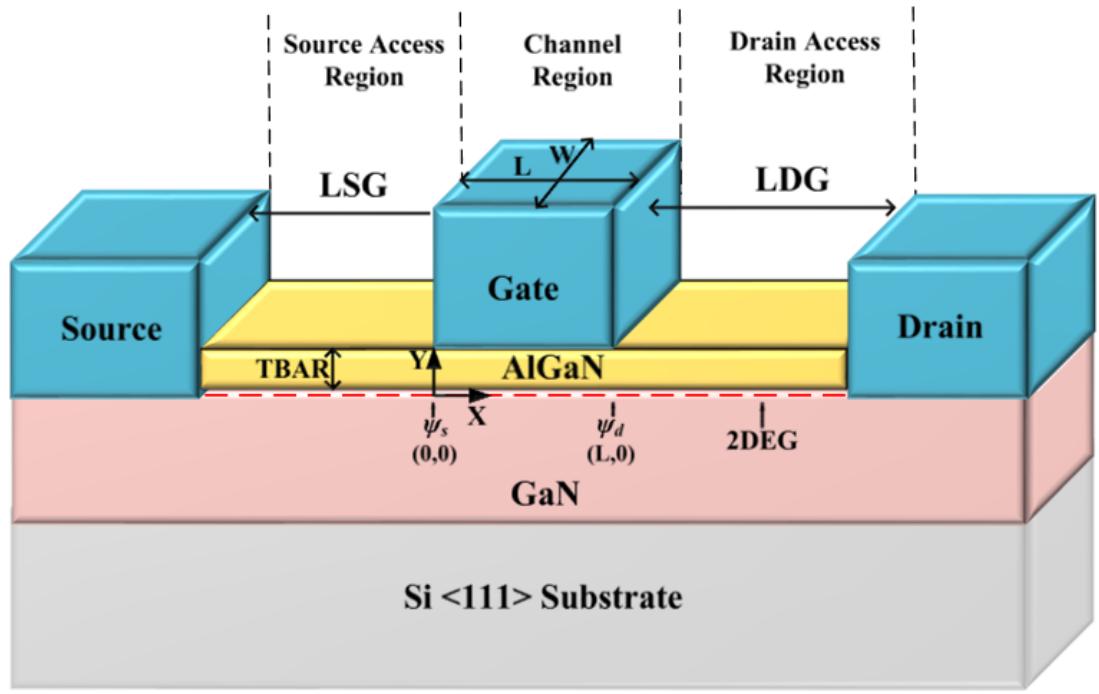


Figure 2.2: A typical 3D drawing of an AlGaN/GaN HEMT device on Si substrate shown without field plates, with various geometry & process parameters, 2DEG, channel region, source/drain access regions & reference X-Y axes for the purpose of analysis shown.

2DEG to gate through AlGaN dielectric layer with principle of potential balance (chapt.2 pg. 73 of [52]) applied to the gate - Al_xGa_{1-x}N - GaN loop ($V_g - V_{off} - E_f$) is

$$n_s = \frac{\epsilon_{\text{AlGaN}}}{qd} (V_g - V_{off} - E_f), \quad (2.3)$$

where ϵ_{AlGaN} and d are the dielectric permittivity and thickness of the AlGaN barrier layer respectively, V_g is the applied gate-voltage, V_{off} is the cut-off voltage. The ASM-GaN model makes all the variables in (2.3) as model parameters, viz. EPSILON (ϵ_{AlGaN}), TBAR (d) and VOFF (V_{off} is evaluated by subtracting the DIBL, trapping and temperature terms from the long channel model parameter VOFF). Furthermore, the long channel cut-off voltage model parameter VOFF can be further modeled in terms of the Schottky barrier height (ϕ_b), conduction band energy difference between the hetero-junction (ΔE_c) etc [50, 51]. Equations (2.1), (2.2) & (2.3) can not be solved analytically, but can be

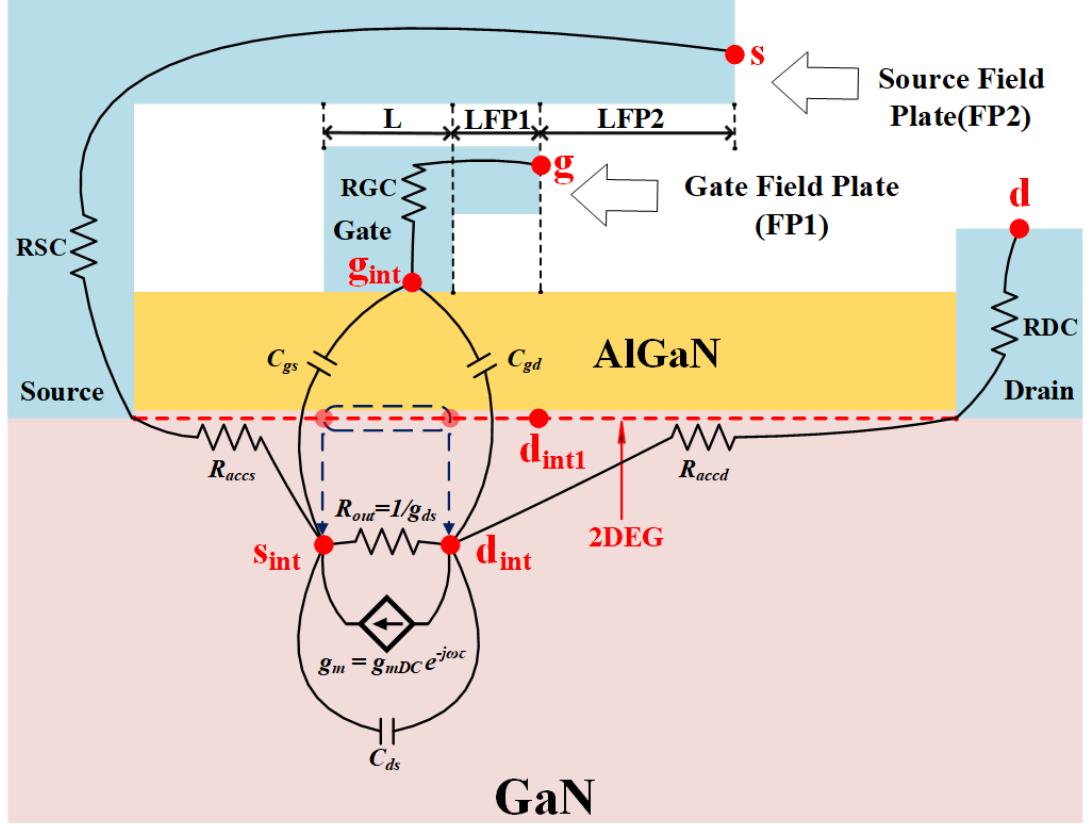


Figure 2.3: A typical cross section of a power AlGaN/GaN HEMT showing source and gate field plates, with various small-signal intrinsic elements which form part of intrinsic FET model. All capitalized elements are direct model parameters, while others are derived model elements from basic equations that are based on the underlying device physics.

solved numerically for a self-consistent set of n_s & E_f for an applied V_g using Householder's method for solving implicit functions described in detail in [43,53,54]. The value of Fermi potential E_f thus solved is calculated w.r.t the bottom of the conduction band as marked in Fig. 2.1. This value is assigned to the surface potential at internal source node in a HEMT structure, i.e. $\psi_s = E_f|_{(x=0)}$ (see Fig. 2.2 for the internal locations/nodes at which source and drain side surface potentials are defined along-with various geometry & process parameter definitions), because at source side, the solution to surface potential is only affected by the gate voltage and not the drain voltage under the assumptions that

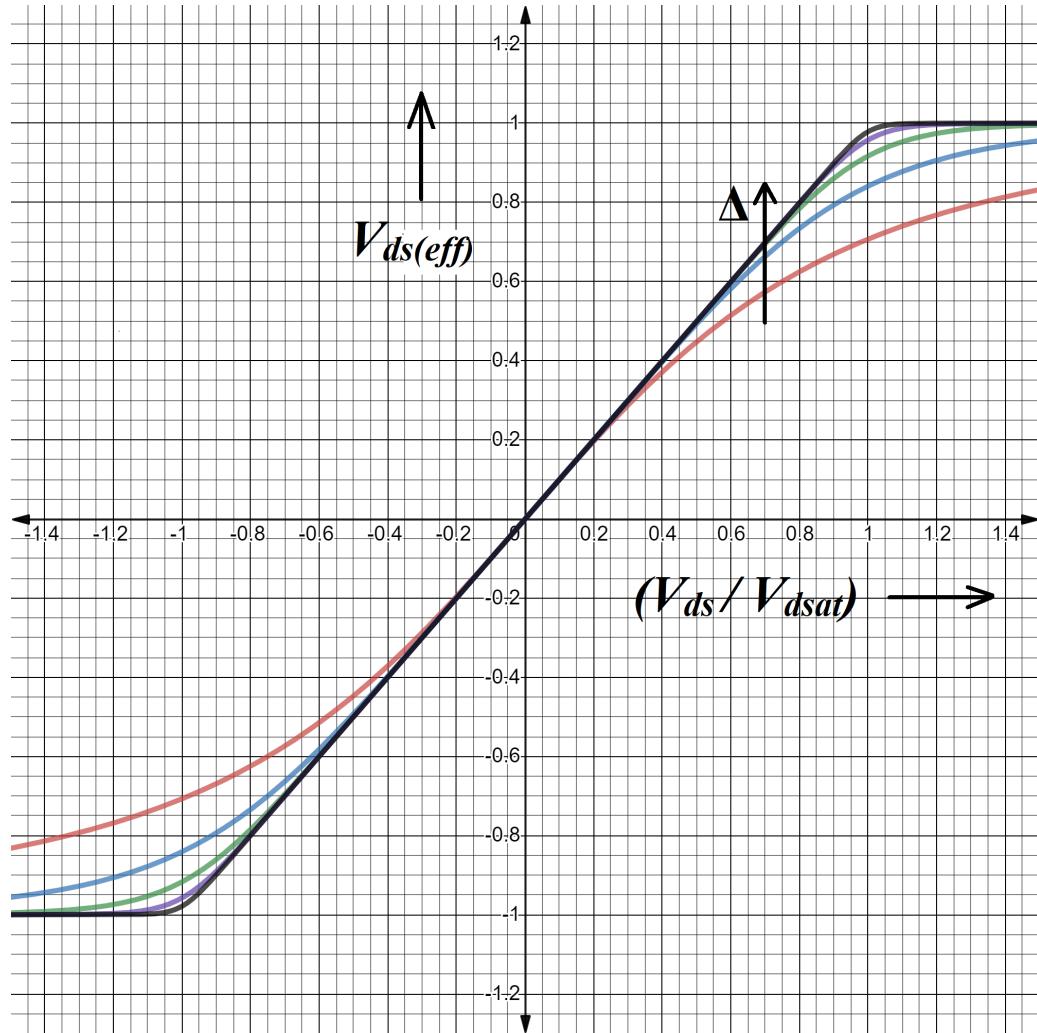


Figure 2.4: Plot of applied $V_{ds(eff)}$ vs $\pm(V_{ds}/V_{dsat})$ for different Δ 's from 2 to 32 in ascending geometric progression with common ratio of 2. It can be seen that as the value of Δ increases, the transition between linear to saturation for $V_{ds(eff)}$ becomes more abrupt.

source is the reference node (source referencing) and the channel length L is long enough such that drain voltage has not punched through to the source side. The surface potential at drain is calculated as per the procedure described in sub-section 2.2.4.

Since most of the commercial HEMT devices don't mention the process parameters used such as TBAR etc in their data-sheets, we defined capacitance per unit area of

AlGaN dielectric as a model parameter CGG0, i.e.

$$\text{CGG0} = C_g = \frac{\varepsilon_{\text{AlGaN}}}{\text{TBAR}} \quad \left[\frac{\text{F}}{\text{m}^2} \right]. \quad (2.4)$$

With this formulation for AlGaN capacitance, we have a model parameter that can be easily extracted from the OFF-ON state C-V measurements, details of which have been described in the chapter on parameter extraction (chapt.3).

2.2.2 Drain Current And Effective Mobility Models

The drain (or to be more precise - channel) current model equation can be called the key formulation required in the development of a FET compact model. In ASM-GaN, drift-diffusion framework is used to calculate the drain current. To begin with, if $V_{g0} = V_g - V_{off}$ is the gate overdrive voltage when referenced to the source terminal, then the electrostatically coupled surface channel charge density (Q_{ch}) at point x along the channel, with a certain gate overdrive is given by the expression,

$$Q_{ch} = qn_s = C_g (V_{go} - \psi) \quad \left[\frac{\text{C}}{\text{m}^2} \right], \quad (2.5)$$

where n_s is 2DEG surface charge density calculated by solving the implicit relationship in equations (2.1), (2.2) and (2.3), ψ is the surface potential at point x along the channel.

Under gradual channel approximation [52], the drain or channel current at any point x along the length of channel can be expressed as a combination of drift and diffusion components, i.e.

$$I_{ds} = -\mu_{eff} W Q_{ch} \frac{d\psi}{dx} + \mu_{eff} W V_{th} \frac{dQ_{ch}}{dx} \quad [\text{A}], \quad (2.6)$$

where μ_{eff} is the effective carrier mobility which takes into account the degradation in surface mobility due to vertical gate electric field, W is the channel width and $V_{th} = KT/q$. A general form of (2.6) can be written as

$$I_{ds} = \mu_{eff} W \tilde{Q}_{ch} \frac{d\psi}{dx}, \quad (2.7)$$

where $\tilde{Q}_{ch} = V_{th} \frac{dQ_{ch}}{d\psi} - Q_{ch}$. Taking dx in (2.6) to the left hand side and integrating from 0 to L , we get $I_{ds} \cdot L$. While on right hand side, integrating w.r.t $d\psi$ from source side to the drain side surface potential, we get the drain current equation of the form

$$I_{ds} = \frac{W}{L} \mu_{eff} C_g (V_{g0} - \psi_m + V_{th}) \psi_{ds}, \quad (2.8)$$

where $\psi_m = \frac{(\psi_d + \psi_s)}{2}$ is called mid-point surface potential & $\psi_{ds} = \psi_d - \psi_s$ is the potential difference across the channel (along the length L in Fig. 2.2). It must be noted here that the surface potentials ψ_s & ψ_d are being calculated at the internal source and drain terminals, viz. s_{int} and d_{int} in Fig. 2.3 respectively. That is, for the sake of brevity, $s \equiv s_{int}$ & $d \equiv d_{int}$ till we discuss the modeling of source and drain access region resistances in sub-section 2.2.5 because these internal nodes exist in the first place due to the access region potential drops.

We have already defined C_g as a model parameter CGG0 in previous sub-section, hence we define the remaining term $\frac{W}{L} \mu_{eff}$ as a new intermediate model parameter BETA. Thus (2.8) can be written as

$$I_{ds} = \text{CGG0 BETA } f(\psi_s, \psi_d, \text{Model parameters}) \quad [\text{A}]. \quad (2.9)$$

The carrier mobility in HEMT devices is found to be a function of 2DEG charge density, which itself is a function of the vertical electric field. Thus, following model which models the universal mobility behavior [55] is used to model the mobility of 2DEG electrons,

$$\mu_{eff} = \frac{\mu_0}{1 + \mu_A E_{y,eff} + \mu_B E_{y,eff}^2} \quad (2.10)$$

where μ_0 (model parameter U0) is the low vertical field surface mobility (since there is no ‘bulk’ mobility in HFETs), μ_A & μ_B (model parameters UA & UB) are the first and second order degradation parameters respectively, due to vertical electric field degradation effect. $E_{y,eff}$ is the effective vertical electric field, which is calculated using Gauss’s law on

channel region as $E_{y,eff} = \bar{Q}_{ch}/\varepsilon_{AlGaN}$, with $\bar{Q}_{ch} = C_g |V_{g0} - \psi_m|$ as the average surface channel charge density.

In (2.9) we defined an intermediate model parameter BETA, which is equal to product of $\frac{W}{L}$ with μ_{eff} of (2.10). Hence, we define a model parameter BETA0 which will be independent of the mobility degradation and will determine the value of the intermediate model parameter BETA as defined earlier in (2.9) as

$$\text{BETA} = \frac{\text{BETA0}}{1 + \text{UA} \cdot E_{y,eff} + \text{UB} \cdot E_{y,eff}^2} \quad [\frac{\text{m}^2}{\text{Vs}}], \quad (2.11)$$

where $E_{y,eff} = \frac{C_g}{\varepsilon_{AlGaN}} |V_{g0} - \psi_s|$ determines the effective vertical electric field on which the model of effective mobility μ_{eff} is based. Note that we have used ψ_s instead of ψ_m while calculating $E_{y,eff}$ in order to simplify the calculation.

2.2.3 Velocity Saturation Model

With an increase in the lateral electric field E_x , the 2DEG electrons can gain sufficient amount of energy to be scattered by optical phonons, thus resulting in a decrease in their mobility and ultimately saturation in their carrier velocity. To account for this increase in carrier velocity for lower lateral electric field and then eventual saturation in the carrier velocity with high lateral electric field, (2.9) is modified as

$$I_{ds} = \frac{\text{CGG0 BETA } f(\psi_s, \psi_d, \text{Model parameters})}{\sqrt{1 + (\mu_{eff}/v_{sat}E_x)^2}}, \quad (2.12)$$

where v_{sat} is the saturation velocity of the carriers and E_x is the average lateral electric field in the channel, which can be expressed in as $E_x = \frac{\psi_{ds}}{L}$. The term $\mu_{eff}/(v_{sat}L)$ is taken as a model parameter θ_{sat} which is extracted from the measurements in saturation region. With this, (2.12) becomes

$$I_{ds} = \frac{\text{CGG0 BETA } f(\psi_s, \psi_d, \text{Model parameters})}{\sqrt{1 + (\theta_{sat}\psi_{ds})^2}}, \quad (2.13)$$

The saturation velocity model for drift velocity (v_d) that includes velocity saturation effect at high lateral electric field $E_x = E_{sat}$, which is used to define the saturation velocity v_{sat} in equations (2.12) & (2.13) is given by [52]

$$v_d = \begin{cases} \frac{\mu_{eff}E_x}{1 + E_x/E_{sat}} & E_x < E_{sat} \\ v_{sat} & E_x \geq E_{sat}. \end{cases} \quad (2.14)$$

This formulation with $E_{sat} = 2 \cdot \frac{v_{sat}}{\mu_{eff}}$ ensures continuity of drift velocity v_d in (2.14) such that for lower E_x , $v_d \cong \mu_{eff}E_x$, while for electric field greater than saturation electric field E_{sat} , (2.14) reduces to v_{sat} . Furthermore, the saturation voltage V_{dsat} is calculated from the value of v_{sat} in (2.14) as

$$V_{dsat} = \frac{2 \cdot \frac{v_{sat}}{\mu_{eff}} L (V_{gs} - V_{off})}{2 \cdot \frac{v_{sat}}{\mu_{eff}} L + (V_{gs} - V_{off})}. \quad (2.15)$$

We defined the term $E_{sat}L = 2 \cdot \frac{v_{sat}}{\mu_{eff}}L$ at nominal temperature T_{nom} (a nominal temperature is a temperature at which the temperature independent model parameters are extracted) as a new model parameter VDSAT0, i.e.

$$\text{VDSAT0} = 2 \cdot \frac{v_{sat}}{\mu_{eff}}|_{(T=T_{nom})} L \quad [\text{V}], \quad (2.16)$$

which leads to a simplification of (2.15) as

$$V_{dsat}|_{(T=T_{nom})} = \frac{\text{VDSAT0} (V_{gs} - V_{off})}{\text{VDSAT0} + (V_{gs} - V_{off})}, \quad (2.17)$$

where the value of V_{dsat} at a user specified temperature T_{dev} is calculated by using a temperature scaling model parameter AT to calculate the value of an intermediate model parameter VDSAT at T_{dev} as $\text{VDSAT}|_{(T=T_{dev})} = \text{VDSAT0} \cdot (\frac{T_{dev}}{T_{nom}})^{AT}$ and then using this intermediate model parameter VDSAT instead of VDSAT0 in (2.17).

(2.13) can be called the core drain (channel) current equation that is used to model both the drift-diffusion components in the channel of the intrinsic device and which includes the saturation of the 2DEG electrons in its formulation. Furthermore, this method

does not change the physical interpretation of saturation voltage V_{dsat} as the voltage at which the intrinsic transistor/FET transitions from linear to saturation region.

2.2.4 Surface Potential Calculations At Source And Drain

The calculation of surface potential at source ψ_s has already been described in sub-section 2.2.1. The calculation was performed by solving equations (2.1), (2.2) with V_{gs} replacing the term V_g in (2.3) for the Fermi potential at the source end, i.e.

$$\psi_s = E_f|_{(x=0, V_g=V_{gs} \text{ in (2.3)})}. \quad (2.18)$$

This is possible because the Fermi potential in (2.3) is referenced to the bottom of the conduction band notch across the AlGaN/GaN hetero-junction, which is essentially the surface potential by definition. At the drain end,

- a) We have to use the gate overdrive voltage as referenced to drain potential i.e. $V_{gd} = V_{gs} - V_{ds}$ in place of V_g in (2.3) &
- b) Add the value of $V_{ds(eff)}$ to it in order to get the surface potential w.r.t source because ASM-GaN is a source referenced model. The voltage $V_{ds(eff)}$ can be seen as channel potential V_x at the drain end, while the channel potential at source end is taken to be zero because of the source referencing.

The preceding discussion leads to following relation for ψ_d

$$\psi_d = E_f|_{(x=L, V_g=V_{gd} \text{ in (2.3)})} + V_{ds(eff)}. \quad (2.19)$$

(2.19) contains $V_{ds(eff)}$ which should behave in the following manner, depending upon its value w.r.t the applied V_{ds}

$$V_{ds(eff)} \cong \begin{cases} V_{ds} & \text{if } V_{ds} < V_{dsat} \text{ i.e. linear region,} \\ V_{dsat} & \text{if } V_{ds} \geq V_{dsat} \text{ i.e. saturation region.} \end{cases} \quad (2.20)$$

In order to implement (2.20) with a smooth transition between linear and saturation regions, we use following functional form for $V_{ds(eff)}$

$$V_{ds(eff)} = V_{ds} \left(1 + \left(\frac{V_{ds}}{V_{dsat}} \right)^{\Delta} \right)^{-\frac{1}{\Delta}}, \quad \text{where } \Delta \in \{\text{even non-zero integers}\}, \quad (2.21)$$

where Δ (model parameter DELTA) is a smoothing parameter whose value must be an even non-zero integer. Fig. 2.4 shows the effect of this model parameter on the calculation of $V_{ds(eff)}$, where it is clear that a higher value of Δ makes the transition between the linear to saturation region less smooth, when compared with lower values of Δ .

2.2.5 Source/Drain Resistance Model

In the ASM-GaN model, the calculations of the source and drain resistances are performed by combining the various sources of resistances such as source & drain access region resistances R_{accs} & R_{accd} respectively, source & drain contact resistances RSC & RDC respectively, resistance contribution due to trapping effects etc [57]. In this analysis, we are neglecting the trapping effects and thus the total source & drain resistances can be expressed as

$$R_s = R_{accs} + \text{RSC}, \quad (2.22a)$$

$$R_d = R_{accd} + \text{RDC}, \quad (2.22b)$$

where the access region resistances are dependent on the 2DEG carrier concentrations at source & drain regions NS0ACCS & NS0ACCD respectively, 2DEG mobility at source & drain regions U0ACCS & U0ACCD respectively, source & drain access region lengths LSG & LDG respectively as shown in Fig. 2.2, channel width W and number of gate fingers NF in following manner

$$R_{accs} = \frac{\left(\frac{LSG}{W \cdot NF \cdot q \cdot NS0ACCS \cdot U0ACCS} \right)}{\left(1 - \left(\frac{I_{ds}}{I_{sat(source)}} \right)^{\text{MEXPACCS}} \right)^{\frac{1}{\text{MEXPACCS}}}}, \quad (2.23a)$$

$$R_{accd} = \frac{\left(\frac{LDG}{W \cdot NF \cdot q \cdot NS0ACCD \cdot U0ACCD}\right)}{\left(1 - \left(\frac{I_{ds}}{I_{sat(drain)}}\right)^{MEXPACCD}\right)^{\frac{1}{MEXPACCD}}}, \quad (2.23b)$$

where $I_{sat,source} = W \cdot NF \cdot NS0ACCS \cdot VSATACCS$ with VSATACCS being the saturation velocity of 2DEG carriers in source access region, $I_{sat,drain} = W \cdot NF \cdot NS0ACCD \cdot VSATACCD$ with VSATACCD being the saturation velocity of 2DEG carriers in drain access region, MEXPACCS & MEXPACCD are the exponents for source & drain access region resistance calculations respectively.

In the proposed power GaN intrinsic FET model, the equations for access regions in (2.23) are simplified to

$$R_{accs} = \frac{RSS0}{\left(1 - \left(\frac{I_{ds}}{IDMAX}\right)^{MEXPACCS}\right)^{\frac{1}{MEXPACCS}}} \quad [\Omega], \quad (2.24a)$$

$$R_{accd} = \frac{RDD0}{\left(1 - \left(\frac{I_{ds}}{IDMAX}\right)^{MEXPACCS}\right)^{\frac{1}{MEXPACCS}}} \quad [\Omega]. \quad (2.24b)$$

where model parameters RSS0 and RDD0 are zero bias current resistances of source and drain access regions respectively, IDMAX controls the transition from linear to saturation region and the exponents of source & drain access region resistances are same and equal to MEXPACCS. Thus, equations (2.24a) and (2.24b) describe the non-linear behavior of access region resistances. This completes the reformulation of the DC model in ASM-GaN.

2.2.6 Charge Model

In order to describe the charge behavior in a consistent manner, efforts were made to change the surface potential based calculations of charges in terms of the newly defined parameters. This was done by introducing an area related parameter AREAFAC, which accounts for the product of $W \cdot L \cdot NF$ i.e. area of AlGaN layer gate - to channel coupling capacitance as shown in Fig. 2.2, in the calculation of the actual charge from the CGG0 i.e., capacitance per unit area. Thus, after calculating the mid-point surface potential

$\psi_m = (\psi_s + \psi_d)/2$ and thermal voltage $V_{th} = KT/q$, we can calculate the gate charge as [58]

$$Q_g = \frac{CGG0 \cdot AREAFACT}{(V_{g0} - \psi_m + V_{th})} \left[V_{g0}^2 + (1/3) (\psi_d^2 + \psi_s^2 + \psi_d \psi_s) - V_{g0} (\psi_d + \psi_s - V_{th}) - V_{th} \psi_m \right] \quad [C]. \quad (2.25)$$

The drain and source terminal charges were derived in [58] using Ward-Dutton's partitioning scheme [61, 62] by defining $Q_d = \int_0^L (x/L) Q_{ch}(V_g, V_x) dx$ and $Q_s = \int_0^L (1 - x/L) Q_{ch}(V_g, V_x) dx$, where $Q_{ch}(V_g, V_x) = Q_d + Q_s$ is the channel charge with V_x as channel potential at any point x in the channel region shown in Fig. 2.2. The channel potential V_x varies as zero at source end and $V_{ds(eff)}$ as given by (2.21) at the drain end. After solving for drain charge, we get following expression

$$Q_d = -\frac{CGG0 \cdot AREAFACT}{120(V_{g0} - \psi_m + V_{th})^2} \left[12\psi_d^3 + 8\psi_s^3 + \psi_s^2 (16\psi_d - 5(V_{th} + 8V_{g0})) + 2\psi_s (12\psi_d^2 - 5\psi_d (5V_{th} + 8V_{g0}) + 10(V_{th} + V_{g0}) (V_{th} + 4V_{g0})) + 15\psi_d^2 (3V_{th} + 4V_{g0}) - 60V_{g0} (V_{th} + V_{g0})^2 + 20\psi_d (V_{th} + V_{g0}) (2V_{th} + 5V_{g0}) \right] \quad (2.26)$$

Once drain terminal charge is calculated by (2.26), the source terminal charge is obtained by the law of conservation of charge as $Q_s = -Q_g - Q_d$. Using this approach, we preserve the consistency between charge and the drain (channel) current model which was described earlier.

Once the terminal charges are calculated, the various non-reciprocal small-signal capacitances of the intrinsic FET are calculated as per the charge-based small-signal capacitance model [52, 59, 60]

$$C_{ab} = \gamma \frac{\partial Q_a}{\partial V_b}, \quad (2.27)$$

where sub-scripts a or b could be gate, drain or source terminals, Q_a and V_b are the charge and voltage associated with terminals a and b respectively. $\gamma = 1$ if $a = b$ or -1 if $a \neq b$.

It can be observed that the newly derived equations (2.9), (2.11), (2.13), (2.17), (2.24), (2.25) and (2.26), which are implemented in the new model, do not contain any of the original model parameters associated with device geometry or process information.

At this juncture, it will be best to present a unified picture of the models described till now in terms of equivalent small-signal sub-circuit components as shown in Fig. 2.3. The intrinsic channel region is modeled by a trans-conductance g_m which is the first order derivative of (2.13) w.r.t V_{gs} , and output-conductance g_{ds} which is the first order derivative of (2.13) w.r.t V_{ds} . These derivatives are evaluated while simulating the Verilog-A code and hence are shown as sub-circuit elements in Fig. 2.3. Furthermore, various resistances and capacitances of the intrinsic model are shown in Fig. 2.3. They include non-linear source and drain access region resistances, which have been modeled as resistance elements R_{accs} and R_{accd} respectively and are given by (2.24a) and (2.24b) respectively, bias independent source and drain contact resistances RSC and RDC (capitalized as they are direct model parameters and unlike R_{accs} and R_{accd} , are not derived quantities in model) and gate contact resistance RGC. In addition, various intrinsic small-signal capacitances such as gate to drain (C_{gd}), gate to source (C_{gs}) and drain to source (C_{ds}) are also shown. They are derived in simulation as per (2.27).

2.2.7 Field-Plate Capacitance Model

The packaged power AlGaN/GaN HEMTs usually come with source and gate field plates, both of which have different purposes. The gate field plate (FP1 in Fig. 2.3) helps in reducing the gate resistance and elimination of electron trapping [63]. The gate field plate design takes into consideration the dielectric constant and the thickness of the insulator layer beneath the gate field plate and the length of the gate field plate (LFP1) [64]. It is found that we can increase the breakdown voltage (BV) of a HEMT significantly by choosing higher dielectric constant of the insulator beneath, in addition to increased LFP1

as shown in Fig. 2.3 and increased insulator thickness which is not shown specifically in Fig. 2.3.

The role of source field plate (FP2 in Fig. 2.3) is to help re-distribute the electric field near the drain end of the transistor and subsequently reduce the peak electric field by Faraday shielding effect[63, 65] and thus increase the breakdown voltage of a device without source field plate. However, this method of adding additional field plates increases the overall Miller capacitance (C_{gd} or C_{iss}) as a result of the successive turn ON of field plates FP1 and FP2 in the OFF-state which will be discussed in the chapter on parameter extraction of intrinsic FET (chapt.3).

The field plates FP1 and FP2 are already modeled as two separate sub-circuit HEMT transistors [47] with VOFFFP1 & VOFFFP2 as cut-off voltage parameters, LFP1 & LFP2 as length of field plates, DFP1 & DFP2 as thickness of the insulator beneath the field plates respectively. Since commercial devices don't provide these process and geometry parameters either, we made the formulation for these field plates independent of these manufacturing related parameters by re-defining their 2DEG electron density, drain current, mobility, velocity saturation, surface potential and charge formulations in the same way as described in previous sub-sections. Thus, we have new model parameters CGG0FP1 & CGG0FP2 for capacitance per unit area of FP1 & FP2, BETA0FP1 & BETA0FP2 for trans-conductance factors of FP1 & FP2, AREAFAFP1 & AREAFAFP2 for geometry (area) factors of FP1 & FP2, VDSAT0FP1 & VDSAT0FP2 for saturation velocity factors of FP1 & FP2 respectively.

2.2.8 Self Heating And DIBL Models

Successive scaling of all the dimensions (W , L , LSG , LDG , TBAR) of AlGaN/GaN HEMTs will eventually lead to increase in the power densities and peak electric field near drain end, which will in turn exacerbate the phenomena of self-heating and DIBL (Drain

Induced Barrier Lowering) respectively. These two effects have already been implemented in the Verilog-A code of ASM-GaN [57, 66]. The self heating model is a simple parallel combination of thermal resistance RTH0 (K/W) and capacitance CTH0 (sW/K) which accepts the power generated in the 2DEG channel ($P_{gen} = V_{ds} \times I_{ds}$) as a current source feeding the network. One of the thermal node ('dta' in Fig. 1.3) is considered as ground and hence the other thermal node ('dt' in Fig. 1.3) represents a change in temperature (ΔT_{dev}) due to self-heating in the channel. This change is then added to the device temperature and then used in the simulation, i.e. $T_{dev(updated)} = T_{dev} + \Delta T_{dev}$. The updated calculation of current using the new temperature does require the correct scaling of temperature scaling parameters for BETA0 (which is UTE) and saturation velocity parameter VDSAT0 (which is AT).

The threshold voltage lowering due to DIBL is given by

$$V_{off(DIBL)} = VOFF - ETA0 \cdot \left(\frac{V_{ds} \cdot VDSCALE}{\sqrt{V_{ds}^2 + VDSCALE^2}} \right), \quad (2.28)$$

where VDSCALE is a scaling model parameter and ETA0 is the DIBL model parameter. Thus, (2.28) models the lowering of the cutoff voltage due to lowering of the drain side potential barrier as a response to applied drain voltage V_{ds} .

2.3 Other Models

Besides the above mentioned models, ASM-GaN models the quantum mechanical shift of the centroid of the 2DEG charge away from the AlGaN/GaN hetero-junction; threshold voltage, sub-threshold slope & source/drain resistance etc shifts due to trapping effects, channel length modulation; parasitic, overlap and fringing capacitances, various (leakage/off and on state) gate currents, thermal and flicker noise models and finally, the temperature scaling of various model parameters in order to model the data collected

at various temperatures [57]. Out of these models, we will use the sub-threshold slope (NFACTOR) and overlap capacitances (CGDO, CGSO & CDSO) to extract the model parameters of a commercial power AlGaN/GaN HEMT power device in the next chapter.

3

Modeling Of Power AlGaN/GaN HEMTs: Parameter Extraction

“Consciousness cannot be accounted for in physical terms. For consciousness is absolutely fundamental. It cannot be accounted for in terms of anything else.”

– Erwin Schrödinger

3.1 Introduction

IN the previous chapter, we saw a re-formulation of the ASM-GaN compact model in order to make it usable for parameter extraction of commercial AlGaN/GaN power HEMTs. This resulted in a modified Verilog-A code with a set of new model parameters in addition to the existing ones. In this chapter, we present a practical demonstration of how to use such a process and geometry independent hybrid model [67] to extract the model parameters based on various measurements such as DC I-V, OFF-ON state C-V and OFF-state C-V measurements.

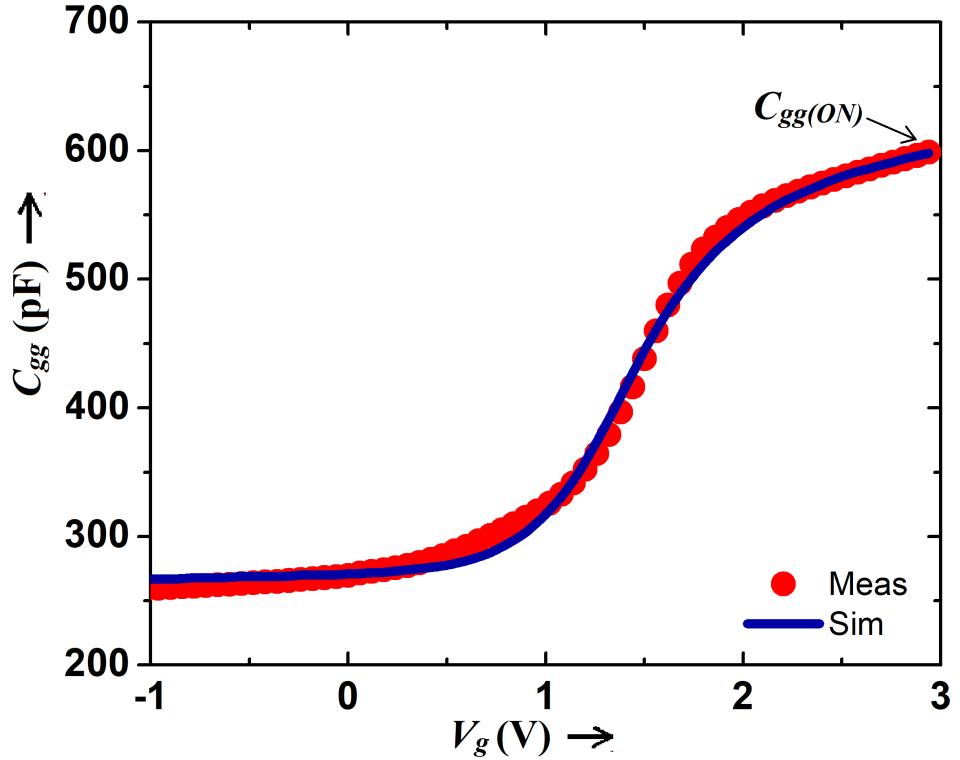


Figure 3.1: Intrinsic FET model simulation (solid line) vs measured data (symbols) of Panasonic’s packaged GaN device PGA26E19BA for OFF-ON C-V characteristics measured at 1 MHz.

3.2 Measurements

In this section, we describe the various measurements that were performed on Panasonic’s e-mode, packaged GaN transistor PGA26E19BA [68], in order to demonstrate the practical usefulness of the model that was developed in previous chapter. DC I_{ds} - V_{ds} characteristics were measured using Keysight’s B1505A [69] parameter analyzer. An effective series resistance of probes was measured and included in the ICCAP setup for measurement and simulation in order to separate the voltage drop across the probes and calculate the packaged device’s drain-source voltage drop. C_{gg} - V_g characteristics was measured using Keysight’s 4285A [70] precision LCR meter. The oscillation frequency of the small-signal source inside the LCR meter was set to 1 MHz in order to get the correct

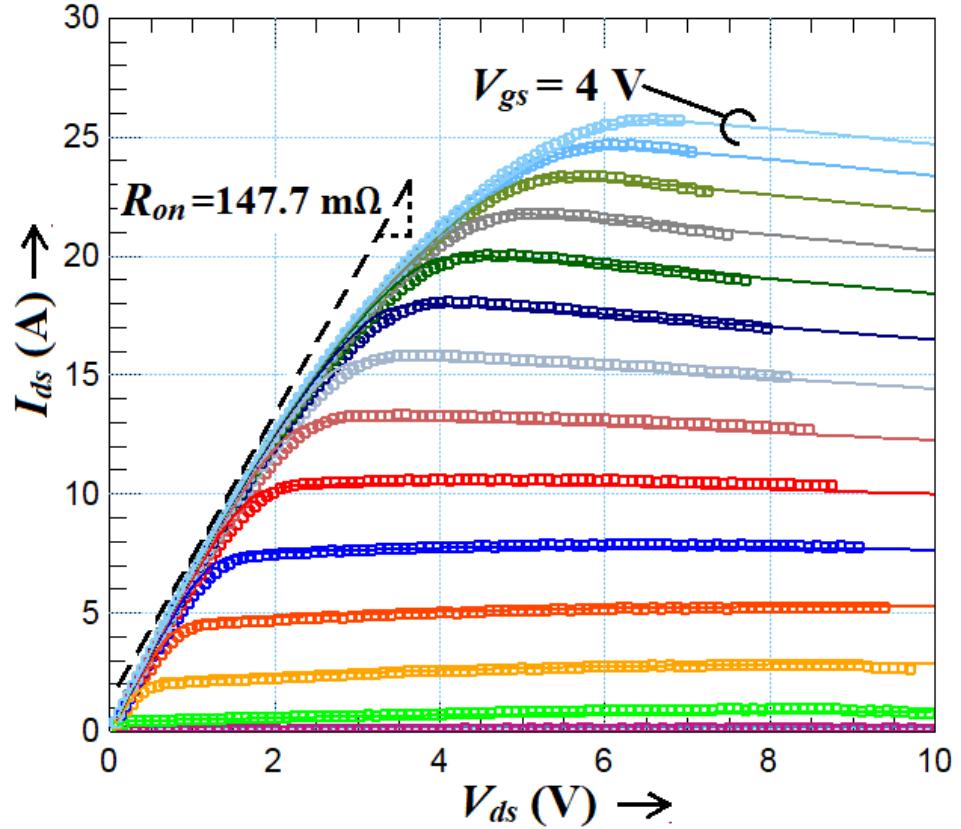


Figure 3.2: Intrinsic FET model simulation (solid line) vs measured data (symbols) for output DC I-V characteristics of Panasonic’s packaged GaN device PGA26E19BA with V_{gs} ranging from 1 V to 4 V in steps of 0.2 V.

capacitance behavior. The OFF-state S -parameter measurements were measured using Keysight’s PD-1000A measurement system [71] with frequency sweep from 0.05 to 600 MHz. Package parasitic modeling using these OFF-state measurements is described in the next chapter (chapt.4). The model parameter extraction flow for different components of the model is described in the following section where we describe the OFF-ON state C-V, I-V and OFF-state C-V modeling in detail.

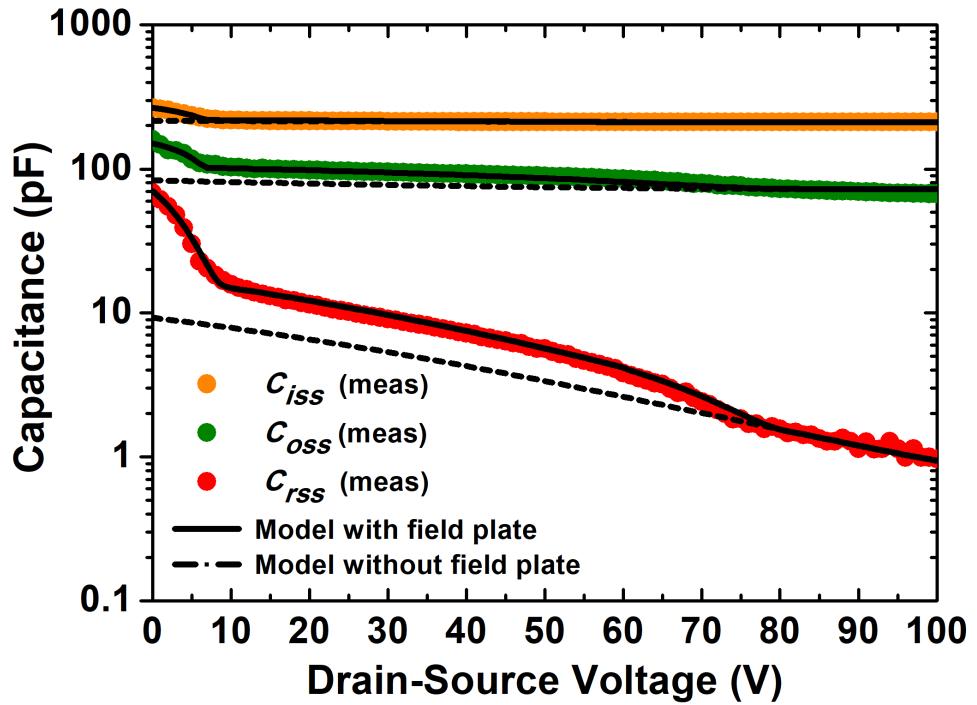


Figure 3.3: Intrinsic FET model simulation vs measured data of Panasonic’s packaged GaN device PGA26E19BA for OFF-state C-V characteristics.

3.3 Extraction Flow For Measured Intrinsic Device Characteristics

The extraction flow for the device measured in the previous section starts with the extraction of CGG0 and VOFF parameters from the OFF-ON C-V measurement performed at $V_{ds} = 0$ V. This is shown in Fig. 3.1. This measurement can be easily performed with regular C-V meters because the power devices are quite large and hence the measured capacitance is very high and above the noise floor of a regular C-V meter. The parameters CGG0 and AREAFACT control the value of capacitance when the device is fully ON ($C_{gg(ON)}$), while model parameter VOFF is the cut-off voltage at which capacitance starts to rise as shown in Fig. 1.1.

Table 3.1: Extracted model parameters from DC I-V measurement

Parameter	Unit	Extracted Value	Description
CGG0	F/m ²	2.264×10^{-3}	C_g value in ON-state
BETA0	m ² /Vs	400×10^3	Trans-conductance factor
UA	m ² /V	0	First order coefficient of BETA0 degradation
UB	m ² /V ²	0	Second order coefficient of BETA0 degradation
AREAFAC	10 ⁻¹² m ²	160×10^3	Geometry factor for $C_{gg(ON)}$
VOFF	V	1.8	Threshold voltage in linear region
ETA0	Unitless	12×10^{-3}	DIBL factor for threshold voltage in saturation region
VDSAT0	V	0.9	Saturation velocity parameter
RDSMODPA	Unitless	1	Flag for (2.24)
RSS0	Ω	20.53×10^{-3}	Bias independent source access resistance (2.24a)
RDD0	Ω	40×10^{-3}	Bias independent drain access resistance (2.24b)
IDMAX	A	28	Max current in (2.24)
MEXPACC	Unitless	2	Exponent in (2.24)
RSC	Ω	31×10^{-3}	Source contact resistance
RDC	Ω	61×10^{-3}	Drain contact resistance
SHMOD	Unitless	1	Flag for self-heating model
RTH0	K/W	2	Thermal resistance
AT	Unitless	-2	VDSAT0 temperature scaling
UTE	Unitless	-2	BETA0 temperature scaling

$$C_{gg(ON)} = CGG0 \text{ AREAFACT} [F]. \quad (3.1)$$

The capacitance below VOFF is modeled by two parameters CGDO and CGSO, which are OFF-state overlap capacitances from gate-to-drain (node g to node d in Fig. 2.3) and gate-to-source (node g to node s in Fig. 2.3) respectively.

Next, the I-V characteristics were modeled. The parameter extraction flow is as fol-

Table 3.2: Extracted model parameters from OFF-state capacitance measurements

Parameter	Unit	Extracted Value	Description
CGDO	F	20×10^{-12}	OFF-state gate-drain capacitance
CGDL	F	146.9×10^{-15}	Voltage variation of OFF-state gate-drain capacitance
CGSO	F	201×10^{-12}	OFF-state gate-source capacitance
CDSO	F	39.53×10^{-12}	OFF-state drain-source capacitance
FP1MOD	Unitless	1	First field plate flag
CGG0FP1	F/m ²	1.01×10^{-3}	Gate capacitance/area of first field plate
BETA0FP1	m ² /Vs	400×10^3	Trans-conductance factor of first field plate
AREAFACFP1	10 ⁻¹² m ²	97.09×10^3	Geometry factor of first field plate
VOFFFP1	V	-22	Threshold voltage of first field plate
VDSAT0FP1	V	1	Saturation velocity parameter of first field plate
FP2MOD	Unitless	2	Second Field plate flag
CGG0FP2	F/m ²	0.2132×10^{-4}	Gate capacitance/area of second field plate
BETA0FP2	m ² /Vs	400×10^3	Trans-conductance factor of second field plate
AREAFACFP2	10 ⁻¹² m ²	10×10^3	Geometry factor of second field plate
VOFFFP2	V	-76	Threshold voltage of second field plate
VDSAT0FP2	V	1	Saturation velocity parameter of second field plate

lows. VOFF (linear region threshold voltage), BETA0 (mobility), RDD0, RSS0, RSC, RDC, MEXPACCS, IDMAX are used to fit the linear region of Fig. 3.2. For the saturation region, parameters such as ETA0 (drain voltage dependence of threshold voltage due to the drain-induced barrier lowering effect) and VDSAT0 were used. Furthermore, we see a current degradation in the region of high V_{gs} and V_{ds} bias as shown in Fig. 3.2. This is because of the well-known phenomenon of self-heating. In order to capture this effect, we used the standard thermal network that exists in the ASM-GaN model [57]. From that thermal network model, we tuned the values of thermal resistance model parameter RTH0 along-with temperature scaling parameters for saturation velocity/voltage

(VDSAT0) - AT and trans-conductance factor (BETA0) - UTE until we got good fits for the current degradation at high bias. The extracted values of parameters used for fitting I-V characteristics are given in Table. 3.1.

Next, we modeled the standard OFF-state capacitance measurements, which are generally given in the data-sheets of commercial power transistors such as PGA26E19BA [68]. These are C_{iss} , C_{rss} , and C_{oss} . These three OFF-state capacitances are a combination of three intrinsic capacitances in OFF-state, viz. C_{gs} , C_{gd} and C_{ds} (existing between the external nodes g, d & s in Fig. 2.3^{§§}). The definitions of the various capacitances as measured and modeled in Fig. 3.3 are:

$$C_{rss} = C_{gd}, \quad (3.2a)$$

$$C_{iss} = C_{gd} + C_{gs}, \quad (3.2b)$$

$$C_{oss} = C_{gd} + C_{ds}. \quad (3.2c)$$

The OFF-state capacitance C_{rss} vs V_{ds} plot exhibits two kinks which correspond to turning ON of the 2DEG channel under gate field plate (FP1) and later on, of source field plate (FP2) as the V_{ds} increases from 0 to 100 V. This is because the threshold voltage of the gate field plate (VOFFFP1, which is negative) is lower in magnitude than the threshold voltage of the source field plate (VOFFFP2, which is more negative than VOFFFP1) due to the higher dielectric barrier thickness of the latter than former. The conditions for turning ON of these field plates can be summarized as follows. For gate field plate (FP1)

^{§§}In the same figure, the same capacitances have been shown between internal nodes g_{int} , d_{int} & s_{int} for the ON-state of the device. For OFF-state, the capacitances between those internal nodes are ≈ 0 and the only source of capacitances are the overlap and fringing parasitic capacitances between the outer nodes g, d & s, which have been modeled in ASM-GaN by four model parameters CGSO, CGDO, CDSO & CGDL (voltage dependence of CGDO). Furthermore, these capacitances, being parasitic in nature, are not non-reciprocal and hence the ordering of the nodes doesn't matter in OFF-state, e.g. $C_{gd} = C_{dg}$ etc.

to turn ON (see Fig. 2.3)

$$V_{gd_{int}} > \text{VOFFFP1}, \quad (3.3)$$

and for source field plate (FP2) to turn ON (see Fig. 2.3)

$$V_{sd_{int1}} > \text{VOFFFP2}. \quad (3.4)$$

A way to interpret the two kinks in C_{rss} in Fig. 3.3 is to scan the Fig. 3.3 from high V_{ds} (100 V) to low V_{ds} (0 V) i.e., from right to left. The point at which we encounter the first upward kink corresponds to VOFFFP2 (source field plate) because the condition of (3.4) gets satisfied at that point. The model parameters VOFFFP2, AREAFAFP2 along-with the one already fitted for OFF-ON state capacitance: gate-drain overlap model parameter CGDO are used to capture this. Furthermore, as we go leftward, we encounter the second upward kink when condition for (3.3) gets satisfied. The model parameters VOFFFP1, AREAFAFP1 in conjunction with CGDO are used to model this area. Simulation plots for “Model without field plate” are also shown in Fig. 3.3 to see the importance of modeling these regions and the amount of extra capacitance that these field plates add when they turn ON successively. The remaining two capacitances C_{iss} and C_{oss} are modeled effectively by tuning remaining OFF-state overlap model parameters CGSO and CDSO respectively. Table. 3.2 shows the parameters extracted while fitting the different OFF-state C-V’s as shown in Fig. 3.3.

3.4 Boost Converter Design Example Using Extracted Intrinsic Model

A circuit diagram of a DC-DC boost converter is shown in Fig. 3.4. We used specifications of a 100 W boost converter design given in [72] to simulate the steady state and transient characteristics of such a circuit. For the GaN transistor Q in Fig. 3.4, we used

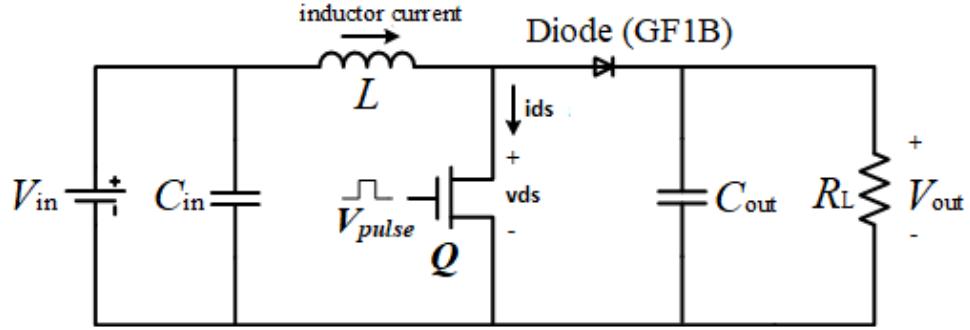


Figure 3.4: Schematic of a DC-DC boost converter.

Table 3.3: Design parameters of boost converter for different switching frequencies with a constant duty cycle of 0.45

f_{sw} (MHz)	ΔV_{out} (V)	ΔI_L (A)	C_{out} (μF)	L (μH)	T_{on} (nsec)
1	0.45	2.4	4	10.415	450
5	0.45	2.4	4	2.083	90

extracted model card from the previous section for the device PGA26E19BA. The circuit was designed for two switching frequencies f_{sw} of 1 MHz and 5 MHz using standard boost converter equations from [73]. The values of input inductor L , output capacitor C_{out} along with design specifications used are given in Table. 3.3. Although very accurate simulation would require the knowledge of package parasitics [75], we have omitted them here because of convergence issues faced by us while trying to simulate with full package parasitic model, which has been formulated and extracted in the next chapter (chapt.4). We have traced those convergence issues mainly to the presence of parasitic inductors in the package model which cause unrealistically high voltage drop estimates across the inductors during transient simulation for a pulsed input with very high rise and fall times. Besides Spectre, we also tried simulating this circuit with full package parasitic model in ADS etc but found similar convergence problems. Thus, designing a robust simulator that specifically caters to power electronic circuits could be a future project for those

working in EDA (Electronic Design Automation) area. Hence, our aim in this exercise is to demonstrate the efficacy of the extracted intrinsic model card in designing a given power electronic circuit with IOS (Initial Objective Specifications) taken from [72].

3.4.1 Circuit Design Method

We start by identifying the knee current (determined at the border between linear and saturation) in the output characteristics (Fig. 3.2) for a particular gate-source voltage ($V_{gs(min)} = 2$ V), which will be the minimum pulsed value of the voltage driven by a gate-drive circuit in a practical application (however during simulation, we found out that the peak pulsed voltage at the gate must be higher than this $V_{gs(min)}$ and took $V_{gs(actual)} = 2.5$ V). This knee current will be the maximum output current $I_{out(max)}$ ($= id_{(max)}$) at which the transistor Q remains in linear region (ON-state) and when the inductor current reaches maximum charging as determined by the magnetic saturation rating of the inductor L . Thus, the inductor's magnetic saturation rating must be selected carefully to at least match the $I_{out(max)}$ calculated above. Then, we used the design procedure given in [73] to find the estimated ripple current in inductor in terms of $I_{out(max)}$ as:

$$\Delta I_L = k \times I_{out(max)} \times \frac{V_{out}}{V_{in}}, \quad (3.5)$$

where k can be in between 0.2 to 0.4. We took a value of 0.3 for our design. We can now find out the inductor value from the equation:

$$L = \frac{V_{in} \times (V_{out} - V_{in})}{\Delta I_L \times f_{sw} \times V_{out}}. \quad (3.6)$$

For the diode, we used a diode model for the power diode GF1B from Vishay[74]. Next, we assumed zero ESR and a voltage ripple of ΔV_{out} for the output capacitance and found out the minimum output capacitance that supports such a voltage ripple by:

$$C_{out(min)} = \frac{I_{out(max)} \times D}{f_{sw} \times \Delta V_{out}}, \quad (3.7)$$

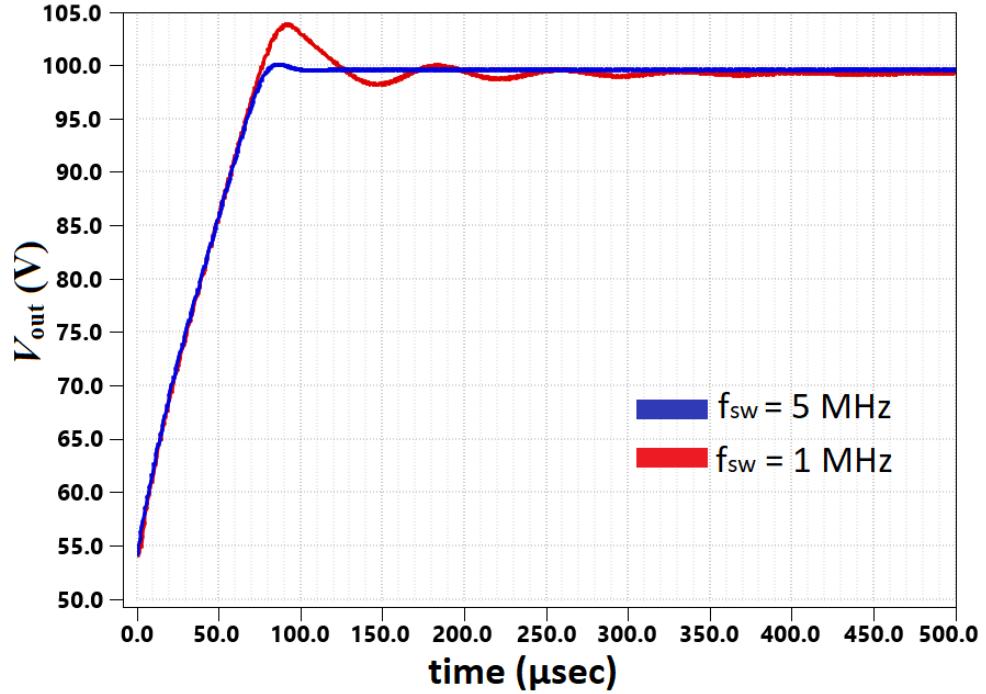


Figure 3.5: Comparison of transient V_{out} for two different switching frequencies f_{sw} of 1 MHz and 5 MHz. The model predicts faster settling time and close to critically damped response for f_{sw} of 5 MHz.

where D is the duty cycle, which we fixed to 0.45 as per the design in [72]. The C_{out} in the design is then taken as this calculated value of $C_{out(\min)}$. This entire process was repeated for the two switching frequencies of 1 MHz and 5 MHz to arrive at Table. 3.3.

3.4.2 Circuit Simulation Results And Discussion

The designed boost converter circuit was simulated with Spectre as circuit simulator. A detailed discussion on how to setup such switching converter simulations in Spectre is given in appendix.A. A transient analysis was run starting from zero time till 1 msec to ensure a steady state operation of the circuit. Fig. 3.5 shows plot of V_{out} vs time obtained from the transient simulation. The circuit predicts faster settling time and close to a critically damped response for higher f_{sw} (5 MHz), while a slow settling time and under-damped response for lower f_{sw} (1 MHz).

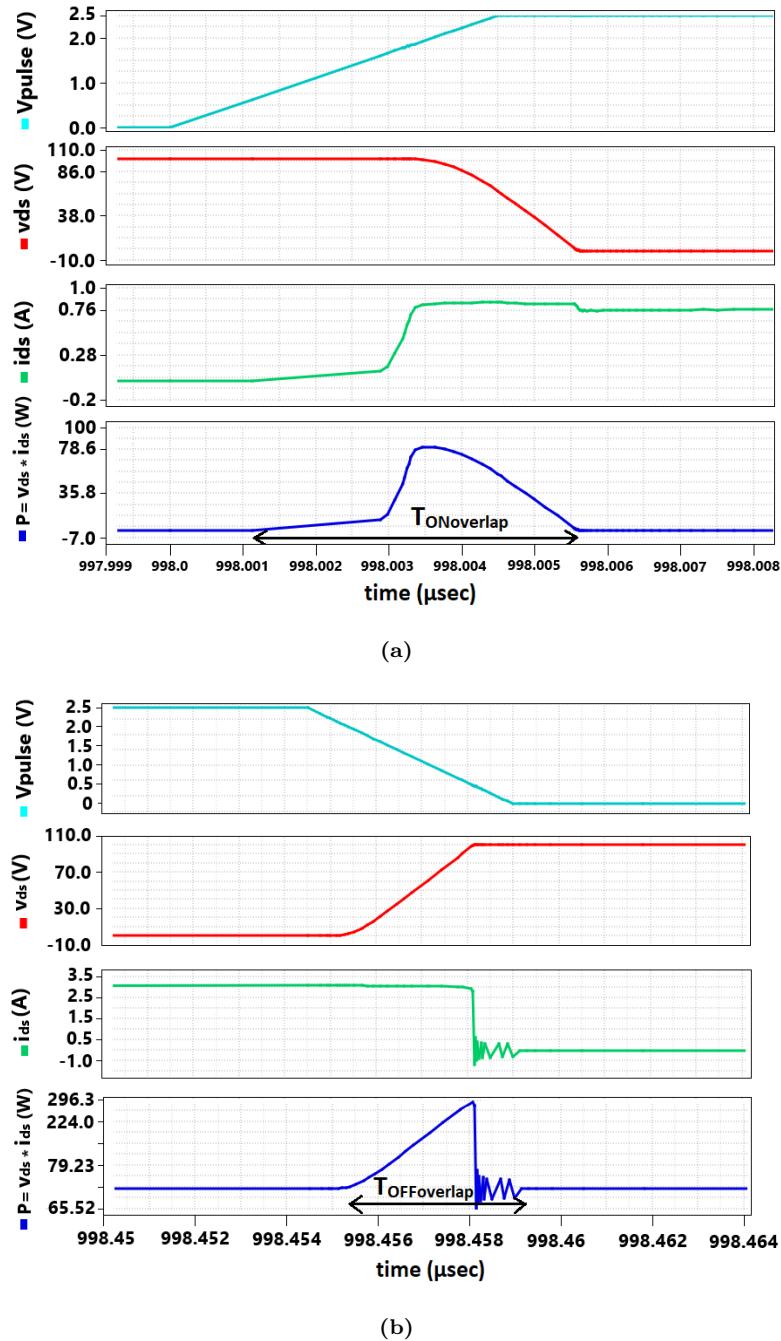
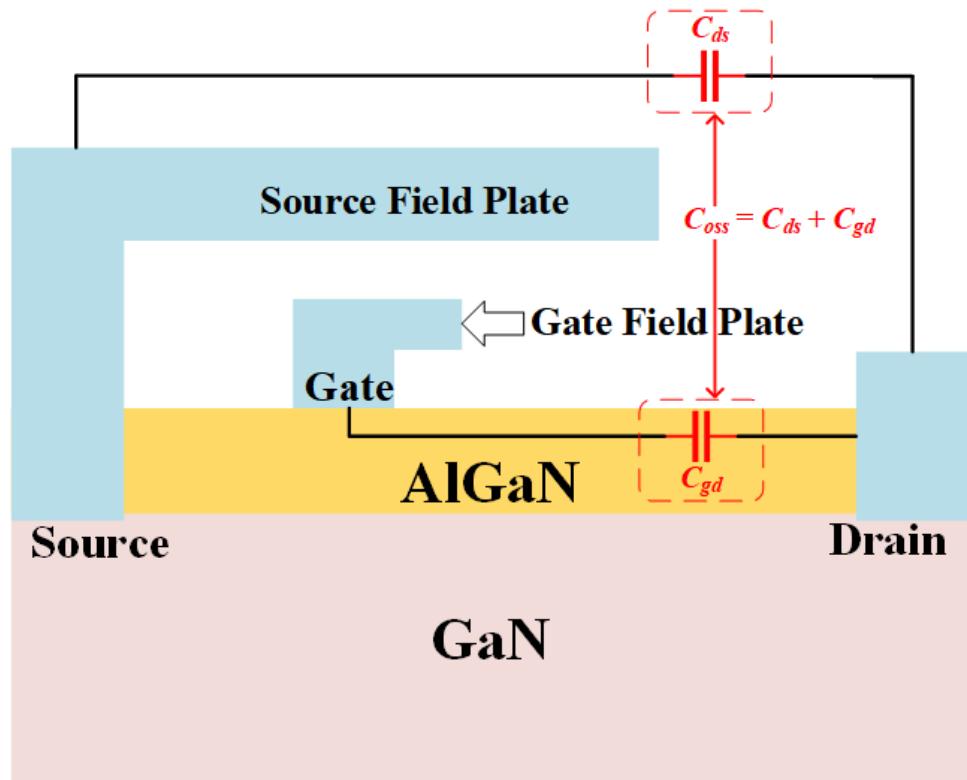


Figure 3.6: (a) Steady state switching waveforms of model with field plate for $f_{sw} = 1$ MHz during transition from OFF-state to ON-state leading to energy loss E_{ON} & (b) Steady state switching waveforms of model with field plate for $f_{sw} = 1$ MHz during transition from ON-state to OFF-state leading to energy loss E_{OFF} .

Table 3.4: Hard switching losses with and without field plate

Without Field Plate		With Field Plate	
E_{ON}	E_{OFF}	E_{ON}	E_{OFF}
140.5 nJ	395.2 nJ	131.6 nJ	395.2 nJ

**Figure 3.7:** Typical cross-section of a power GaN device clearly showing the output capacitance C_{oss} with its two components viz. C_{ds} and C_{gd} .

Furthermore, Figs. 3.6a and 3.6b show a zoomed in portion of the steady state waveform for drain-source voltage (v_{ds}) and current (i_{ds}) and their product which is the power loss in transistor Q . The ON and OFF state hard switching losses calculated from these waveforms are shown in Table. 3.4 with and without field plate in the transistor model. This can be achieved by toggling model flags related to field plate capacitances as already explained.

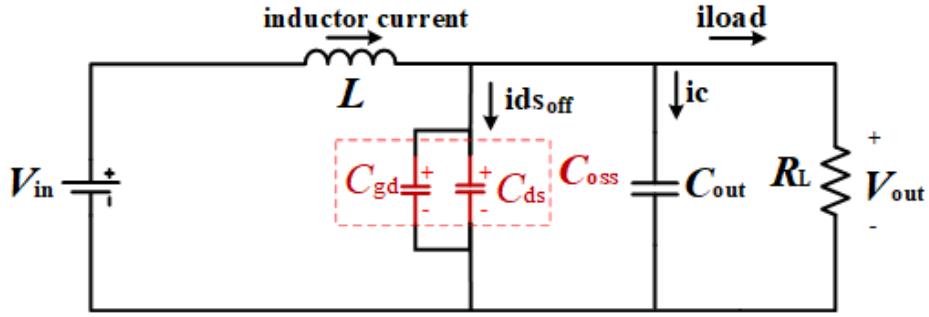


Figure 3.8: Equivalent circuit of the boost converter in Fig. 3.4 with the transistor Q in OFF-state for the time T_{OFF} of a switching cycle.

Fig. 3.7 shows the physical origin of the OFF-state output capacitance C_{oss} . This capacitance has two components - drain to source and gate to drain capacitances (i.e. $C_{oss} = C_{ds} + C_{gd}$), both of which have been modeled correctly for OFF-state C-V (C_{oss} vs V_{ds}) measurements as shown in the previous section (see Fig. 3.3). Capturing this variation is important for determining the large-signal switching behavior of a transistor because the transient waveform of v_{ds} (drain-source voltage) during switching is going to determine the value of the capacitor $C_{oss}(v_{ds})$ as seen by the input voltage V_{in} .

In order to understand how the OFF-state output capacitance C_{oss} affects the performance of the circuit, we consider the following scenario. During the OFF-state of transistor Q , the given boost topology looks like Fig. 3.8 with an output capacitance C_{oss} value of approximately 67 pF. During this time, C_{oss} charges with the polarity as shown in Fig. 3.8 with an OFF-state charging current of ids_{off} , while the output capacitor C_{out} and load resistor R_L pull out currents ic and i_{load} respectively. This charged capacitance with the given polarity of its terminals (Fig. 3.8) doesn't allow ids_{off} to change suddenly when the transistor Q is switched from OFF-state to ON-state because of the unrealistically high amount of dV/dt across C_{oss} required to increase the ids from ids_{off} to an ON-state value ids_{on} and hence the current doesn't rise from ids_{off} for quite a time during the initial ramp up period as shown in Fig. 3.6a.

A finite amount of power is lost during switching processes that occur from OFF to ON and then ON to OFF states, with a corresponding energy loss of E_{ON} and E_{OFF} respectively. These energy losses can be quantitatively calculated by integrating the overlap of drain current and drain-source voltage as shown in Figs. 3.6a & 3.6b.

$$E_{ON} = \int_{OFF\ STATE}^{ON\ STATE} i ds_{(t)} v ds_{(t)} dt, \quad (3.8a)$$

$$E_{OFF} = \int_{ON\ STATE}^{OFF\ STATE} i ds_{(t)} v ds_{(t)} dt. \quad (3.8b)$$

Table. 3.4 shows that there is no difference between E_{OFF} predicted by using model with or without field plate, while E_{ON} shows a difference of about 8.9 nJ ($\approx 6\%$). This difference arises because C_{oss} sees a different capacitance value during the transient voltage drop of vds from 100 V (OFF-state) to some linear region (ON-state) value of few hundreds of mV for simulations with and without field plate as per Fig. 3.3, which leads to different amount of switching drain currents $i ds_{(t)}$ during the transition from OFF-state to ON-state. These varying amounts of switching currents lead to different instantaneous values of switching loss and hence different values of E_{ON} .

Thus, we can predict the dynamic behavior of a given power circuit using the new process and geometry independent ASM-GaN model for a given choice of power AlGaN/-GaN HEMT and furthermore, refine our efficiency etc calculations based on the accurate predictions given by a physically calibrated compact model. The calibrated model also allows us to see the difference in losses with and without field plates which can be used by device designers to fine tune their power HEMT's field plate designs in TCAD. This circuit design methodology can be further refined and used to predict overall performance (transient, steady-state switching etc) of other switching converter topologies. In the next chapter, we will model the package parasitics using the model card generated in this chapter as an ‘intrinsic’ component of the overall model and a parasitic lumped network as extrinsic ‘wrapper’ component around the intrinsic component, in order to create a

complete model of an AlGaN/GaN power HEMT.

4

Modeling Of Power AlGaN/GaN HEMTs: Package Parasitics*

“I do not know what I may appear to the world, but to myself I seem to have been only like a boy playing on the sea-shore, and diverting myself in now and then finding a smoother pebble or a prettier shell than ordinary, whilst the great ocean of truth lay all undiscovered before me.”

– Isaac Newton

4.1 Introduction

In this chapter, we will continue to model the Panasonic’s e-mode power AlGaN/GaN HEMT- PGA26E19BA, whose intrinsic device modeling (parameter extraction) was com-

*Note: The Verilog-A model file with name ‘asmhemt_power.va’ that was formulated, extracted and simulated in chapters 2 3 & 4 and the supporting model files for Cadence ADE simulation in Spectre simulator for power AlGaN/GaN HEMT - PGA26E19BA such as ‘nmos4.scs’ and ‘stats_include.scs’ are given in [76] and appendix. B.

pleted with threshold voltage $V_{off} \approx + 1.8$ V as extracted in previous chapter. This value of V_{off} is lower than the typical values for vertical power FETs, which have a range of 3 to 5 V's in order to prevent false operation resulting from noise[77, 78]. Thus the low value of V_{off} proves that the structure of PGA26E19BA is lateral and not vertical, because threshold voltage of lateral FETs are lower than their vertical counterparts[77].

Commercial power transistors come in packaged form in which a protective package encapsulates a given die of the device via bond wires and contact leads/pins. These contact leads/pins are further connected to other circuit components on a PCB via soldering. In order to model the package parasitics, we have used techniques which were originally developed for modeling the device parasitics of RF III-V FETs, starting with the work of Dambrine et al.[79], who used the broad-band S -parameter measurements and proposed a lumped element network around the intrinsic small-signal PI topology model of the FET (see Fig. 2.3, which is essentially a PI topology for common source biasing, but represented in a different manner on the cross-section of a power HEMT device), in order to model the gate, drain and source parasitics arising out of back-end metalization and interconnects on the die, which are termed as ‘extrinsic’ small-signal elements. Berroth & Bosch[80, 81] further perfected this work[80] and extended this model to large-signal switching applications such as digital circuits using differential resistances of the gate-to-source and gate-to drain diodes as well as the serial resistance of the feedback capacitance of a HEMT. An important aspect of such modeling is that these models are valid for a broad-band frequency range i.e. from DC up-to 5 GHz[80], but produce significant errors at higher frequencies. However, for power transistors used as a switching element in power electronic circuits, the typical switching frequencies start from few 100's of KHz and go up-to tens of MHz. We used this limited range of operation to our advantage by limiting the S -parameter measurement to a maximum frequency of 600 MHz, which according to our experience, is sufficient for modeling the package parasitics.

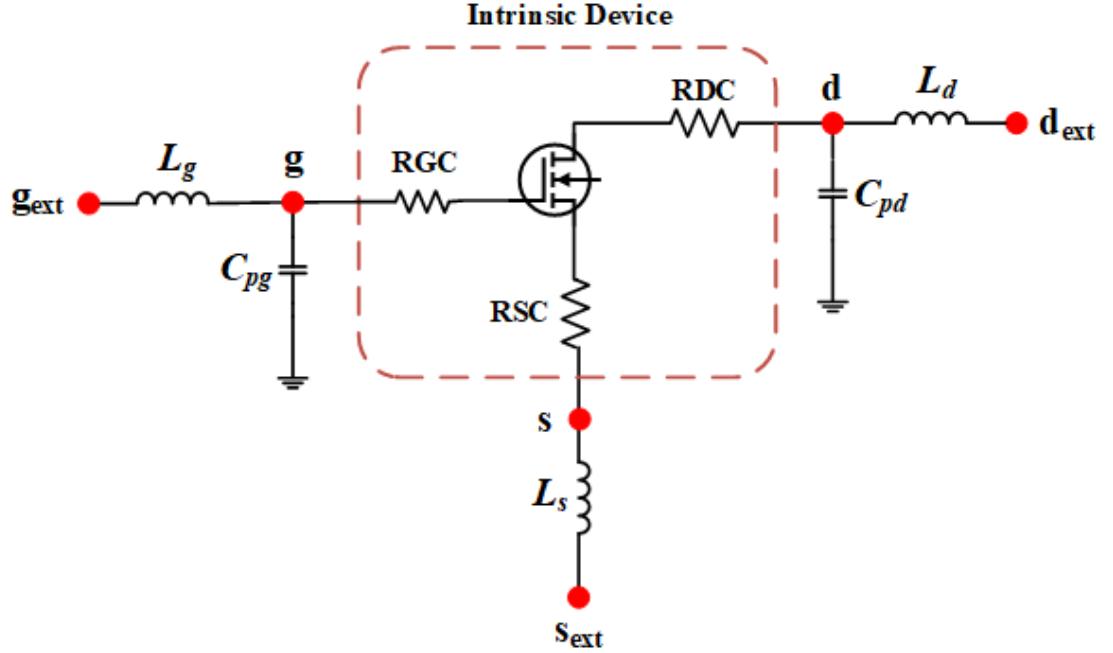


Figure 4.1: Extrinsic parasitic network due to the package around the intrinsic FET model as described in Fig. 2.3.

4.2 Model Development Of Extrinsic Parasitic Elements

Various active and passive elements of the intrinsic device model derived in chapt.2 & extracted for a Panasonic's power HEMT PGA26E19BA in chapt.3 are shown in Fig. 2.3. These elements are a part of the intrinsic FET model of a packaged device. However, in order to model a packaged device completely, we need to consider the inside picture of a packaged device. It consists of a die containing intrinsic FET device and a package surrounding it with bond wires connecting the die to external contact leads/pins of the package. This combination of package material, bond wires and external leads/pins can be modeled as a lumped network as shown in Fig. 4.1 [79–82]. Such package level modeling has been found to be quite useful in detailed analysis of high frequency switching performance of GaN power devices [75]. There are total five extrinsic (L_g , C_{pg} , L_s , L_d ,

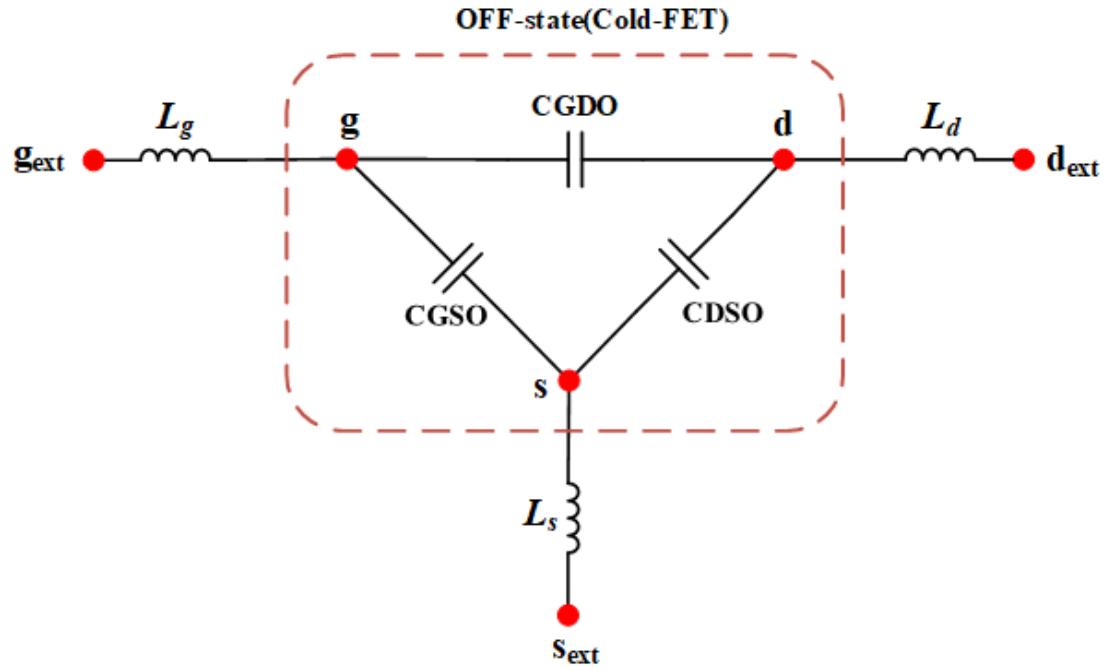
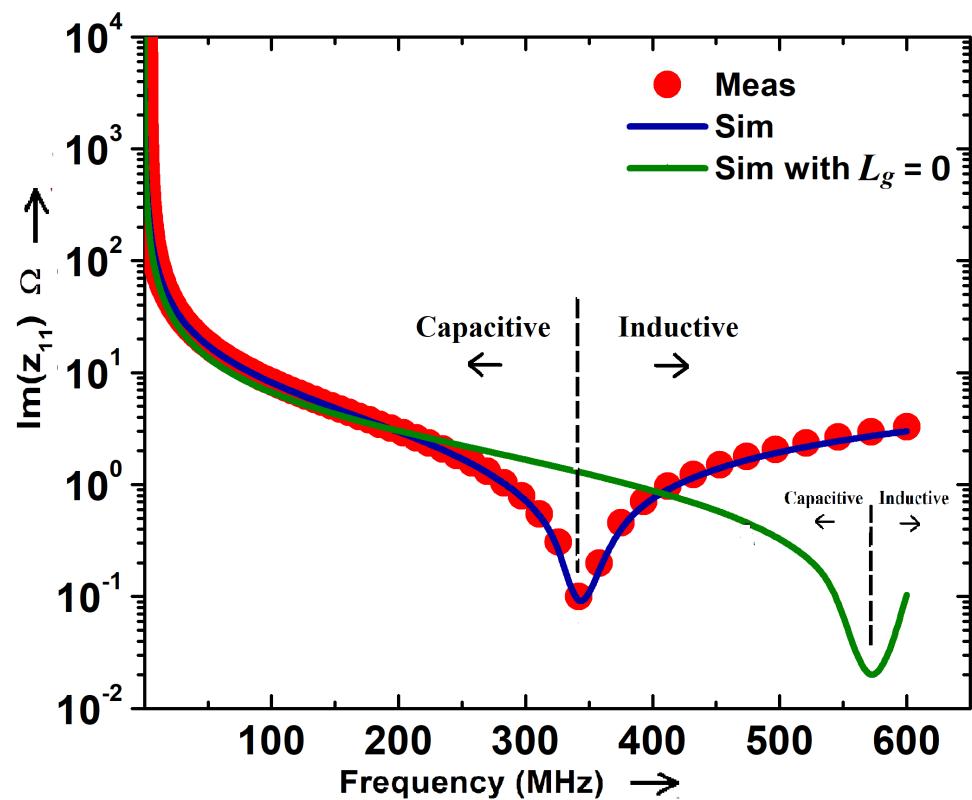
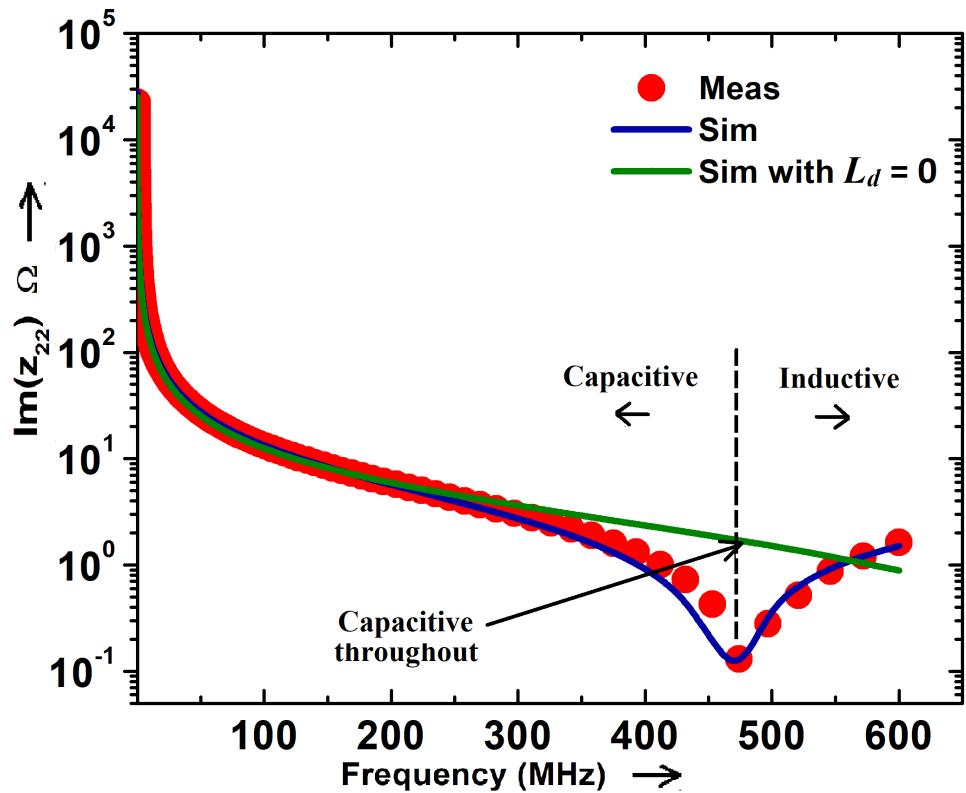


Figure 4.2: Equivalent circuit of Fig. 4.1 under OFF-state ($V_{g_{\text{ext}}s_{\text{ext}}} = V_{d_{\text{ext}}s_{\text{ext}}} = 0$ V) condition. The capitalized elements of OFF-state (Cold-FET) are all model parameters of ASM-GaN compact model.

C_{pd}) and three intrinsic elements (RGC, RSC, RDC) in the lumped network that model the gate side, source side and drain side of the equivalent model shown in Fig. 4.1.

4.3 Extraction Of Package Parasitics From OFF-State S -Parameter Measurements

As a part of our model extraction flow so far, the two intrinsic elements RSC and RDC in Fig. 4.1 have already been extracted by using them in fitting the linear region of the DC I-V characteristics as shown in chapt.3. This leaves us to extract the remaining five extrinsic elements of package and intrinsic model element RGC. In order to extract them, we measured OFF-state S -parameter measurements using the Keysight's PD-1000A measurement system with frequency sweep from 0.05 to 600 MHz. The bias condition

(a) $Im(z_{11})$ (b) $Im(z_{22})$

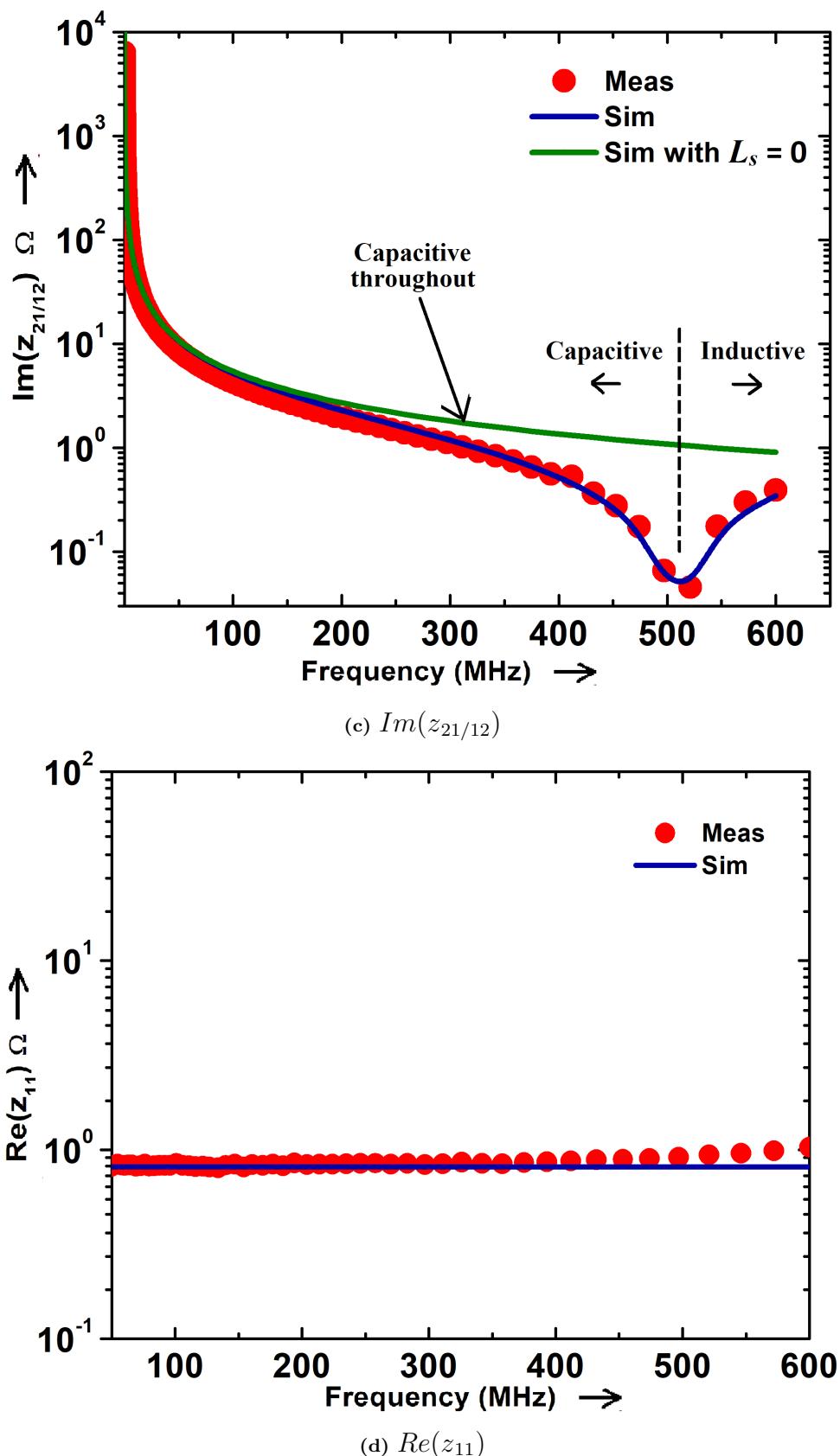


Figure 4.3: Imaginary and real parts of the measured OFF-state Z-parameters vs OFF-state model (Fig. 4.2) simulation, with semi-log scale on Y-axis and linear scale on X-axis for Panasonic's packaged GaN device PGA26E19BA.

Table 4.1: Extracted model elements of Fig. 4.1

Model Element	Extracted Value	Panasonic's Model Value
RGC ($\text{m}\Omega$)	798.8	2200
RDC ($\text{m}\Omega$)	61	96
RSC ($\text{m}\Omega$)	31	20.33
L_g (pH)	632.7	4000
L_d (pH)	616.4	2000
L_s (pH)	328.4	1500
C_{pg} (fF)	0	NA
C_{pd} (fF)	0	NA

for measurement was zero gate and drain bias ($V_{g_{\text{ext}} s_{\text{ext}}} = V_{d_{\text{ext}} s_{\text{ext}}} = 0 \text{ V}$), for which the device is in OFF-state [82]. Under such conditions, we can further approximate the model in Fig. 4.1 to one in Fig. 4.2 which shows that the three OFF-state capacitance model parameters CGDO, CGSO and CDSO are the only elements from the intrinsic FET device that contribute to the topology. Furthermore, we found that Z -parameters, as converted from measured S -parameters, are sufficient to model these measurements as shown in Fig. 4.3. In order to see how we modeled Z -parameters and extracted the five extrinsic elements, we write

$$\text{Im}(z_{11}) = \omega(L_g + L_s) - \frac{1}{\omega(\text{CGSO} + \frac{\text{CGDO} \cdot \text{CDSO}}{\text{CGDO} + \text{CDSO}})}, \quad (4.1a)$$

$$\text{Im}(z_{21/12}) = \omega(L_g + L_d) - \frac{1}{\omega(\text{CGDO} + \frac{\text{CGSO} \cdot \text{CDSO}}{\text{CGSO} + \text{CDSO}})}, \quad (4.1b)$$

$$\text{Im}(z_{22}) = \omega(L_d + L_s) - \frac{1}{\omega(\text{CDSO} + \frac{\text{CGSO} \cdot \text{CGDO}}{\text{CGSO} + \text{CGDO}})}. \quad (4.1c)$$

In the above expressions capacitances C_{pg} and C_{pd} have been neglected because we found that while tuning the model to imaginary parts of various OFF-state Z -parameters, the

required values for C_{pg} and C_{pd} were zero (see Table. 4.1). This is because we already extracted all the ON and OFF state capacitances from C-V measurements as discussed in detail in previous chapter. Therefore in our modeling methodology, we are implicitly including the effects of C_{pg} and C_{pd} as a part of the capacitance network as shown in Fig. 4.2. In order to extract the three extrinsic inductances, we used the imaginary part of Z-parameters viz. z_{11} (Fig. 4.3a), z_{22} (Fig. 4.3b) and $z_{21/12}$ (Fig. 4.3c) which exhibit resonance at a particular frequency which is determined by tuning the values of these extrinsic inductance elements. Analytically, these resonant frequencies can be found by equating all the three imaginary parts of Z-parameters given in (4.1) to zero. After tuning of these three inductances in simulation, it was found that resonance in $Im(z_{11})$ is governed by a combination of L_g and L_s as indicated by (4.1a), resonance in $Im(z_{22})$ by a combination of L_d and L_s as indicated by (4.1b) and resonance in $Im(z_{21/12})$ by a combination of L_g and L_d as indicated by (4.1c). In order to see the sensitivity of these parasitic package inductances, we have also plotted the simulated imaginary values of Z-parameters by setting the key controlling inductance for the corresponding imaginary part to zero in Fig. 4.3a, Fig. 4.3b and Fig. 4.3c. Thus, it can be seen that inductance L_g is the key element affecting $Im(z_{11})$, L_d is the key element affecting $Im(z_{22})$ and L_s is the key element affecting $Im(z_{21/12})$.

At this stage, it can be noted that the intrinsic FET model as shown in Fig. 2.3, which was extracted in detail in previous chapter (chapt.3), has modeled both the linear (RSC and RDC) and non-linear (R_{accs} and R_{accd}) components of source and drain resistances respectively. The only element remaining to be extracted now is the gate resistance RGC. It was extracted from the $Re(z_{11})$, which is given by (see Fig. 4.1 with internal transistor replaced by Fig. 2.3)

$$Re(z_{11}) = RGC + RSC + R_{accs}. \quad (4.2)$$

Thus, we were able to get the value of RGC by tuning its value in simulation of $Re(z_{11})$

as shown in Fig. 4.3d. The extracted value of RGC is 798.8 mΩ which closely matches the one given in data-sheet [68] which is 800 mΩ. The final values for all the eight intrinsic and extrinsic elements of the overall model in Fig. 4.1 are given in Table. 4.1, where we have compared the extracted values with Panasonic’s values (which they have used in their sub-circuit model [83]). It was found that except for drain and source resistances (RDC and RSC), whose values are of same order as those of Panasonic’s and the nil values of C_{pg} and C_{pd} which make no impact on the model (i.e., they can be taken out of the overall model of Fig. 4.1), all the other extracted model element values deviate from those given in Panasonic’s model by at-least an order. This highlights the importance of modeling a packaged power transistor based on various measurements rather than using an estimated model given by vendors.

4.4 Conclusion

This completes the modeling of a power AlGaN/GaN HEMT device with re-formulated ASM-GaN model. In chapt.2, a physically-oriented hybrid model which does not need detailed geometry and process information about the device was formulated around the typical cross-section of a III-V power HFET/HEMT. A systematic parameter extraction flow was proposed and executed for modeling the DC I-V and C-V characteristics in chapt.3. The resultant intrinsic device model, composed of I-V and C-V models that preserve the key benefits of physics-based models, was then used to demonstrate a power electronic circuit design with DC-DC boost converter as an example. In chapt.4, the parasitic effects associated with device package were modeled with an equivalent lumped element model. An extraction flow for lumped model elements was then established using the OFF-state (Cold-FET) S -parameter measurements. Thus, the final model is a combination of intrinsic (HFET) and extrinsic (package) models. Furthermore, using

the model parameters from tables 3.1, 3.2 & 4.1, we created the final model card for the device PGA26E19BA, which has been used as a base for further simulation and modeling studies such as modeling of OFF-state C_{oss} losses in chapt.5 and statistical modeling in chapt.6. The final model card of device PGA26E19BA is given in [76] and appendix. B.

5

Modeling Of Large-Signal OFF-State Losses In Power AlGaN/GaN HEMTs*

“The greatest enemy of knowledge is not ignorance, it is the illusion of knowledge.”

– Stephen Hawking

5.1 Introduction

*Note: The C_{oss} loss model for power AlGaN/GaN HEMT - PGA26E19BA created in this chapter can be retrieved from the overall model card (B.1) by choosing the section ‘coss_loss’ from the include file ‘stats_include.scs’ (B.2) and further editing the Verilog-A file ‘asmhemt_power.va’[76] to add the simple equations for ESR and *NLESR* models formulated in this chapter. Although ‘coss_loss’ is not a statistical corner, still we have created this special corner (section) in order to make the model code unified & simple.

IT has been observed in various studies[33,84–86,88] that when certain commercial power transistors were operated in OFF-state under large-signal operation such as in DC-DC or DC-AC power converters, the measured losses exceeded the amount that would have been expected from a transistor in OFF-state (ideally zero). Sawyer-Tower measurement setup[89] as shown in Fig. 5.1, is an excellent tool to characterize these additional OFF-state losses occurring across the OFF-state output capacitance C_{oss} of a power transistor[84–88]. The key advantage of this set-up over traditional C-V meter is that in Sawyer-Tower setup, more realistic measurements are performed on the output large-signal charge transients and the corresponding energy losses. Thus these measurements are a better representative of real power electronic applications when compared with small-signal measurements from C-V meters. In [84,85], these OFF-state losses have been studied in detail using Sawyer-Tower setup for various commercial power GaN HEMTs, where it is shown that they are due to hysteresis that occurs in the V_{DS} vs Q_{oss} characteristics measured across the output capacitance in OFF-state.

The reported energy losses for Panasonic's power GaN HEMT - PGA26E19BA measured in [84,85] are in the range of sub- μ J's per switching cycle, which can easily translate to several tens of Watts of power dissipation in C_{oss} at HF/VHF (3 MHz - 300 MHz) switching frequencies. This in turn can severely deteriorate the efficiencies of well designed DC-DC or DC-AC power converter circuits that utilize HF/VHF switching frequencies in order to minimize the size of passives, along-with large size power devices in order to reduce ON-state conduction losses (via corresponding reduction in R_{on})[84,87].

Similar OFF-state hysteretic energy losses in C_{oss} have been reported for superjunction power MOSFETs[86,87] and SiC power MOSFETs and diodes[88]. This necessitates detailed simulation study and modeling of this phenomenon. In the chapters 2, 3 & 4, we presented a package level model for the same device (PGA26E19BA) using model extraction based on C-V, I-V and OFF-state S-parameter measurements and hence

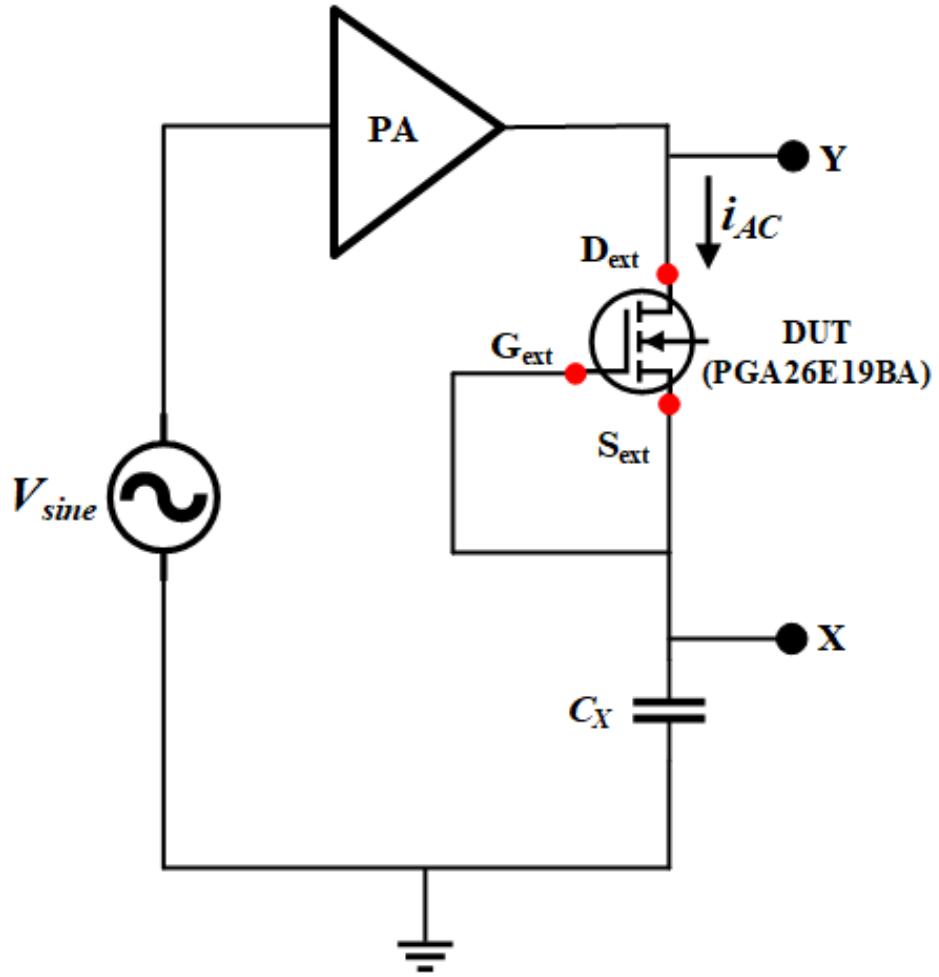


Figure 5.1: Sawyer-Tower setup for measuring/simulating the V_{DS} vs Q_{oss} characteristics.

chose this device for further analysis of its OFF-state losses; so as to gain a complete understanding of modeling a power HEMT, with possibility to model other power HEMTs in a similar manner. The newly implemented formulation in ASM-GaN (chapt.2) does not need proprietary foundry parameters such as geometry and device cross section details as its inputs, yet it maintains its surface potential and drift-diffusion based framework intact. We used the calibrated model of PGA26E19BA using a model card created with model parameters extracted in tables 3.1, 3.2 & 4.1 (see [76] and appendix. B) to study and model the hysteretic losses measured using Sawyer-Tower setup in [84, 85]. However, the sample which was used in [84, 85] is different and hence required some re-calibration in

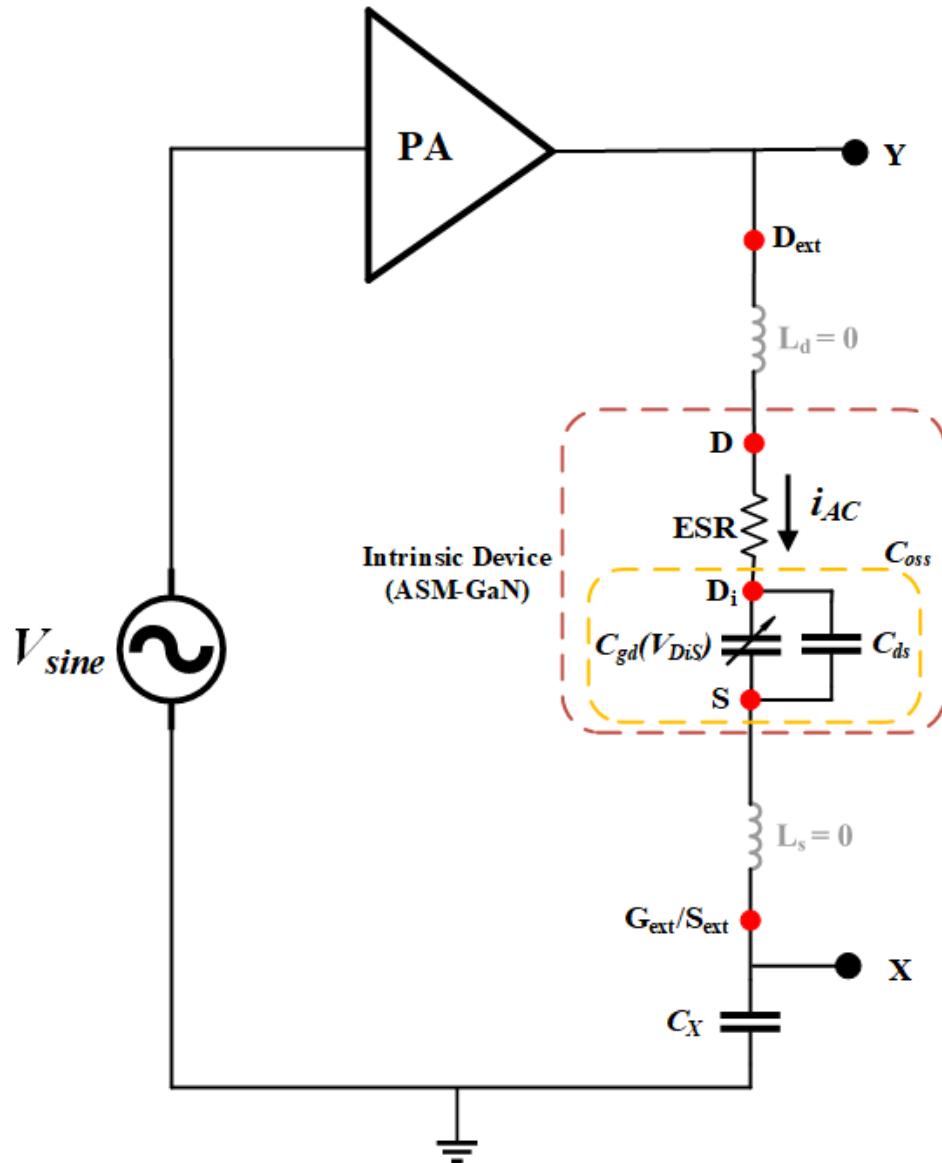
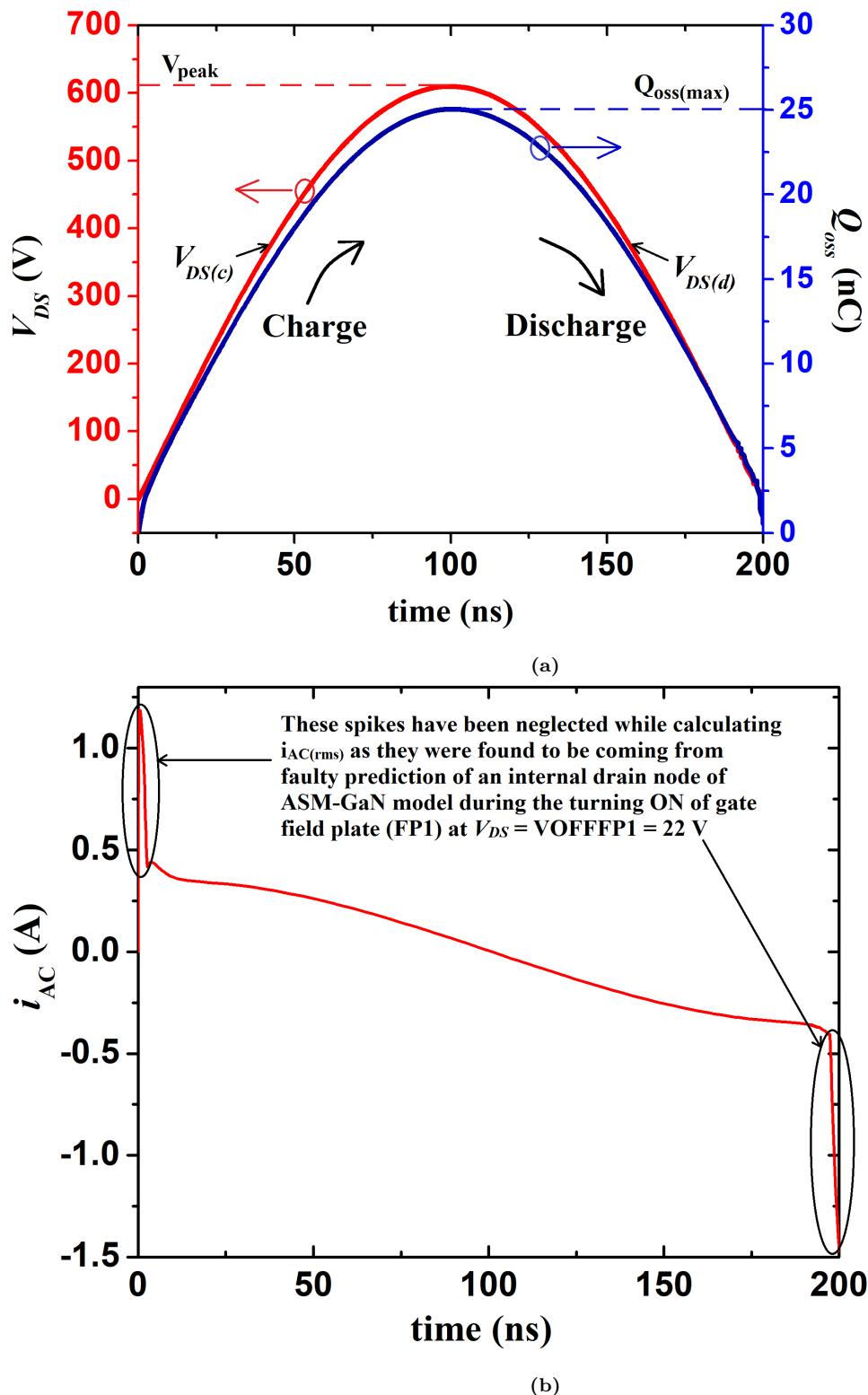


Figure 5.2: Physics oriented ASM-GaN package model without package inductances (because of no ringing in the measured data shown in Fig. 5.3c) with addition of ESR in series with C_{oss} for the Sawyer-Tower setup shown in Fig. 5.1.

model parameters (the re-calibrated model parameters can be retrieved from the special corner ‘coss_loss’ from the include file ‘stats_include.scs’ in B.2) which will be explained later in section 5.3.

A couple of solutions have been developed to model the hysteretic losses in C_{oss} . One



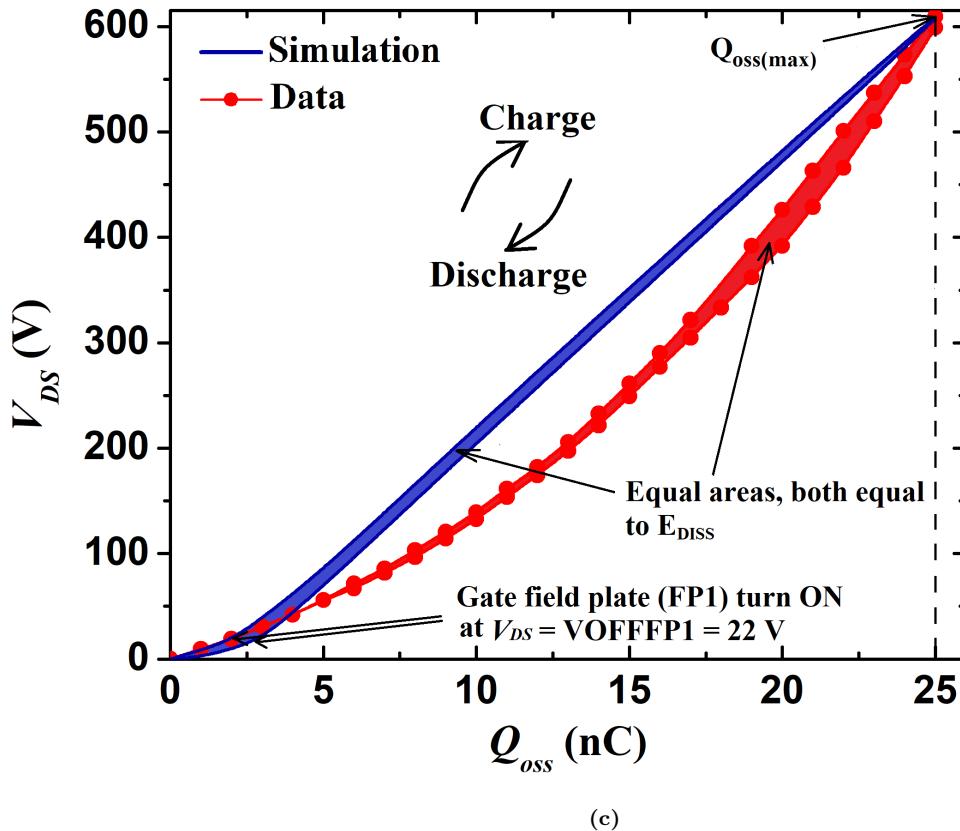


Figure 5.3: (a) Simulated transient waveform for V_{DS} and Q_{oss} with $f_{sine} = 5$ MHz and $V_{peak} = 610$ V, (b) corresponding simulated transient waveform for i_{AC} & (c) corresponding simulated V_{DS} vs Q_{oss} plot as derived from Fig. 5.3a vs data measured in [84, 85] for the power GaN HEMT - PGA26E19BA. Each shaded area for measured and simulation is equal to $0.3 \mu\text{J}$.

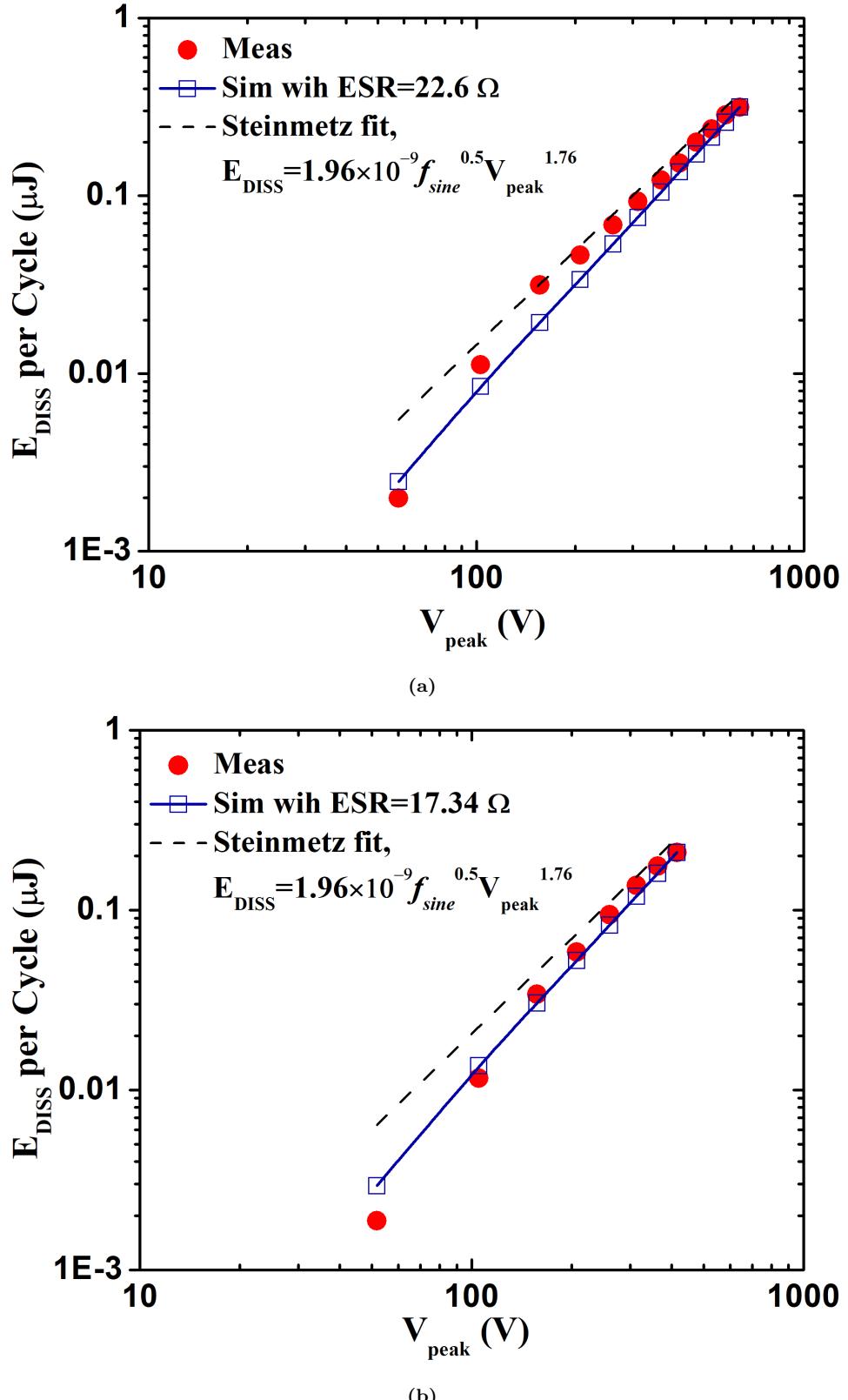


Figure 5.4: (a) Plot for E_{DISS} per cycle using Sawyer-Tower measurements from [85] and simulation model of Fig. 5.2 with linear ESR and corresponding Steinmetz fit vs peak value of sinusoidal voltage across the device (V_{peak}) for $f_{\text{sine}} = 5 \text{ MHz}$ of input large-signal source V_{sine} & (b) same plot for $f_{\text{sine}} = 10 \text{ MHz}$. Note that at lower peak voltages, the measurements for E_{DISS} are not that accurate[85]. We extracted the ESR values till $f_{\text{sine}} = 35 \text{ MHZ}$ in a similar way. The extracted ESR vs frequency plot is shown in Fig. 5.5.

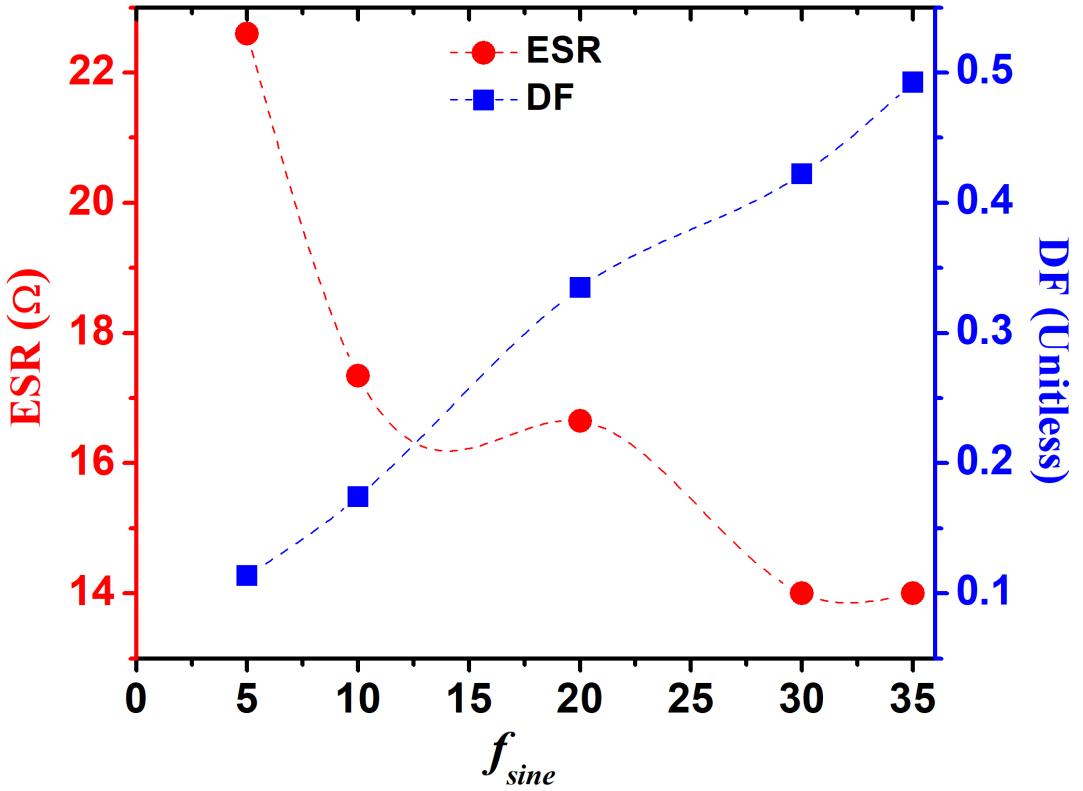


Figure 5.5: Plot of extracted ESR & dissipation factor ($DF = \tan(\delta)$) at $V_{DS} = 0$ V vs sinusoidal excitation frequency f_{sine} of input large-signal source V_{sine} .

such approach in [88] uses an extra capacitance term derived from the Steinmetz equation for the hysteretic energy loss per switching cycle - E_{DISS} , which can be expressed as (by neglecting the frequency dependent term)[88]

$$E_{DISS} = \int_0^{V_{peak}} C_{EXTRA}(V_{DS}) \cdot V_{DS} dV_{DS} = k \cdot V_{peak}^{\beta} \quad (5.1a)$$

where,

$$C_{EXTRA}(V_{DS}) = \beta k V_{DS}^{\beta-2}. \quad (5.1b)$$

The above formulation results in a sub-circuit implementation[88], which can be easily used in simulating power electronic circuits. However, this approach doesn't give a detailed mechanism of the losses occurring in the capacitor C_{oss} . Another approach models the V_{DS} vs Q_{oss} characteristics using non-linear ESR(*NLESR*)[90]. This approach, how-

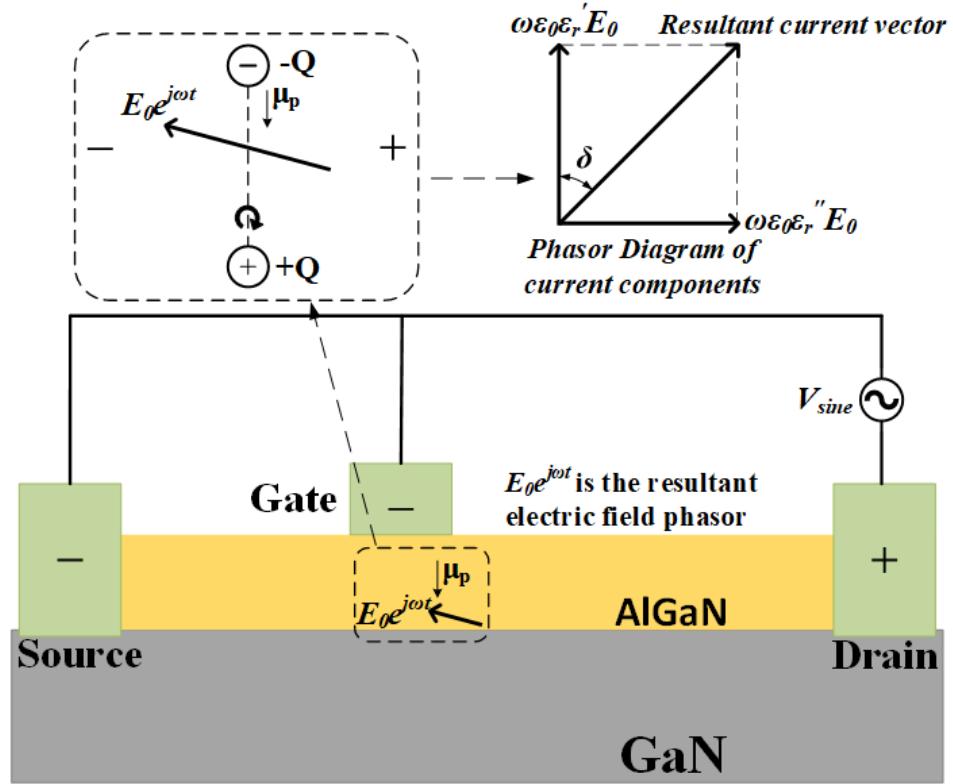
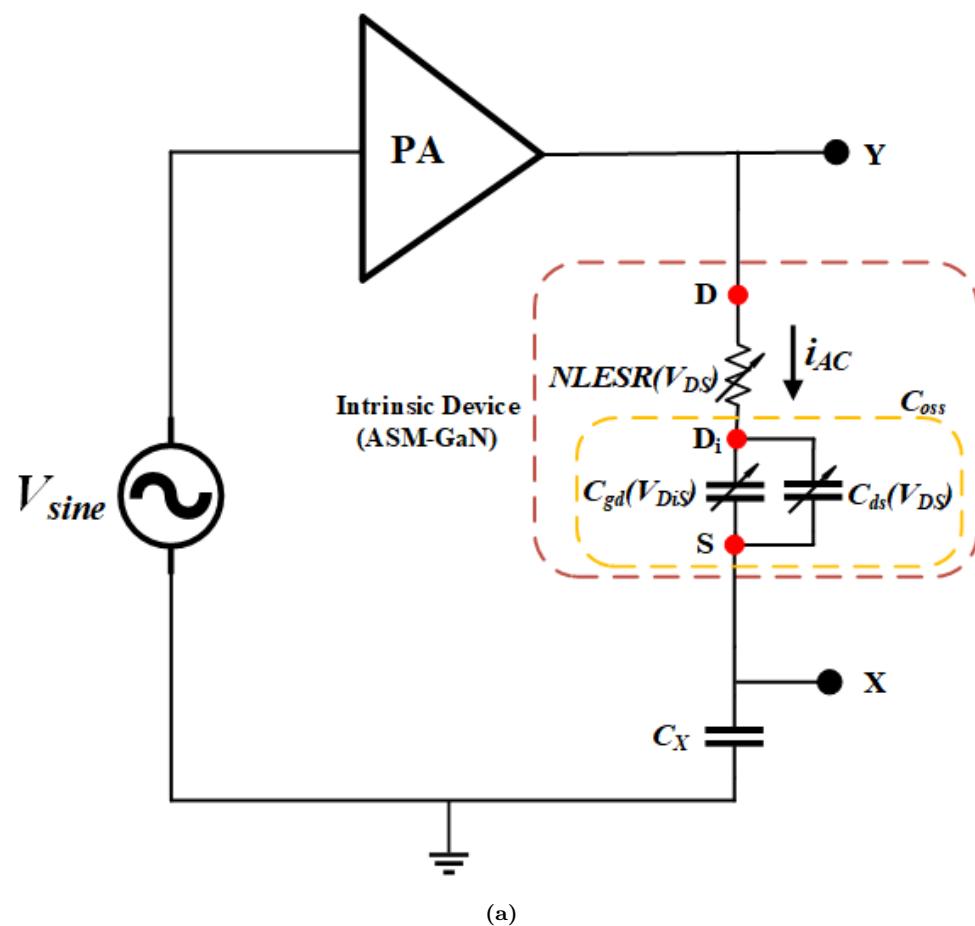


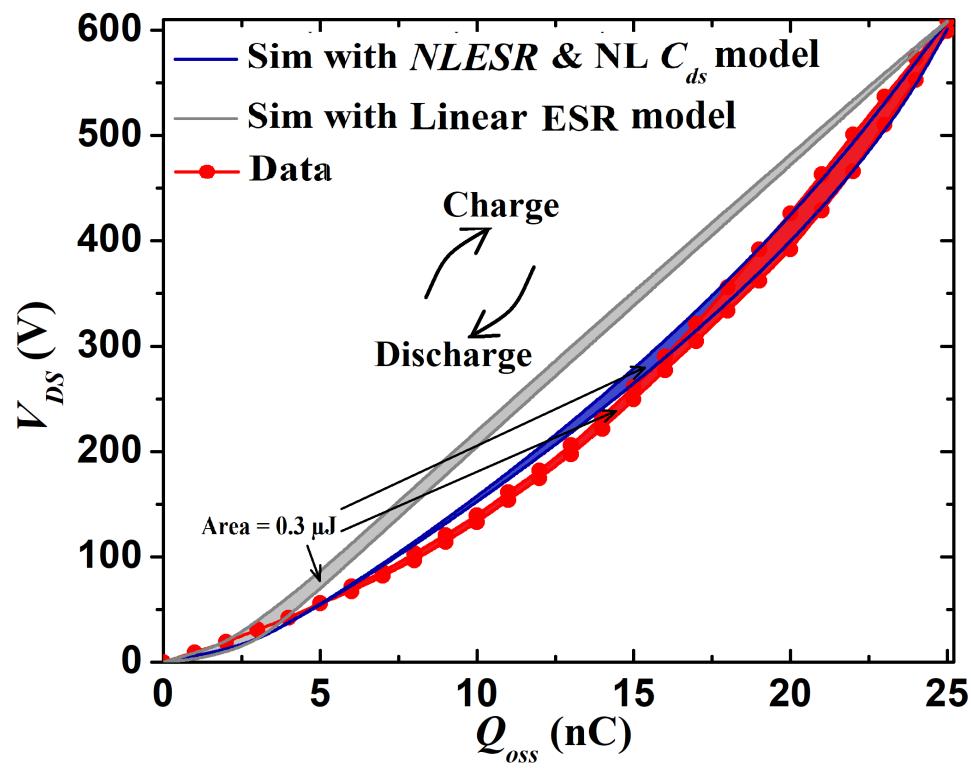
Figure 5.6: Schematic of an OFF-state GaN HEMT device in Sawyer-Tower setup at an instant when the drain terminal is positive w.r.t source and gate terminals showing the origin of dielectric losses in output capacitance C_{oss} . It shows that the losses occur due to the rotation of permanent dipoles, each with an average dipole moment μ_p . This results in two current components, first the lossy capacitor current aligned along the applied electric field and another the ideal capacitor current ahead by $\pi/2$ radians, which results in a resultant current vector (phasor) lagging behind the ideal capacitor current by an angle δ . The dissipation factor (DF) is a circular tangent function of this δ .

ever, results in an equation for $NLESR$ with an abrupt change at a particular applied bias, where $NLESR$ reaches a maximum value. Such abrupt formulation is generally avoided in formulating compact models because of potential convergence issues.

This chapter is organised as follows. In section 5.2 we describe the general method of calculating the OFF-state energy losses across C_{oss} using Sawyer-Tower method. Sections 5.3 & 5.4 present two models which model the frequency and bias dependent behavior of



(a)



(b)

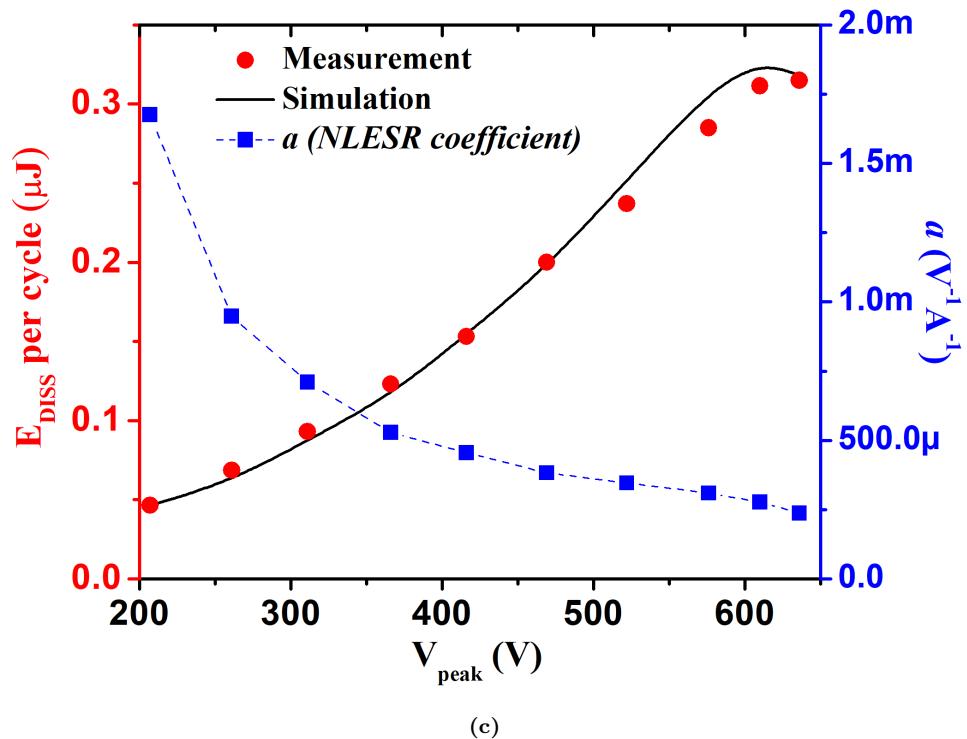


Figure 5.7: (a) Sawyer-Tower setup with equivalent model of DUT's C_{oss} using *NLESR* in conjunction with non-linear C_{ds} , both modeled as a function of applied drain to source voltage V_{DS} , (b) corresponding V_{DS} vs Q_{oss} plot with areas and shapes under hysteresis matching for both data and simulation ($= 0.3 \mu\text{J}$) & (c) corresponding plot for E_{DISS} per cycle using Sawyer-Tower measurements from [84] vs V_{peak} at $f_{sine} = 5 \text{ MHz}$.

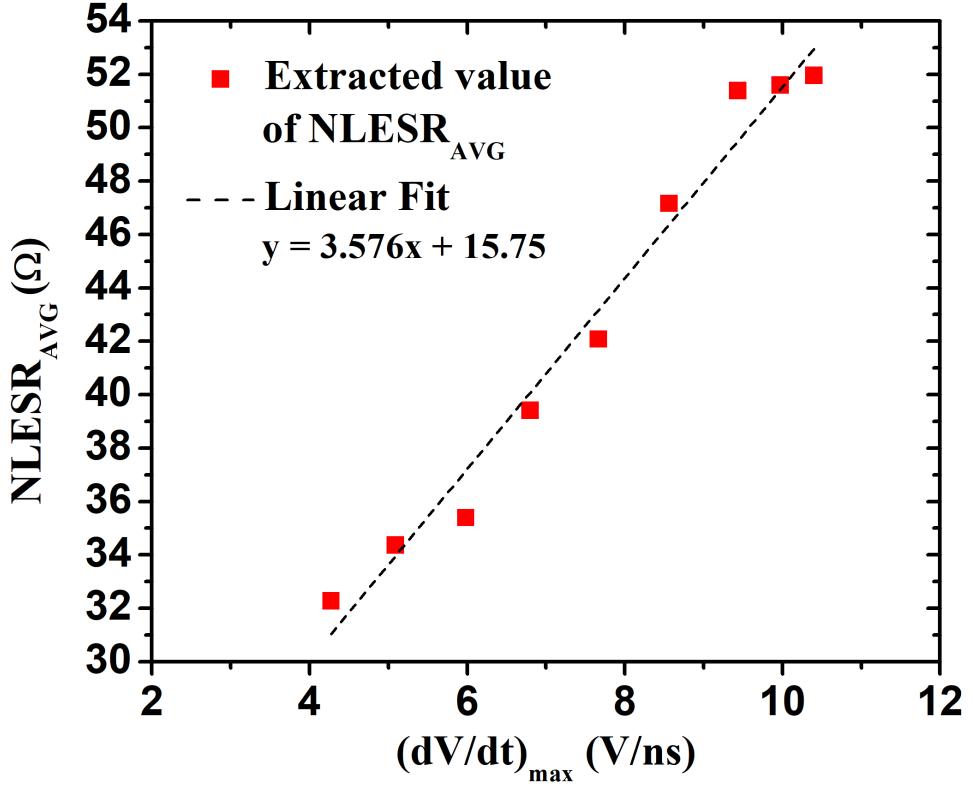


Figure 5.8: A plot of extracted value of $NLESR_{AVG}$ vs $(dV/dt)_{\max}$ of V_{DS} waveform, thus proving that the average value of $NLESR$ is a linear function of maximum dV/dt of the applied waveform across C_{oss} .

energy losses due to hysteresis in the output capacitance C_{oss} of the device PGA26E19BA. The first model captures the hysteretic energy loss with a linear effective series resistor (ESR) in series with C_{oss} . The linear resistor model is found to be simple, well grounded in its physical interpretation and reasonably accurate model for modeling the energy loss per cycle at multiple peak voltages (V_{peak}) and frequencies (f_{sine}). However, this model has a shortcoming in capturing the exact shape of the hysteresis curve. In order to capture it, we propose another approach which uses a non-linear ESR ($NLESR$) and an extra non-linear term in the output capacitance component C_{ds} . It is seen that this approach can also model the energy loss per cycle for multiple V_{peak} 's and frequencies. In section 5.5, we analyse our results in the light of some new work in this area, summarize the key differences between the two models, and furthermore, compare the C_{oss} vs V_{DS}

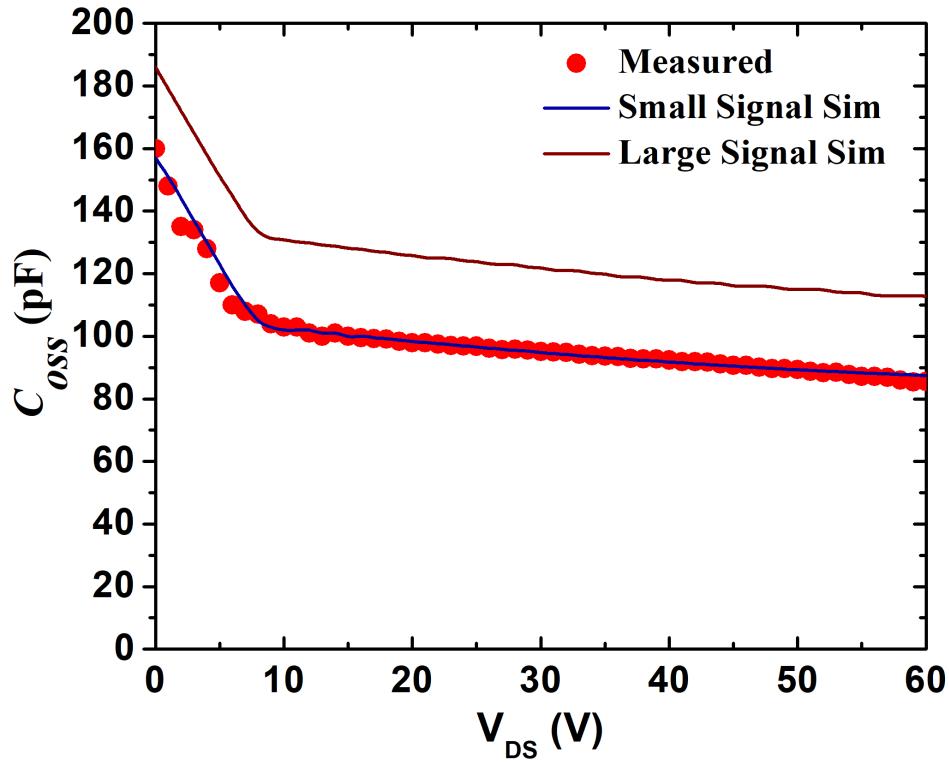


Figure 5.9: Plot of C-V meter based measured and modeled C_{oss} vs V_{DS} from the small-signal model in chapt.3 with large-signal, *NLESR* and non-linear C_{ds} based model.

characteristics obtained using *NLESR* & non-linear C_{ds} based large-signal model with the small-signal model already measured and modeled in chapt.3 and [67]. Finally, section 5.6 concludes the work.

5.2 C_{oss} Loss Calculation Using Sawyer-Tower Method

As a large-signal is applied to the drain terminal of the DUT (device PGA26E19BA), the voltage developed across terminals Y and X in Fig. 5.1 is the same as that across the external drain and source terminals of the device. The charge Q_{oss} across the non-linear capacitor C_{oss} is given by the corresponding charge accumulated across ideally loss-less linear capacitor C_X (where $C_X \gg C_{oss}$ in order to ensure that their series combination

is effectively dominated by capacitor C_{oss}) i.e.

$$Q_{oss} = V_X \cdot C_X \quad (5.2a)$$

&

$$V_{(DS)ext} = V_{YX}. \quad (5.2b)$$

The charging and discharging of a non-linear capacitor such as C_{oss} shows an asymmetry in the voltage measured across the capacitor ($V_{(DS)ext}$) when a large-signal sinusoidal voltage source V_{sine} is applied across the DUT in Fig. 5.1. This has been verified by plotting measured $V_{(DS)ext}$ as a function of time or Q_{oss} for various power devices in [84–86,88,90]. If $V_{(DS)ext(c)}$ and $V_{(DS)ext(d)}$ represent the charging and discharging voltages of the capacitor C_{oss} respectively, while $E_{oss(c)}$ and $E_{oss(d)}$ are the corresponding energies required to charge and discharge the output capacitor C_{oss} , then

$$\begin{aligned} E_{DISS} &= E_{oss(c)} - E_{oss(d)} \\ &= \int_{Q_i}^{Q_f} V_{(DS)ext(c)} dQ_{oss} - \int_{Q_i}^{Q_f} V_{(DS)ext(d)} dQ_{oss}, \end{aligned} \quad (5.3)$$

where Q_i is initial charge on the capacitor which is found to be zero under steady state measurements done in [84, 85] for the device PGA26E19BA and Q_f is the final charge corresponding to the peak sinusoidal voltage V_{peak} . Note that one cycle refers to a fully rectified sinusoid which is applied by the Power Amplifier (PA) in Fig. 5.1.

Fig. 5.2 shows the Sawyer-Tower simulation setup with the package level model of device PGA26E19BA as derived from previous three chapters, replacing the DUT in Fig. 5.1. We used the model without package inductances due to the absence of low voltage ringing in the measured data[84,85]. Hence we can replace $V_{(DS)ext}$ by V_{DS} here after. The non-linear capacitor $C_{oss}(V)$ is itself composed of the OFF-state linear capacitance C_{ds} and non-linear capacitance $C_{gd}(V)$. In order to model the lossy behavior of C_{oss} and the fact that the measured voltage developed across the output capacitor is asymmetrical as

discussed earlier, we added an ESR[91] in series with C_{oss} as shown in Fig. 5.2, inside the Verilog-A code of ASM-GaN. A series combination of R and C can model the asymmetry in the drain to source voltage and the corresponding energy dissipation across the series resistor due to rms current $i_{AC(rms)}$ can model the energy losses across the capacitor i.e.

$$E_{DISS} = \frac{i_{AC(rms)}^2 \cdot ESR}{f_{sine}}. \quad (5.4)$$

Another way of looking at (5.4) is to consider what happens when a non-linear capacitor such as C_{oss} charges from $V_{D_iS} = 0$ V to a voltage of $V_{D_iS} = V_{max}$ through a series resistor ESR as shown in Fig. 5.2. The energy dissipation occurs at ESR with a charging current of $i_{AC} = C_{oss} \frac{dV_{D_iS}}{dt}$. Thus, we get an alternate expression for E_{DISS} as[97]

$$E_{DISS} = 2 \cdot ESR \left(\frac{dV_{D_iS}}{dt} \right) \int_0^{V_{max}} C_{oss}^2 dV_{D_iS}. \quad (5.5)$$

The factor of 2 in (5.5) comes from the assumption that the waveform of V_{D_iS} is approximately symmetrical around the charging (to V_{max}) and discharging (from V_{max}) of the capacitor $C_{oss}(V_{D_iS})$, due to which energy loss during charging and discharging are same, although in reality, it can not be so because the total voltage developed across the DUT (V_{DS}) is itself asymmetrical as shown in Fig. 5.3a. In practice, due to the asymmetry of the voltage wave-forms, the losses will be different with an energy loss per cycle given by the expression

$$E_{DISS} = ESR \left[\left(\frac{dV_{D_iS(c)}}{dt} \right) \int_0^{V_{max}} C_{oss}^2 dV_{D_iS(c)} + \left(\frac{dV_{D_iS(d)}}{dt} \right) \int_{V_{max}}^0 C_{oss}^2 dV_{D_iS(d)} \right], \quad (5.6)$$

where $\frac{dV_{D_iS(c)}}{dt}$ & $\frac{dV_{D_iS(d)}}{dt}$ are the rate of change of the voltage across C_{oss} during charging and discharging periods respectively. (5.6) can be evaluated during circuit simulation by evaluating $i_{AC(rms)}$ during one charge-discharge cycle from the steady-state waveform of i_{AC} as shown in Fig. 5.3b and then plugging that value back in (5.4), thus avoiding the complex evaluation routine required for (5.6) in simulation. This is how E_{DISS} was

calculated in our simulation study for the linear ESR model as described in section 5.3. For the non-linear ESR model of section 5.4, we used the area under the curve of the V_{DS} vs Q_{oss} characteristics as shown in Fig. 5.3c plotted from the time-domain, steady-state wave-forms in the transient simulation. It must be noted here that both the methods for calculating the energy losses in the simulation give the same results, with the choice based on the target characteristics to be modeled. Based on preceding discussion and how we model the ESR in detail, we now describe the two different models in the sections below.

5.3 Linear ESR Model

In this model, we used a constant value of ESR and simulated the setup of Fig. 5.2 for various V_{peak} 's and f_{sine} 's to model the corresponding data measured in [84, 85]. Fig. 5.3 shows the results for sinusoidal peak voltage of $V_{peak} = 610$ V and $f_{sine} = 5$ MHz. We found that we had to reduce both the OFF-state model parameters CGDO and CDSO (which determine the final C_{oss} in the model) of the calibrated model for device PGA26E19BA (see Table. 3.2) by 11 % in order to model the $Q_{oss(max)}$ as shown in Fig. 5.3c (this can be seen in the model card given in listing B.1 by choosing the section “coss_loss” from the include file “stats_include.scs” given in listing B.2). This variation between the model parameters might be due to package to package variation in addition to die to die variation between the two different specimens of the same device PGA26E19BA, measured in [84, 85] and in chapters 3 & 4. Using a constant valued ESR in the simulation for different V_{peak} 's and sinusoidal excitation frequencies f_{sine} , we were able to model the energy dissipation (E_{DISS}) measurements done electrically using Sawyer-Tower setup in [84, 85] by the $i_{AC(rms)}$ method described earlier in the section 5.2. The maximum frequency in these measurements was limited to 35 MHz by the bandwidth limitation of the PA used in [84]. Fig. 5.4 shows model results obtained by using linear ESR model for frequencies

Table 5.1: Table showing calculated values of $\tau = \text{ESR} \cdot C_{oss}$ for different frequencies at $V_{DS} = 0$ V

f_{sine} (MHz)	τ (ns)
5	3.616
10	2.774
20	2.664
30	2.24
35	2.24

of 5 MHz and 10 MHz. We were able to extract different ESR's by doing this exercise for frequencies till 35 MHz. Note that at lower peak voltages, measurement inaccuracies can be considerable as the energy is in the order of sub- μ J's[84].

Fig. 5.5 shows the plot of extracted ESR and dissipation factor ($\text{DF} = \tan(\delta) = \omega \cdot \text{ESR} \cdot C_{oss}$), with the value of C_{oss} taken at $V_{DS} = 0$ V, as a function of sinusoidal frequency f_{sine} . It shows that ESR is a complex function of frequency as opposed to having an inverse dependence on frequency, which is expected for a lossy linear capacitor with a constant DF. It also shows an increasing trend for DF which can be explained by the standard dielectric loss model of a capacitor.

Fig. 5.6 shows a physical interpretation of the linear ESR model according to the standard theory of dielectric absorption. The applied large-signal sinusoidal voltage across C_{oss} develops a sinusoidal electric field which can be expressed at any point in the semiconductor layer (AlGaN, GaN or any insulating layer present) as an electric field phasor $E_0 e^{j\omega t}$. The permanent electric dipoles which are present in the compound semiconductor layers such as AlGaN or GaN can be attributed to the presence of spontaneous and piezoelectric polarizations[92]. If we assume that the resultant electric field acts on dipoles each with an average dipole moment μ_p , then it can be shown[93] that the dipoles experience a torque and hence rotate in response to the applied alternating electric field. This rotation

results in an expenditure of energy contained in the electric field as heat. This heat loss manifests itself as the hysteresis loss as measured in the Sawyer-Tower setup. The rotated dipoles take an average time of τ s before they return back to their original positions. It is this characteristic time constant (also called as dipole relaxation time constant) that is modeled by the linear ESR as (see chapter 3, problem no. 3.3 of [93])

$$\tau = \text{ESR} \cdot C_{oss} \quad (5.7)$$

Table. 5.1 shows various values of τ calculated with C_{oss} taken at $V_{DS} = 0$ V for different sinusoidal excitation frequencies using (5.7). The mean value of τ is 2.707 ns, which results in a characteristic angular frequency $\omega_\tau = \frac{1}{\tau}$ of 369.41 MHz. This characteristic frequency (58.79 MHz when expressed as $f_{\sin\tau}$) corresponds to a frequency at which the imaginary part of the dielectric constant (ε_r'') reaches its peak (i.e the dielectric losses also reach their peak) and the real part (ε_r') reduces to half its value at very low frequencies[93]. Using this τ , capacitor C_{oss} can further be modeled as the standard Cole-Cole equivalent model of a capacitor showing dielectric absorption[94].

5.4 Non-Linear ESR & C_{ds} Model

The linear ESR model that was described in previous section could model the area under hysteresis in the V_{DS} vs Q_{oss} characteristic but couldn't model the location of bulge and the concave curvature (see Fig. 5.3c). We were able to get this concave curvature in the measured data by introducing a non-linearity in the C_{ds} component of the capacitor C_{oss} as (this non-linearity is in addition to the already existent bias dependence of capacitor C_{gd} which is used to model C_{iss} in chapt.3)

$$C_{ds} = \text{CDSO} - \text{CDSL} \cdot V_{DS}, \quad (5.8)$$

where CDSO [F] is the drain to source OFF-state capacitance parameter and CDSL [F V^{-1}] is its first order voltage coefficient. In order to model the E_{DISS} using the method of calculating the area under simulated V_{DS} vs Q_{oss} characteristics as already explained in the section 5.2, we had to scale the value of model parameter CDSO extracted in Table. 3.2 by 1.522 and extracted the value of CDSL to be 30×10^{-15} , thus making the large-signal C_{oss} greater than its small-signal counterpart as shown in Fig. 5.9. The model fit for $V_{\text{peak}} = 610 \text{ V}$ & $f_{\text{sine}} = 5 \text{ MHz}$ is shown in Fig. 5.7b with superposition from simulation with linear ESR model, which shows a considerable improvement in the simulated shape (concave curvature). Furthermore, in order to shift the simulated bulge in the hysteresis area at lower voltages (in Fig. 5.3c) towards higher voltages as shown in Fig. 5.7b, we had to introduce a non-linearity in the ESR as a function of the drain to source voltage V_{DS} using following equation

$$NLESR(V_{DS}) = a \cdot V_{DS}^n, \quad (5.9)$$

where a [$\text{V}^{-1}\text{A}^{-1}$] is the coefficient of $NLESR$ and n [unitless] is the exponent of power function. This resulted in shift of the bulge at lower V_{DS} for linear ESR model to higher V_{DS} in the simulation as shown in Fig. 5.7b. For $V_{\text{peak}} = 610 \text{ V}$ & $f_{\text{sine}} = 5 \text{ MHz}$, we extracted the values of a and n equal to 2.77×10^{-4} and 2 respectively. The above formulation in ASM-GaN code was run on two commercially available simulators - ADS and Spectre and we found no convergence issues due to the smooth formulation of $NLESR$ in (5.9), without any abrupt change as in [90], which uses an abrupt formulation in $NLESR$ without non-linear C_{ds} .

Since the exponent of V_{DS} in (5.9) is 2, it can be concluded that at a given instant, $NLESR$ is proportional to the power content of the applied signal. Fig. 5.7c shows the modeling of E_{DISS} per cycle as a function of V_{peak} for $f_{\text{sine}} = 5 \text{ MHz}$ and the corresponding variation in the $NLESR$ coefficient a required to achieve it.

From Fig. 5.7c, we notice that the $NLESR$ coefficient a is not a constant, but a

function of the applied V_{peak} . In order to see why a changes with V_{peak} , we computed an average value of $NLESR$ from (5.9) as (by assuming that the asymmetrical waveform of V_{DS} is approximately sinusoidal, i.e. symmetrical around a peak voltage of V_{peak})

$$\text{NLESR}_{\text{AVG}} = \frac{\int_0^\pi a \cdot V_{\text{peak}}^2 \sin^2(\frac{\omega t}{2}) d\omega t}{\pi} = \frac{a \cdot V_{\text{peak}}^2}{2}. \quad (5.10)$$

When $\text{NLESR}_{\text{AVG}}$ as calculated from (5.10) is plotted against the maximum dV/dt ($(dV/dt)_{\text{max}}$) of the waveform of V_{DS} as shown in Fig. 5.8, we see that it is a linear function of $(dV/dt)_{\text{max}}$. Thus, the existence of $NLESR$ explains the strong dependence of dissipated energy in output capacitance on dV/dt of drain to source wave-form[84], which can not be explained by the $C \cdot dV/dt$ losses occurring across linear ESR coming from (5.6), which only scale linearly with the dV/dt of the drain to source waveform. Thus $NLESR$ model predicts a loss across C_{oss} that is proportional to both $(dV/dt)^2$ and dV/dt of the drain to source waveform, since the linear fit equation for $\text{NLESR}_{\text{AVG}}$ from Fig. 5.8, when substituted in (5.6) in place of ESR will result in two terms, one proportional to $(dV/dt)^2$ and another to dV/dt . Thus, $NLESR$ model is useful in the cases where accurate dynamic prediction (i.e. of transient wave-forms) in the calculation of energy dissipation across C_{oss} and the $(dV/dt)^2$ dependent loss term are of paramount importance.

5.5 Model Comparison And Analysis

Unlike the linear ESR model, $NLESR$ & non-linear C_{ds} model lacks a physical explanation as of now, because their non-linearity doesn't fit into the well established theory on dielectric absorption or any other established theory. Furthermore, according to the recent work on OFF-state modeling of energy losses in C_{oss} there have been following hypotheses regarding the origin of these losses:

1. According to [95], the physical origin of ESR could be due to the resistive behavior of the carbon-related defect band present in the multi-layer III-N buffer, i.e. in the

Table 5.2: Table comparing the linear ESR model with *NLESR* & NL C_{ds} model

Linear ESR model	<i>NLESR</i> & NL C_{ds} model
Uses constant valued resistor	Uses bias dependent resistor
Uses non-linear C_{gd} & linear C_{ds} model of C_{oss}	Uses both non-linear C_{gd} & C_{ds} model of C_{oss}
Unable to model the location of bulge and curvature of the V_{DS} vs Q_{oss} characteristics	Can model both the location of bulge and curvature of the V_{DS} vs Q_{oss} characteristics
Can't model second degree dV/dt losses in power GaN HEMTs but only models first degree dV/dt term	NLESR _{AVG} models the second degree dV/dt losses in power GaN HEMTs in addition to the first degree dV/dt term

dielectric of the parasitic capacitance between the drain and the substrate of the lateral HEMT device.

- According to [96], there exists a close relationship between the vertical physical stack design in the lateral HEMT device and electrical characteristics such as R_{on} & C_{oss} losses. Deep trap levels in the GaN buffer layer have a long trap/de-trap time constant, which makes the electrons trapped in these deep levels unable to follow the high frequency V_{DS} change, which contributes to the hysteretic behavior in the OFF-state C_{oss} losses. These trap sites in the vertical GaN stack are primarily due to threading dislocations resulting from the large lattice mismatch between the GaN and (Si) substrate. When a large bias is applied between the drain and source terminals, the electrons accelerate in the conducting channel to gain enough kinetic energy to be injected into nearby buffer layer traps. Furthermore, [96] shows that

E_{DISS} reaches peak at around room temperature and decreases as we move away from room temperature in either direction. Also, the total charge stored at V_{peak} for multiple temperature conditions is approximately the same, which implies that the reduction in C_{oss} loss as we move away from room temperature is mainly due to a decrease in trapping effect, not due to reduction in overall stored energy. This leads to a hypothesis that the reduction in hysteresis loss with increase in temperature is because of faster de-trapping time constant during the voltage ramp-down, i.e. a decrease in the de-trapping time constant with increase in temperature.

3. Finally, in [97] small-signal C-V measurements on C_{oss} are used to characterize the dielectric stack from drain to the substrate with an addition of parallel resistance across C_{oss} to model the DC leakage path and the corresponding losses through that resistance. Furthermore, it is shown that the effect of parallel resistance is dominant at lower frequencies , while ESR significantly contributes to the switching dynamics and C_{oss} losses for sinusoidal frequencies higher than 1 MHz through its contribution to the Q factor (which is the reciprocal of DF, whose origin is shown in Fig. 5.6). This justifies our assumption of infinite parallel resistance across the nodes D & S in Fig. 5.2 (i.e. not a part of our model at all due to open circuit). However, for applied sinusoidal frequencies below 1 MHz, this parallel resistance will be a dominant factor in determining E_{DISS} .

Fig. 5.9 shows a plot of C_{oss} vs V_{DS} using small-signal model that was created from the measurements performed by C-V meter and modeled in chapt.3, with simulation results from the large-signal, $NLESR$ and non-linear C_{ds} based model as given by equations (5.8) and (5.9). It shows that the large-signal capacitance can be quite higher than that measured by small-signal measurements. This has been verified experimentally in separate studies performed on super junction MOSFETs in [87] and SiC power transistors and AlGaN/GaN HEMTs in [97].

A comparison between the two models discussed so far has been summarized in Table. 5.2. Thus, the choice of model to be used in a practical power electronic circuit simulation will depend upon a trade-off between the level of accuracy required in the prediction of dynamic steady-state wave-forms and higher dV/dt dependent losses in a particular circuit, and the complexity of model.

5.6 Conclusion

In this chapter, we presented two approaches to model the large-signal Sawyer-Tower measurements from the small-signal package model based on ASM-GaN compact model. The results show that the losses resulting in the OFF-state output capacitance C_{oss} can be modeled using an ESR which represents the dielectric losses occurring in the vertical stack of compound semiconductor layers in a lateral HEMT device. Furthermore, we have compared our modeling approach with other approaches and found that our models give a detailed physical interpretation of the hysteretic losses occurring in the output capacitor C_{oss} .

6

Statistical Modeling Of Power AlGaN/GaN HEMTs*

“A judicious man looks on statistics not to get knowledge, but to save himself from having ignorance foisted on him.”

– Thomas Carlyle

6.1 Introduction

Circuit design tools and models for power electronic applications have lagged behind the mature IC industry for a very long time. Whereas IC industry, which is primarily based on Silicon technologies, adopts device modeling and circuit design methods based on

*Note: The various process corner and statistical models used in this chapter can be retrieved from the overall model card (B.1) by choosing the appropriate sections from the include file ‘stats_include.scs’ (B.2), with four available choices - ‘as_measured’ gives the model which was extracted in chapters 3 & 4; ‘typical’, ‘fast’ & ‘slow’ give the corresponding nominal, highest & lowest performance models and finally section ‘monte_carlo’ gives the statistical model of the power AlGaN/GaN HEMT PGA26E19BA.

wafer level PCM (Process Control Monitor) measurements quickly, the power electronic industry has been slower in adapting, perhaps because the switching frequencies that have been traditionally used to drive the discrete power semiconductor devices are primarily in the range of few 100's of KHz, which gives the circuit designers enough leeway to overlook or sometimes totally neglect the effects of process variations in the underlying discrete power devices present in their designs.

This outlook, however, seems to be changing with the practical DC-DC power converters designed and implemented[84] using power GaN HEMTs with switching frequencies reaching as high as 10 MHz, after considering various factors such as the saturation limits of magnetic materials used in inductor cores and constraints due to thermal budget of a given PCB design, resulting in much needed reduction in the passive component sizes, especially those of inductors. Typically, e-mode power AlGaN/GaN HEMTs are used in order to avert the false turn on because they can be easily designed with high threshold voltages with positive sign. The advantage of using GaN HEMTs are that they have a very high breakdown voltage and at the same time can achieve lower $R_{DS(on)}$ due to highly mobile 2DEG formed underneath AlGaN/GaN hetero-junction[29, 32].

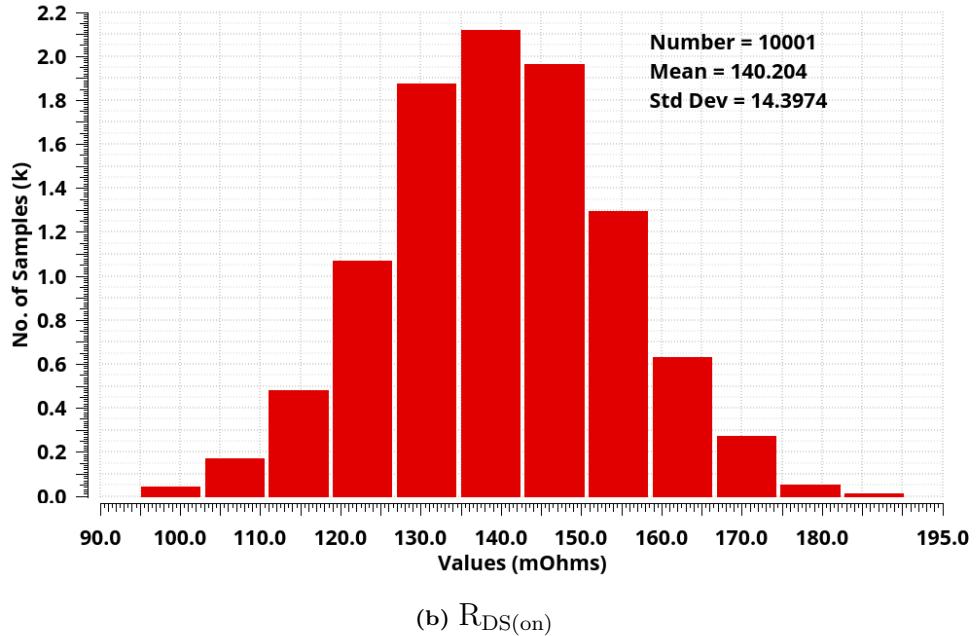
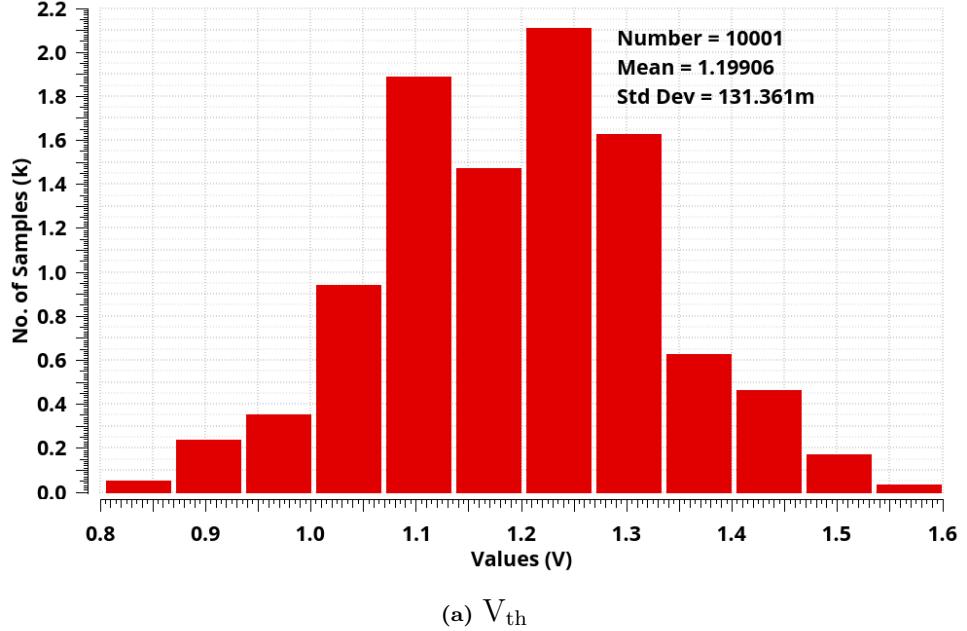
In [98], it has been shown that corner and statistical compact models of a Shielded-Gate Trench Power MOSFET can be extracted by using IC industry standard Backward Propagation of Variance (BPV) technique[99, 100], with the compact model giving the required sensitivities that relate the variances in the output electrical specifications to the variances in the input process/model parameters. This method, however, requires wafer level PCM measurements as one of its inputs. However, one of the major disadvantage of wafer level PCM measurements on power devices is that the drain to source ON-state resistance - $R_{DS(on)}$ can't be determined accurately because of high contact probe resistance relative to the channel, access/drift and source/drain contact resistances combined[98, 101]. TCAD based DOE (Design Of Experiments) could be used instead of

Table 6.1: Electrical specifications in the data-sheet of power HEMT PGA26E19BA.

Electrical Characteristics	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
Threshold voltage	V_{th}	$V_{DS} = 10 \text{ V},$ $I_{DS} = 1 \text{ mA}$	0.9	1.2	1.6	V
Drain-source ON-state resistance	$R_{DS(on)}$	$V_{GS} = 3.5 \text{ V}$ $I_{DS} = 5 \text{ A}$	-	140	190	$m\Omega$
Input capacitance	C_{iss}	$V_{iss} = 400 \text{ V},$ $V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$	-	160	-	pF
Output capacitance	C_{oss}		-	28	-	pF
Reverse transfer capacitance	C_{rss}		-	0.2	-	pF
Gate resistance	R_g	Open drain, $f = 100 \text{ MHz}$	-	800	-	$m\Omega$

PCM measurements, however that is not an option for a power electronic circuit designer because of the lack of actual process parameter inputs which are generally a well kept secret of semiconductor foundries.

In this chapter, we used data-sheet based specifications of a commercially available power AlGaN/GaN HEMT - PGA26E19BA[37] (which has been used for model parameter extraction in chapters 3, 4 & 5), on various DC and AC electrically measurable quantities such V_{th} , $R_{DS(on)}$, C_{oss} etc in order to create corner models and then Monte Carlo simulation based statistical model. Note that since the above electrical specs of a given device are measured as a single point measurements, they are not printed in italics, because they are no longer dynamic quantities. The as-measured model was first centred to the specifications, which we call as typical corner model. Then this typical corner model was used to find out the key model parameter variations required to give



the shift in the min/max values of chosen electrical specifications given in Table. 6.1 from the data-sheet of PGA26E19BA[68]. Using this process, corner models were generated. We assume that these corner models model the $\pm 3\sigma$ variation in device characteristics. We further mapped this $\pm 3\sigma$ variation in device characteristics given by corner models to

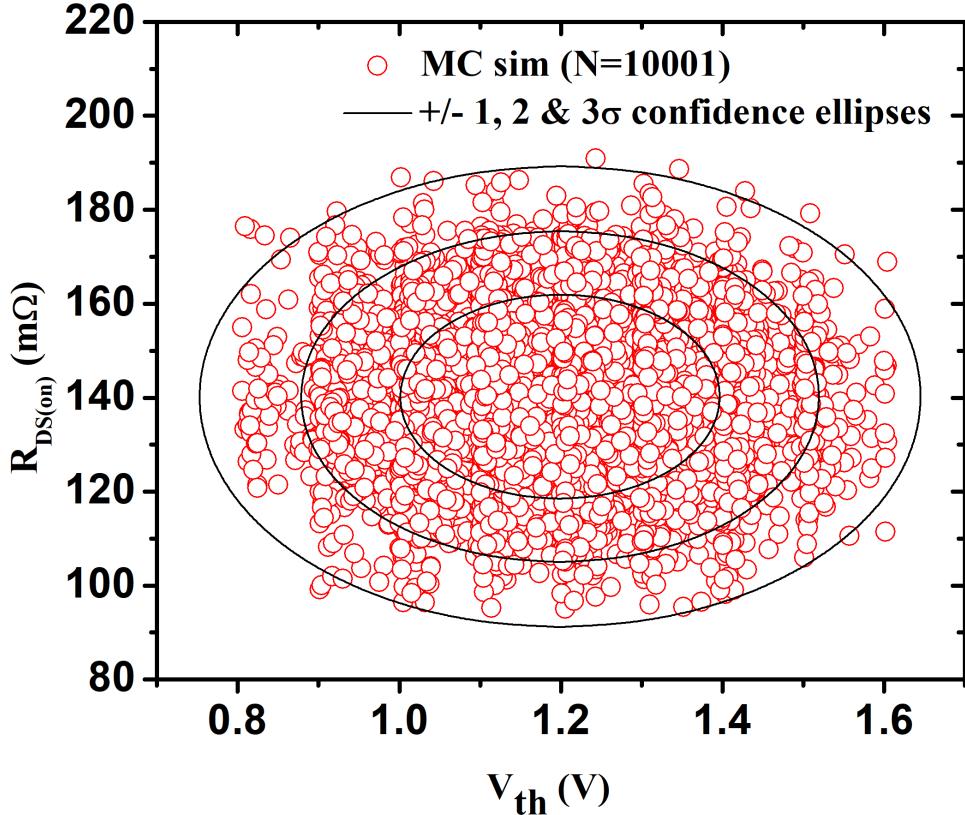
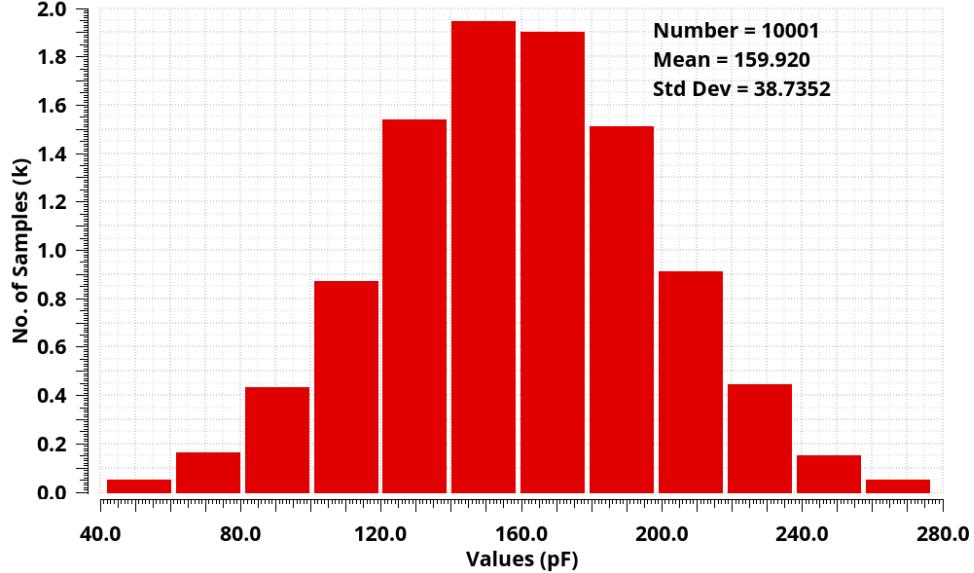
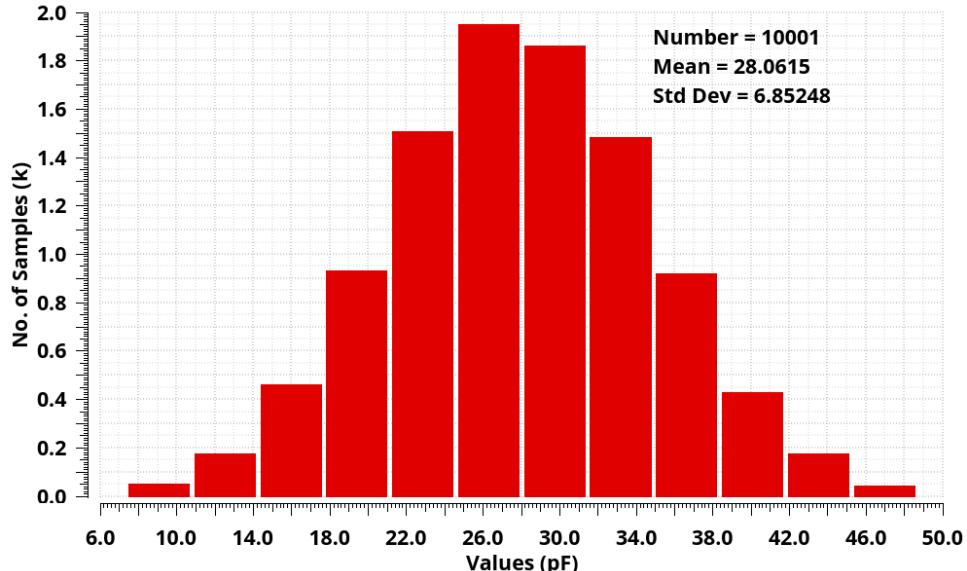


Figure 6.1: Monte Carlo simulation results for various DC electrical specifications using statistical model.

the $\pm 3\sigma$ variation in the input model parameters using the BPV technique by assigning a Gaussian standard deviation of

$$\sigma = \max \left(\frac{|p_{slow} - p_{typical}|}{3}, \frac{|p_{fast} - p_{typical}|}{3} \right), \quad (6.1)$$

to each constituent model parameter that was used to create the corner models, where model parameter p_{corner} is the value of p for a particular corner - “corner”. Here, a Gaussian or normal distribution in the constituent model parameters is assumed because that is the most general distribution encountered in practice and when sufficiently large samples are taken, then any other types distributions approach Gaussian according to the central limit theorem. The implementation of statistical model was done by using

(a) C_{iss} (b) C_{oss}

statistics block of Spectre simulator, where we can input the statistical variation in the model parameters as an input for Monte Carlo simulations. Thus, a statistical model of given HEMT was generated. All of this is discussed in section 6.2. In section 6.3, the developed statistical model is then used to simulate some key electrical specifications of

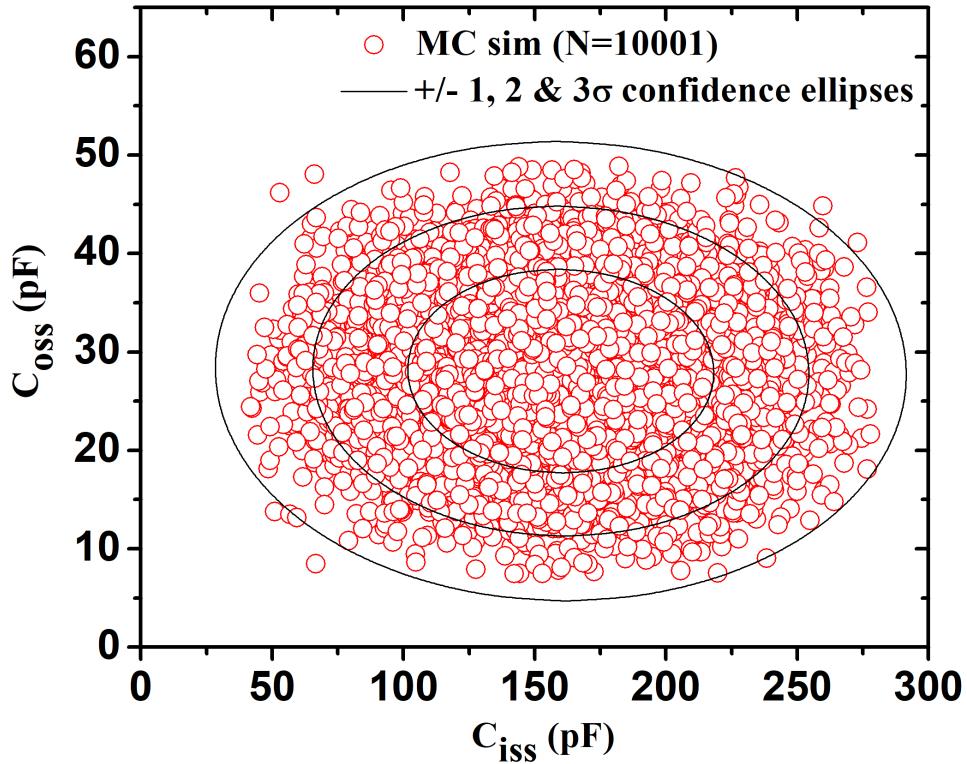
(c) Correlation plot between C_{oss} & C_{iss}

Figure 6.2: Monte Carlo simulation results for various AC electrical specifications using statistical model.

a gate charge and switching times circuit.

6.2 Corner And Statistical Model Extraction from BPV Technique

6.2.1 BPV Technique

BPV is a popular technique[98–100] used to extract statistical models for a given centred model. A centred model is a model whose model parameters (p) have been further tuned to model the nominal or typical performance of the device, with nominal parameters

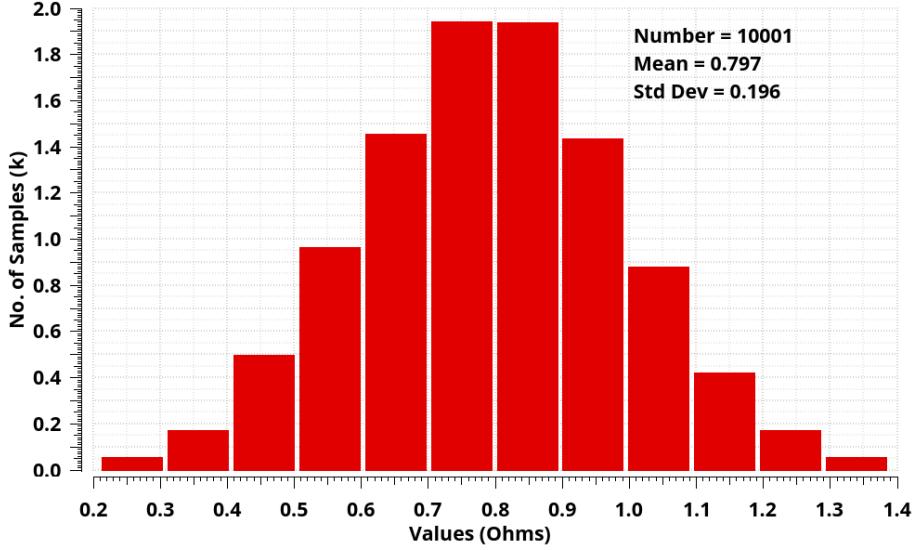


Figure 6.3: Monte Carlo simulation results for the RGC component of total gate resistance R_g .

$p_{typical}$. Normally, BPV requires variation in physical process parameters in the model such as AlGaN barrier thickness, carrier mobility etc. These are model parameters in ASM-GaN compact model. Their variation in a large-scale manufacturing environment are not generally available to a common user. However, if we use a physically calibrated compact model, then we can select a set of uncorrelated model parameters from a typical corner model - $p_1, p_2..p_N$ that give us maximum sensitivity to a selected set of electrical specifications at typical corner - $e_1, e_2..e_M$. In this case we write,

$$\mu_{e_m} = e_m(p_{typical}), \quad (6.2a)$$

$$\sigma_{e_m}^2 = \sum_{i=1}^N s_{m,i}^2 \sigma_{p_i}^2, \quad (6.2b)$$

where $s_{m,i} = \frac{\partial e_m}{\partial p_i}$ is the sensitivity which is given by the ASM-GaN compact model. Equation (6.2b) gives the relationship between variances in the outputs (e) and inputs (p) in terms of this sensitivity.

Table 6.2: Model parameters used for corner model generation

Model Parameter	Fast	Typical	Slow	3σ for statistical model, calculated from (6.1)
VOFF (V)	1.4	1.7	2.1	0.4
RDC ($m\Omega$)	35.063	55.266	75.213	20.203
RSC ($m\Omega$)	17.818	28.086	38.223	10.267
RSS0 ($m\Omega$)	11.8	18.6	25.313	6.8
RDD0 ($m\Omega$)	22.992	36.24	49.32	13.248

6.2.2 Corner Modeling

A corner model can be defined as a set of models that correspond to the min/typical/max limits of a chosen set of electrical specifications. For a corner model (6.2b) can then be re-written as

$$\sigma_{e_m} = \sum_{i=1}^N s_{m,i} \sigma_{p_i}. \quad (6.3)$$

After the initial step of determining the typical corner model parameters $p_{typical}$ from the as extracted model, both of which can be accessed by selecting the section “typical” & “as_measured” respectively from the include file “stats_include.scs” given in listing B.2, we used (6.3) to vary the model parameters VOFF, RDC, RSC, RSS0 & RDD0 which were chosen for their maximum sensitivity for a selected set of DC electrical specifications V_{th} and $R_{DS(on)}$ from the data-sheet of the given device PGA26E19BA (see Table. 6.1). These particular choices of electrical specifications ($e_1 = V_{th}$, $e_2 = R_{DS(on)}$) and model parameters ($p_1 = VOFF$, $p_2 = RDC$, $p_3 = RSC$, $p_4 = RSS0$, $p_5 = RDD0$) needs further explanation in terms of their uncorrelated character, which is essential for BPV technique to work as discussed earlier. For a long channel MOSFET device, for example, threshold voltage and channel ON resistance (which is dominated by the mobility factor BETA, as contact

resistances are a small fraction of the drain to source resistance) are correlated through the oxide thickness (t_{ox}) variation. In case of HEMTs, this would come through the AlGaN barrier thickness (TBAR) variation. For our HEMT device PGA26E19BA, if the channel resistance is bigger than the source/drain access and contact resistances (see Fig. 2.3), then we would be required to find out the correlation between their constituent model parameters i.e. between VOFF and BETA0 either experimentally or through TCAD DOE simulations. In order to verify our assumption of V_{th} & $R_{DS(on)}$ and their constituent model parameters being uncorrelated, so that equations 6.2b & 6.3 work without an additional term for correlation, we performed a simulation study in which we calculated the relative contributions of various resistances to $R_{DS(on)}$ as shown in Fig. 2.3. We simulated the typical corner model for this and found following composition for the $140\ m\Omega$ of $R_{DS(on)}$:

1. $73.67\ m\Omega$ comes from contact resistances with model parameters RSC and RDC.
2. $64.33\ m\Omega$ comes from the bias independent source and drain access resistance model parameters RSS0 and RDD0.
3. $2\ m\Omega$ comes from the mobility factor BETA ($= \mu_{eff} \cdot \frac{W}{L}$ from 2.8 & 2.9), i.e. from the channel resistance.

Thus, the channel resistance that is controlled by mobility factor BETA has very little or no effect on the total drain to source ON resistance $R_{DS(on)}$ and hence the correlation between V_{th} & $R_{DS(on)}$ is negligible, which justifies our assumption that the electrical specifications that we chose (e_1, e_2 etc) and subsequently their constituent model parameters (p_1, p_2 etc) are uncorrelated in between themselves, which is also evident from the correlation plot between them in Fig. 6.1c for DC and Fig. 6.2c for AC electrical specifications.

For AC electrical specifications, we chose C_{iss} , C_{oss} , C_{rss} & R_g . Since none of the AC electrical specifications chosen had min/max values given in the data-sheet (i.e. only

typical values were given), we assumed a $\pm 25\%$ variation in order to get their min/max limits. Fig. 6.2c shows that there is no correlation in between C_{iss} & C_{oss} , which is expected because they share C_{rss} as a common factor, which turns out to be negligible when compared to their values, hence not plotted separately.

The model parameter values used to create various sub-sets of a corner model following the process described above has been summarized in Table. 6.2. We call the sub-set model with highest threshold voltage and on resistance to be slow corner, and the sub-set model with lowest threshold voltage and on resistance to be the fast corner, as threshold voltage and on resistance are critical parameters that control the switching speed of the device.

6.2.3 Statistical Modeling

A statistical model is a model derived from the typical corner model by assigning some variations to selected model parameters, assuming they all follow a certain distribution such as Gaussian, uniform etc. The generated model then emulates a real world variation by randomly varying the specified model parameters in the statistical block (in case of Spectre circuit simulator) and which can then be used to simulate the corresponding random distribution in the chosen electrical specifications by performing Monte Carlo simulations. We mapped the minimum and maximum limits of our statistical model to the $\pm 3\sigma$ variation given by the corner models, because corner models give us the limits of a fabrication process that has been controlled by statistical process control, by covering the 6σ minimum to maximum variation around the mean.

The statistical model which was thus created is shown in the statistics block in the file “stats_include.scs” given in listing B.2 in appendix. B. Note that we assumed a very high amount of variability ($\pm 25\%$) for all the AC electrical specifications because their lower and upper limits aren’t given in Table. 6.1. This model card was then used to perform Monte Carlo simulations. Thus, the final value of a model parameter p_i used during one

of the iterations of a Monte Carlo simulation is given by

$$p_i = p_{i,\text{typical}} \left(1 + 0.01 N_{S,p_i} \sigma_{p_i} \right), \quad (6.4)$$

where $p_{i,\text{typical}}$ is the nominal/typical corner value of model parameter p_i , σ_{p_i} is the standard deviation of the global variation in p_i in terms of percentage, N_{S,p_i} is a random number generated within a range of $[-3, +3]$ in order to simulate the $\pm 3\sigma$ variation, which corresponds to a 99.7% confidence interval. Note that the maximum variation in N_{S,p_i} is controlled by the statement “truncate tr=3” in listing B.2. That can be changed to any other maximum variation of say $\pm x\sigma$ by changing the statement to “truncate tr=x”. Fig. 6.1 and Fig. 6.2 show the Monte Carlo simulation results after running the statistical model for 10001 runs (since it includes an initial typical corner run in addition to 10000 random runs).

6.3 Circuit Level DOE Using Monte Carlo Simulations

In order to understand how the statistical model generated in previous section impacts at circuit level, we used a gate charge and switching times evaluation circuit as shown in Fig. 6.4, with typical simulation outputs for gate charge and various switching times shown in Fig. 6.5 & Fig. 6.6 respectively. This circuit was used as a bench-mark setup in order to understand circuit-level performance variations due to the underlying process variations. The circuit is based on a 55 V - 100 V, 100 W DC-DC boost converter designed and simulated in chapt.3 for a switching frequency of 5 MHz. The results after performing Monte Carlo runs for total gate charge ($Q_{g(\text{tot})} = Q_{gs1} + Q_{gd} + Q_{gs2}$, shown in Fig. 6.5 for a single simulation) and switching times ($t_{d(\text{on})}$, t_r , $t_{d(\text{off})}$ & t_f , shown in Fig. 6.6 for a single simulation) are shown in Fig. 6.7, Fig. 6.8 & Fig. 6.9. We see a ± 0.3 nC variation

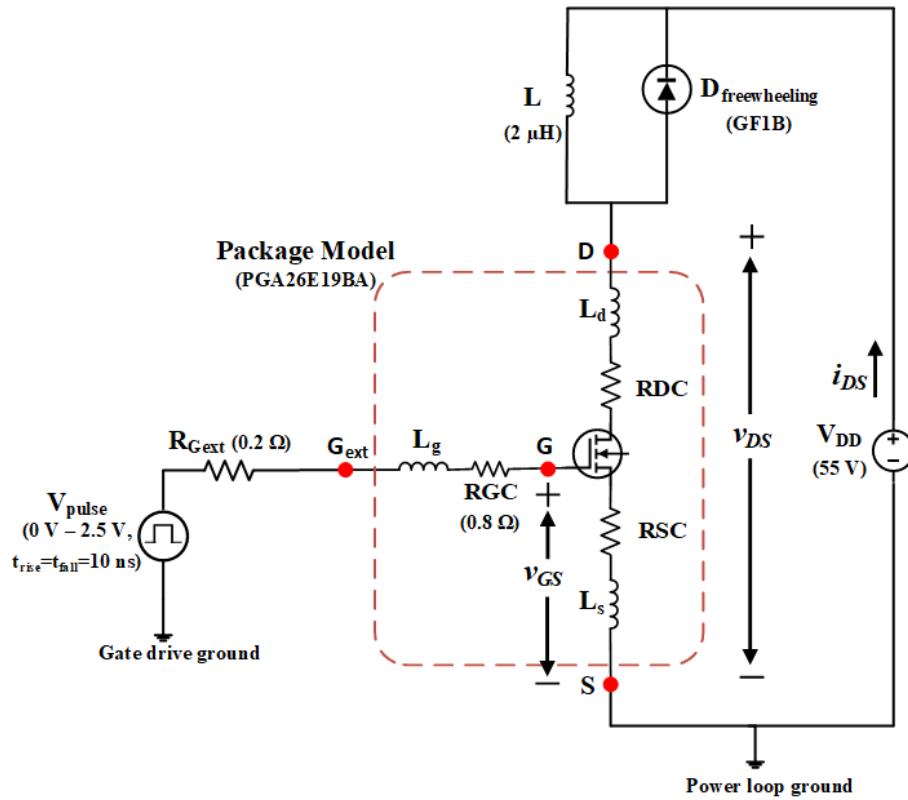


Figure 6.4: Schematic of a gate charge and switching times evaluation circuit. Note that for Monte Carlo simulation, $L_g = L_d = L_s = 0$ was taken as these inductances cause many iterations in the Monte Carlo simulation to fail due to convergence errors caused by random shift in device characteristics during these iterations. This simplifying assumption also leads to equations (6.5a) & (6.5b) for charging and discharging of input gate capacitance C_{iss} respectively.

around the typical gate charge of 1 nC for the designed gate overdrive voltage or peak pulsed voltage V_{GP} of 2.5 V and V_{DD} of 55 V in Fig. 6.7. This means that for a boost converter designed using given component values, a designer must keep in mind that the gate drive circuit must be able to deliver an extra charge of 0.3 nC over the typical design. Similarly, Fig. 6.8 & Fig. 6.9 show the correlation between two pairs of switching times which are correlated. For t_r & t_f , it shows a positive correlation i.e. both move in the same direction when the model parameters are randomly varied, while $t_{d(on)}$ & $t_{d(off)}$ show a negative correlation, which implies that they move in opposite direction when subjected

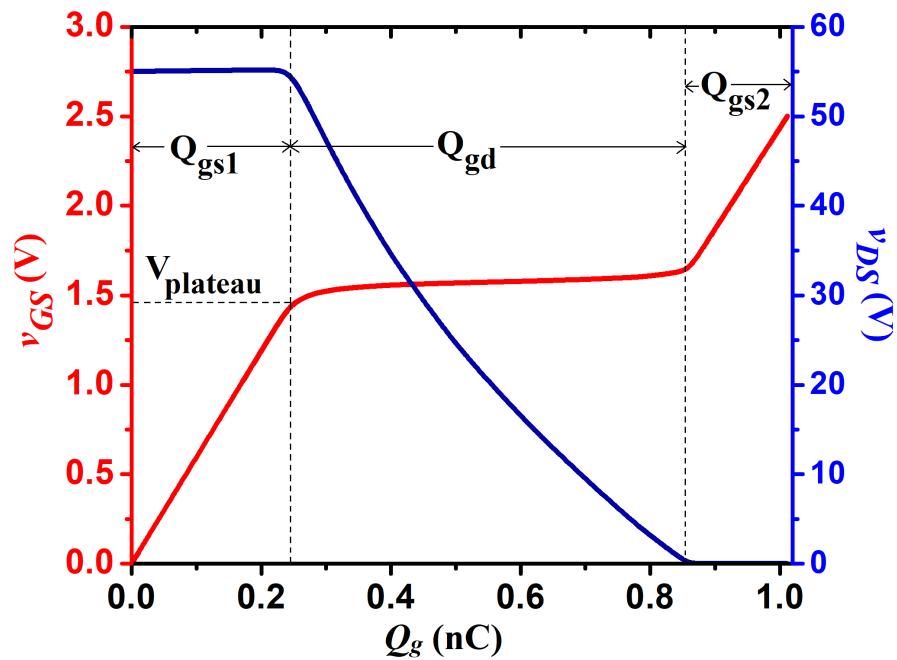


Figure 6.5: Simulated wave-forms for gate charge using circuit in Fig. 6.4.

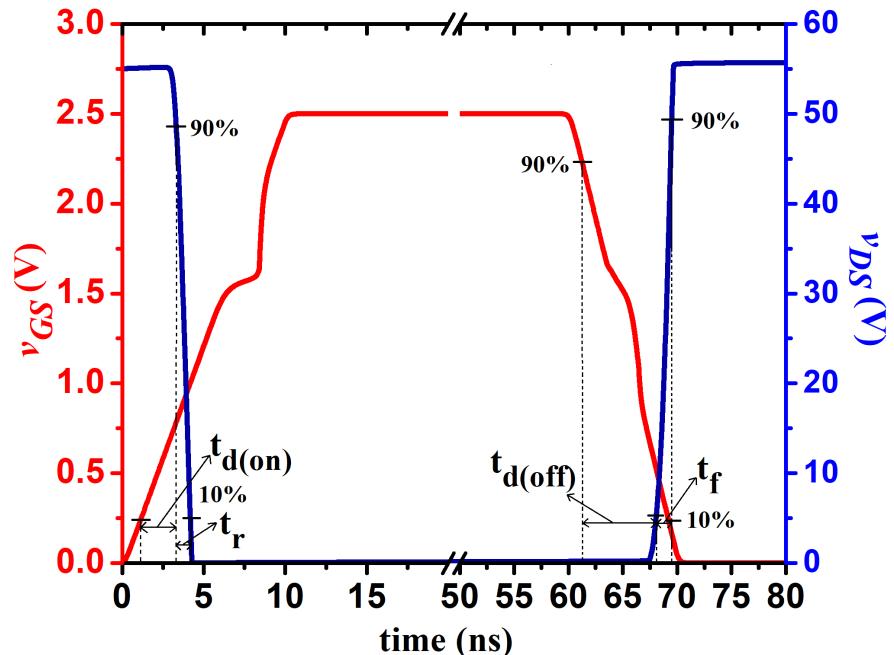


Figure 6.6: Simulated wave-forms for switching times using circuit in Fig. 6.4.

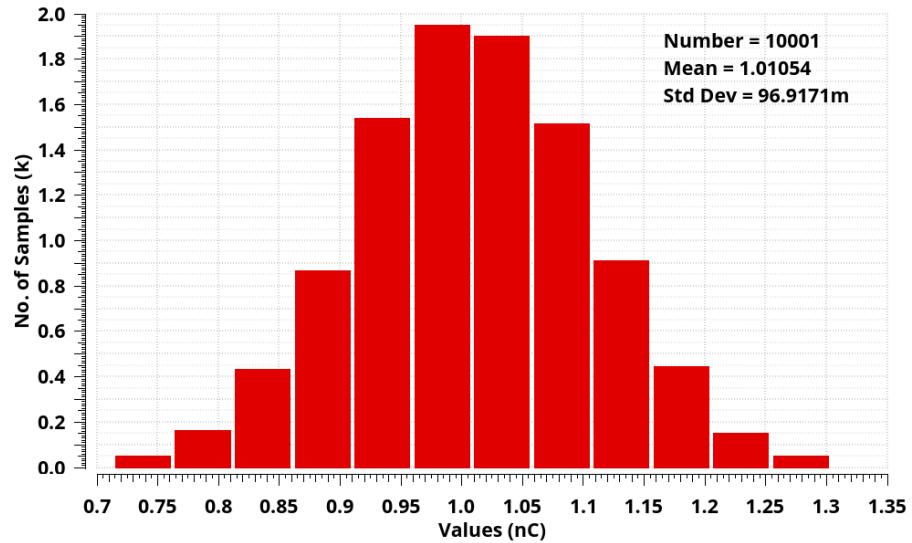


Figure 6.7: Monte Carlo distribution for total gate charge $Q_{g(\text{tot})}$.

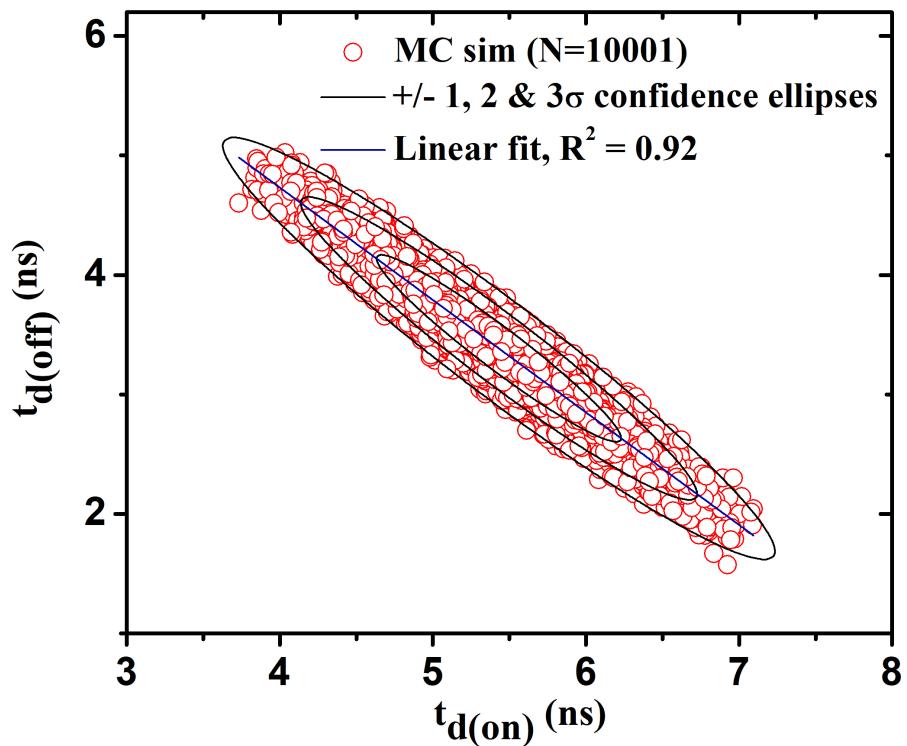


Figure 6.8: Correlation plot between $t_{d(\text{off})}$ & $t_{d(\text{on})}$.

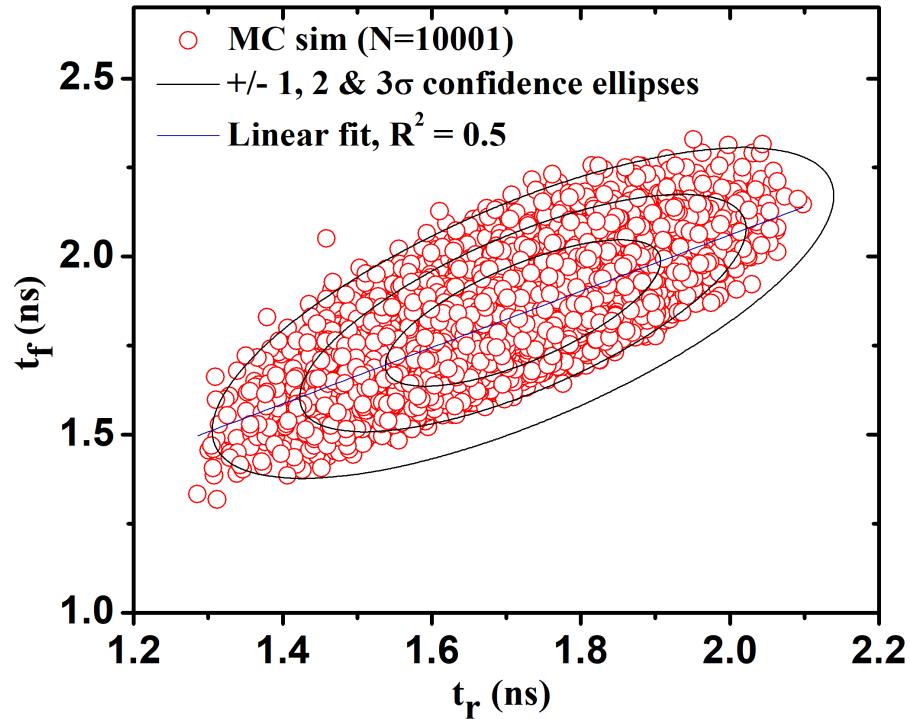


Figure 6.9: Correlation plot between t_f & t_r .

Table 6.3: Switching times simulation output using simulation setup of circuit in Fig. 6.4 for various corner models of Table. 6.2

Timing parameter	Fast	Typical	Slow
$t_{d(on)}$ (ns)	4.05	5.3	6.962
t_r (ns)	1.684	1.729	1.785
$t_{d(off)}$ (ns)	4.5	3.225	1.6
t_f (ns)	1.675	1.836	2.04
$t_{d(on)} + t_{d(off)}$ (ns)	8.55	8.525	8.562
$V_{plateau}$ (V)	1.13	1.45	1.9

to process variations. This is summarized in Table. 6.3 by using the limits of the statistical model i.e. corner models.

The corner simulations in Table. 6.3 show that addition of $t_{d(on)}$ & $t_{d(off)}$ for any corner

is a constant value, approximately equal to 8.5 ns. This is because $t_{d(on)}$ & $t_{d(off)}$ are the times taken to charge & discharge the input OFF-state gate capacitance $C_{iss} = C_{gs} + C_{gd}$ (see Fig. 6.5 & Fig. 6.6), with $t_{d(on)}$ given by the time it takes to charge C_{iss} to the value of approximately Q_{gs1} plus some part of Q_{gd} (let us say equal to Q_{gd1} , covering only 10 % decrease of v_{DS} , with an associated time delay of $t_{d(Q_{gd1})}$), while $t_{d(off)}$ is given by the time it takes to discharge C_{iss} from the 90% of peak value of v_{GS} ($= V_{Gp}$, with a value of 2.5 V in our case as shown in Fig. 6.6), i.e. almost the whole of Q_{gs2} plus some part of Q_{gd} (let us say equal to Q_{gd2} with an associated time delay of $t_{d(Q_{gd2})}$). It is evident that both Q_{gd1} & Q_{gd2} are negligible, hence the delays associated with them $t_{d(Q_{gd1})}$ & $t_{d(Q_{gd2})}$ too are negligible. Furthermore, from the above discussion & [102], we can write following expressions:

$$t_{d(on)} \approx (R_{Gext} + R_{GC}) C_{iss} \cdot \ln \left(\frac{V_{Gp}}{(V_{Gp} - V_{plateau})} \right) + t_{d(Q_{gd1})}, \quad (6.5a)$$

$$t_{d(off)} \approx (R_{Gext} + R_{GC}) C_{iss} \cdot \ln \left(\frac{V_{Gp}}{V_{plateau}} \right) + t_{d(Q_{gd2})}, \quad (6.5b)$$

which have been derived by solving simple charging and discharging series RC circuit formed by $(R_{Gext} + R_{GC})$ & C_{iss} , with V_{pulse} as the switching power supply. The above equations are further based on following assumptions:

1. $L_g = L_d = L_s = 0$ in Fig. 6.4,
2. as already stated, both $t_{d(Q_{gd1})}$ & $t_{d(Q_{gd2})}$ are very small,
3. C_{iss} stays approximately constant with the device switching back and forth between OFF and ON states, which can be verified from Fig. 3.3, and
4. ON - state capacitance doesn't play a key role in the discharge process from ON-state to OFF-state.

Thus, a negative or inverse correlation between $t_{d(\text{off})}$ & $t_{d(\text{on})}$ as shown in Fig. 6.8 can be explained with the variation of plateau gate-source voltage V_{plateau} , which increases from fast to slow corner via typical corner, as summarized in Table. 6.3, in the same manner as the threshold voltage V_{th} of the device. With this increase, (6.5a) tells us that $t_{d(\text{on})}$ will increase, while (6.5b) tells us that $t_{d(\text{off})}$ will decrease, which explains the negative correlation between them in Fig. 6.8. However, if we add $t_{d(\text{on})}$ & $t_{d(\text{off})}$ by adding equations (6.5a) & (6.5b), we get a total time required to complete Q_{gs1} charging ($\approx t_{d(\text{on})}$) and Q_{gs2} discharging ($\approx t_{d(\text{off})}$) of C_{iss} at a given peak gate voltage V_{Gp} , which is primarily a function of input gate capacitance C_{iss} and total gate resistance R_g ($= R_{\text{Gext}} + \text{RGC}$). Although the variations in C_{iss} and R_g (via variation of model parameter RGC , while keeping external resistance R_{Gext} at a constant value) are kept at $\pm 25\%$ in their constituent model parameters CGDO, CGSO and RGC (see the ‘statistics’ block statement in the file ‘stats_include.scs’ in B.2) while performing Monte Carlo simulations using the statistical model, they were kept constant while creating the corner models because of their minimal role in affecting the various timing characteristics. Thus, the addition of $t_{d(\text{on})}$ & $t_{d(\text{off})}$ remains approximately constant for all the three corners, even though its individual time components vary according to (6.5) via the variation in plateau gate-source voltage V_{plateau} of the device. It is interesting to note that as a corollary of the above conclusion, the gate charge components Q_{gs1} & Q_{gs2} are also negatively correlated via V_{plateau} .

A positive correlation between t_f & t_r as shown in Fig. 6.9 can be explained from the fact that they both represent variation in v_{DS} from 10 % to 90 % and vice versa respectively, both of which happen during the Miller plateau, i.e. the Q_{gd} portion of Fig. 6.5. Hence, if one of the timing component changes, the other one follows because essentially one and the same part of gate charge/discharge cycle (Q_{gd}) is being traced with a change in the direction, which in itself is dictated by the charging/discharging process.

Thus, a gate charge and switching times evaluation circuit can be used in conjunction with a fully calibrated compact model of a power device with corner and statistical models embedded in it, in order to evaluate the extra gate charge requirements due to process variations and perform simulation studies on various switching times by which we can design appropriate snubber circuits for soft switching applications.

6.4 Conclusion

In this chapter, we created corner and statistical models of a commercial power GaN HEMT using electrical specifications based on its data-sheet. We applied BPV technique to calculate the required variations in various uncorrelated model parameters. The statistical model was further used to simulate and analyze various electrical specifications of a gate charge and switching times evaluation circuit based on a DC-DC boost converter design that was already designed and analyzed in chapt.3. It is shown that ASM-GaN compact model can be used to create such models and can further be used for process variation aware design of power electronic circuits.

7

Modeling Of Charge Trapping In AlGaN/GaN HEMTs

“The history of semiconductor physics is not one of grand heroic theories, but one of painstaking intelligent labor. Not strokes of genius producing lofty edifices, but great ingenuity and endless undulation of hope and despair. Not sweeping generalizations, but careful judgment of the border between perseverance and obstinacy. Thus the history of solid-state physics in general, and of semiconductors in particular, is not so much about great men and women and their glorious deeds, as about the unsung heroes of thousands of clever ideas and skillful experiments—reflection of an age of organization rather than of individuality.”

– Ernest Braun

7.1 Introduction

It is well-known that GaN HEMTs fabricated in many III-V semiconductor processes suffer from charge trapping related performance degradation. Charge trapping has been

linked to the imperfections in the device fabrication process. This results in the creation of so-called defect centres, or more commonly trap centres. Because of this problem, the considerable list of advantages attributed to GaN HEMTs in the last decade, due to their excellent and superior properties, are not fully realizable.

In the presence of charge trapping the DC characteristics of the GaN HEMTs are not representative of high-frequency operation [103]. Charge trapping is known to change the device characteristics significantly. Although, several promising techniques have been published to minimize this phenomenon, it still exists in state-of-the-art GaN devices to varying degrees. A comprehensive FET model which includes a model for charge trapping that is able to accurately predict this effect is crucial for accurate circuit design and simulations.

Trapping is often modeled by introducing empirical dispersion-related parameters [104–114]. A typical empirical approach in modeling charge trapping is Taylor expansion of the “state” of the trap center [104, 108, 114–116]. The coefficients are evaluated by numerical calculation of linear equations. Look-up table approach is then used in the simulator. As with all empirical models, these models are valid only for the regions for which the values of the look-up table are extracted. An alternative empirical approach is to use a low-frequency resistive-capacitive (RC) network(s) to model the dynamic of charge trapping [105, 107]. In [106, 108], and [113], diodes were also included in the RC network in order to differentiate between trapping and detrapping, which exhibit distinct time constants. None of these empirical RC-network based models capture the bias and temperature dependence of the trapping process. In [117] and [118], a simple, yet elegant model is proposed for a trap center that is based on Shockley-Read-Hall (SRH) statistics of the trapping process. This model can capture the trapping behavior at various bias conditions and temperatures. In this model, the trapping phenomenon is represented in terms of controlled current sources that can be easily handled by a circuit simulator. The

potential introduced by the trapping subcircuit has been used in [117] and [118] to offset the gate voltage. This potential can also be used to offset the drain and source access resistances to capture the trapping process induced by surface traps [118].

In this chapter, we adopt the SRH-based trap model presented in [117] and [118], and unify it with ASM-GaN model to develop a complete model of traps in GaN devices. Unlike the approach presented in [117] and [118], where the potential introduced by the SRH-based trap model modifies, depending on the location of the trap centers in the device, the gate voltage and/or the drain and source access resistances; in the modified GaN-HEMT model presented in this chapter, this potential modifies, depending on the location of the trap centers in the device, different physical parameters of ASM-GaN model.

The developed model is extensively validated by modeling DC and pulsed I-V characteristics of a GaN device. The accuracy of the model is validated for eight different quiescent bias points, with quiescent drain voltage ranging from 5 V to 20 V and quiescent gate voltage ranging from -2.8 V to -3.8 V, and a large range of gate and drain voltages to which the device was pulsed in the pulse measurements and at which the device was measured in the DC measurements, with gate voltage ranging from -4 V to 0.4 V and drain voltage ranging from 0 V to 40 V.

The chapter is arranged as follows. Section 7.2 presents the results of DC measurements as well as pulsed measurements from eight different quiescent conditions performed on a GaN HEMT. Section 7.3 reviews the charge-trapping mechanism in FETs and the SRH-based trap model developed in [117] and [118]. Section 7.4 presents a comprehensive model for the device under test which combines the ASM-GaN model with the SRH trap model, yielding an excellent fit to both the DC and pulse measurements. It is shown that, for the device under test, the parameters which are affected by the trap model are V_{OFF} (the cut-off/threshold voltage), $NS0ACCD$ (the 2-DEG charge density in per square meter

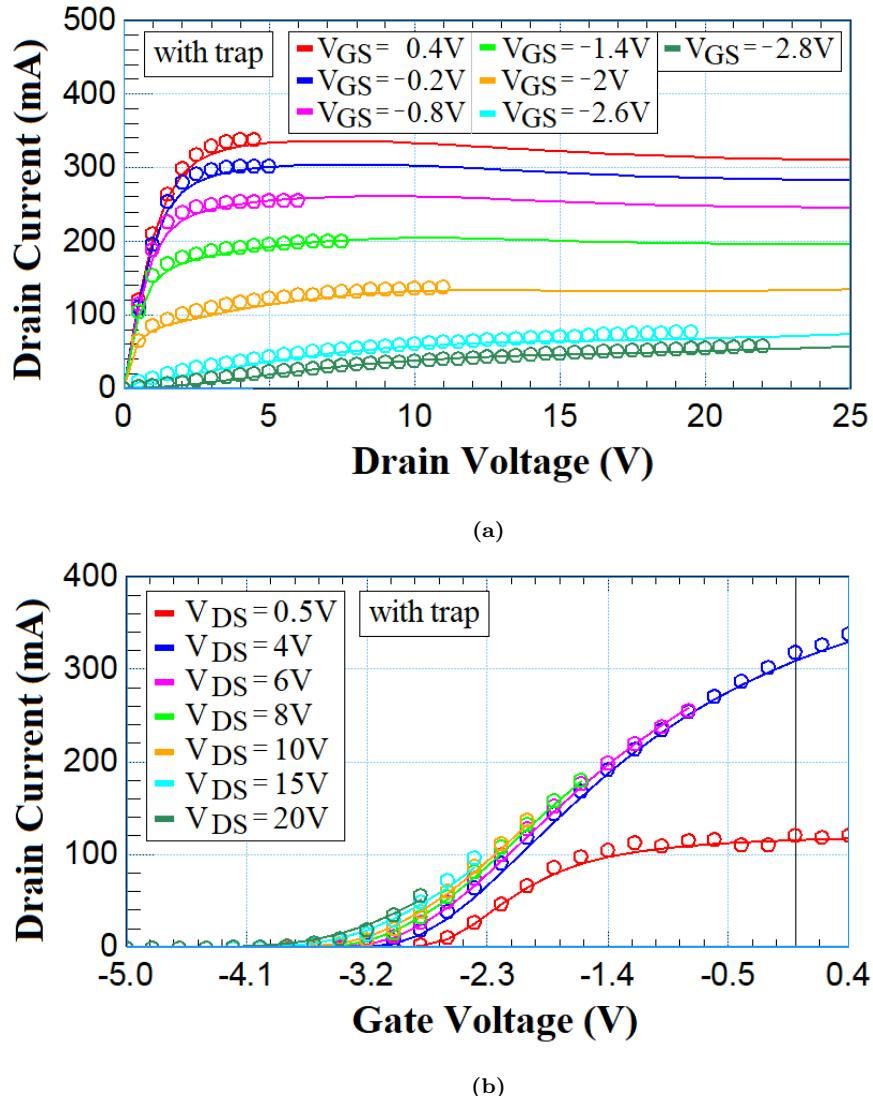


Figure 7.1: Measured (symbol) and modeled (solid line) DC output characteristics (a) and DC transfer characteristics (b) of the device under test. Self-heating was accounted for using the standard thermal network present in ASM-GaN model.

in drain access region) and UA (the first-order mobility degradation parameter). Finally, Section 7.5 draws conclusions.

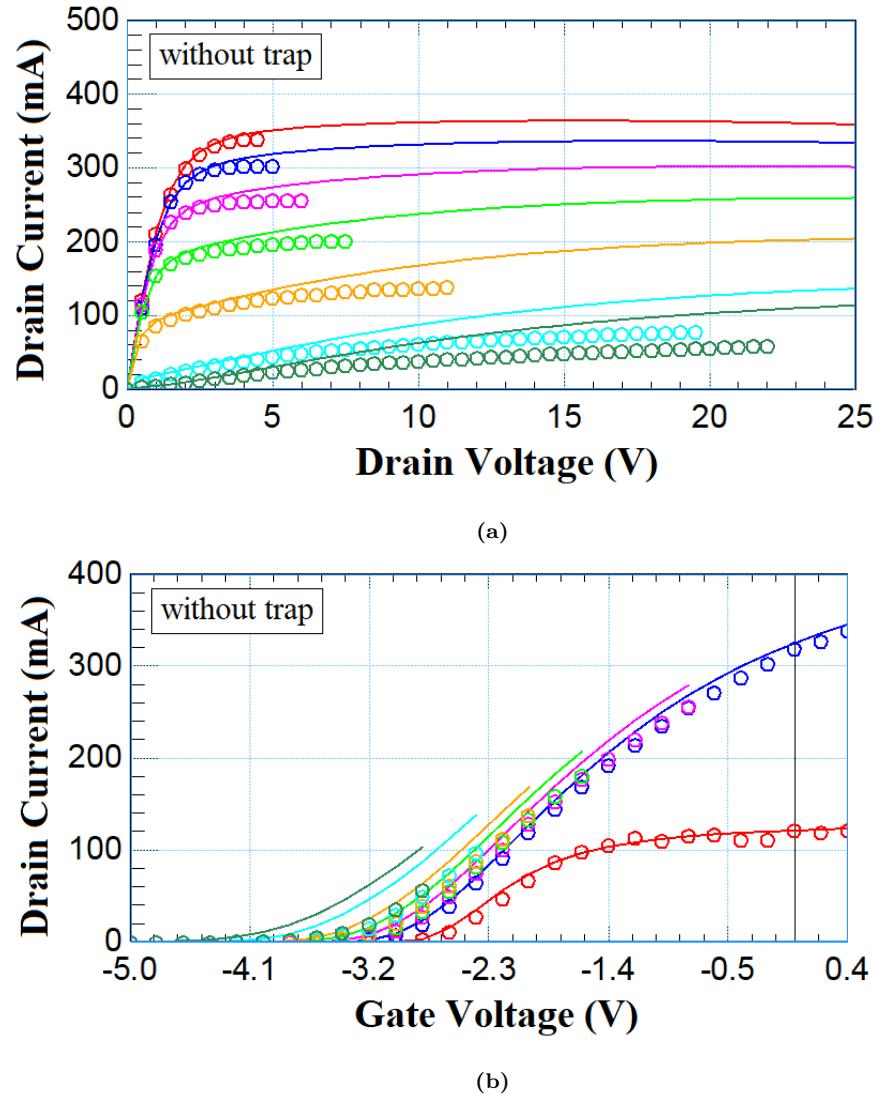


Figure 7.2: The simulation results of Fig. 7.1 for when the trap model is disabled.

7.2 Measurement Results

DC and pulse measurements were performed on a commercially available d-mode GaN HEMT of total $20 \mu\text{m}$ channel width and $0.25 \mu\text{m}$ channel length. The pulse width and duration in pulse measurements were $20 \mu\text{s}$ and 1 ms respectively. Measurements were performed $10 \mu\text{s}$ after step change. The DC output and transfer characteristics of this device are shown in Fig. 7.1. The device was pulsed from the following eight different

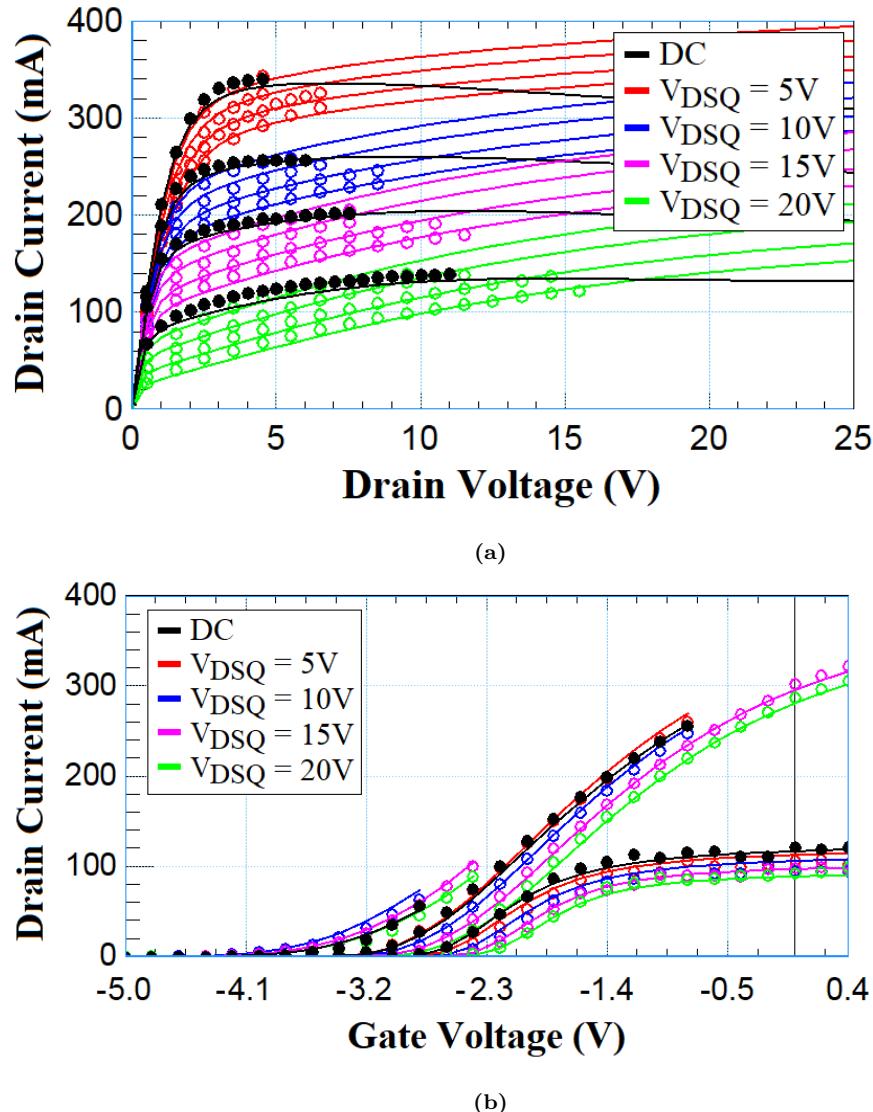


Figure 7.3: Measured (symbol) and modeled (solid line) pulsed output characteristics (a) and transfer characteristics (b) of the device under test for the following quiescent bias points: $(V_{DSQ}, V_{GSQ}) = (5 \text{ V}, -3.2 \text{ V}), (10 \text{ V}, -3.4 \text{ V}), (15 \text{ V}, -3.6 \text{ V})$ and $(10 \text{ V}, -3.8 \text{ V})$. The gate voltages for the output characteristics are: $0 \text{ V}, -0.8 \text{ V}, -1.4 \text{ V}$ and -2.0 V . The drain voltages for the transfer characteristics are: $0.5 \text{ V}, 6 \text{ V}$ and 20 V . The output and transfer characteristics are shown, for the purpose of comparison, alongside the DC characteristics of Fig. 7.5 for the same gate voltages.

quiescent conditions:

- $(V_{DSQ}, V_{GSQ}) = (5 \text{ V}, -3.2 \text{ V}), (5 \text{ V}, -2.8 \text{ V})$

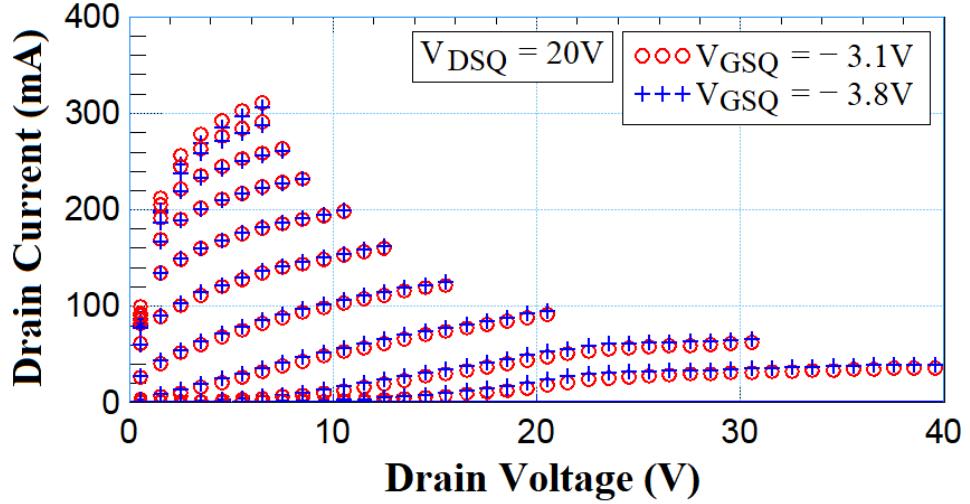


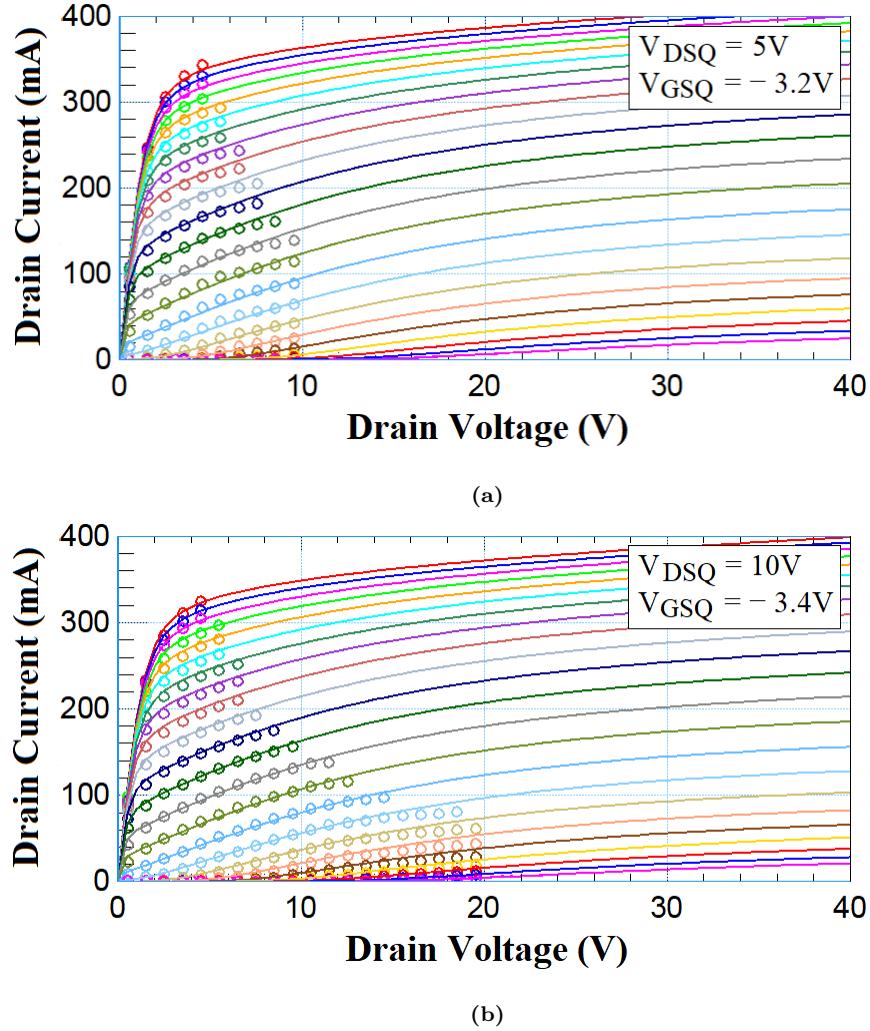
Figure 7.4: Measured pulsed output characteristics of the device under test for the quiescent bias point indicated in the legend. Gate voltage ranges from -3.2 V to 0.4 V with a step size of 0.4 V. This figure shows that the pulsed output characteristic of the device exhibits negligible dependence on the quiescent gate voltage. Similar results were obtained for other quiescent bias points.

- $(V_{DSQ}, V_{GSQ}) = (10 \text{ V}, -3.4 \text{ V}), (10 \text{ V}, -2.9 \text{ V})$
- $(V_{DSQ}, V_{GSQ}) = (15 \text{ V}, -3.6 \text{ V}), (15 \text{ V}, -3.0 \text{ V})$
- $(V_{DSQ}, V_{GSQ}) = (20 \text{ V}, -3.8 \text{ V}), (20 \text{ V}, -3.1 \text{ V})$

to a set of final bias points, with final drain voltage ranging from 0 V to 40 V with a step size of 0.5 V and final gate voltage ranging from -4 V to 0.4 V with a step size of 0.2 V.

Measurement results indicate that the I-V characteristics of the device exhibit, as shown in Fig. 7.3, significant variation with the quiescent drain voltage, but are insensitive, as shown in Fig. 7.4, to the quiescent gate voltage. From the results of Fig. 7.3, one can note the following:

- There is a positive shift in the threshold voltage with increasing V_{DSQ} .
- There is a decrease in the ON-state current with increasing V_{DSQ} .



These observations suggest that to model the trapping behavior of the device under test, one must consider an acceptor-like trap center which modifies the parameters VOFF and NS0ACCD of the ASM-GaN model. Existence of an acceptor-like trap is justified because, by definition, an acceptor-like trap center is a trap center that is neutral when all the energy levels of the trap center are empty, and negatively charged and, therefore, ionized, when one or more energy levels of the trap center are occupied by electrons. Thus, when subjected to a charge (electron) injection current either via reverse biased Schottky gate tunneling current, which is dictated by the Poole-Frenkel mechanism[119, 120], or via the tunneling of channel current in the ON-state of the device, the presence of an

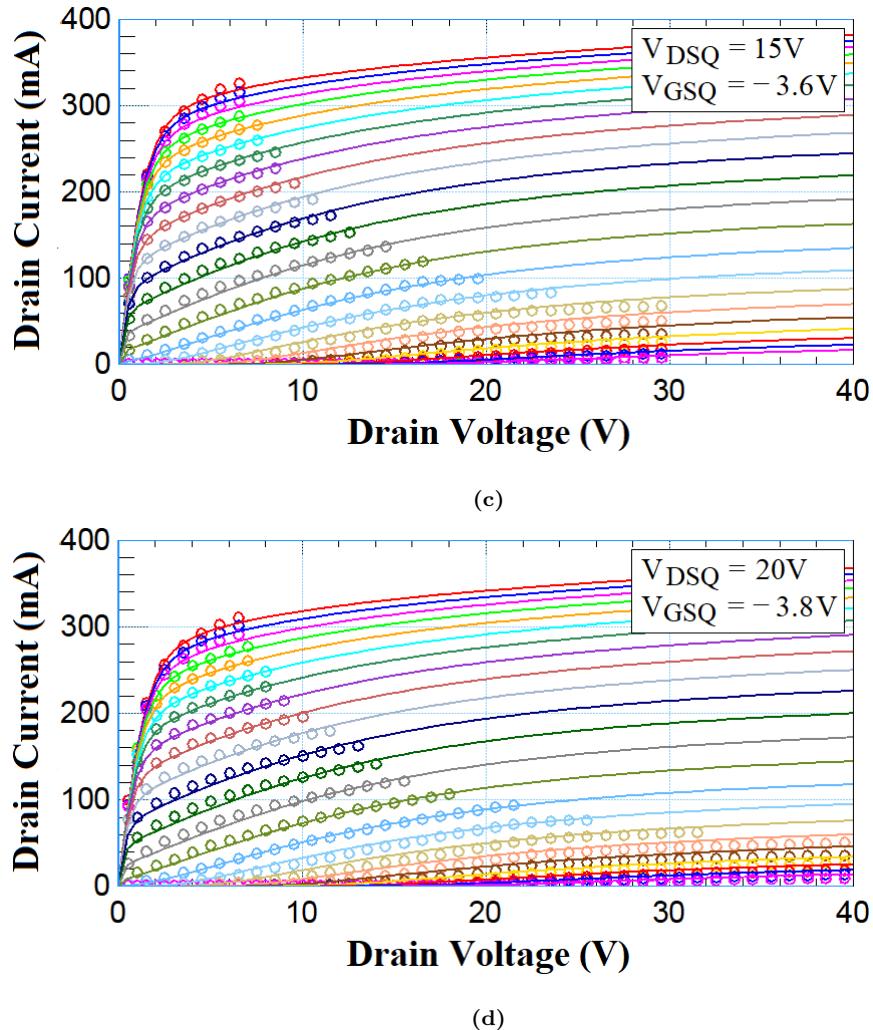
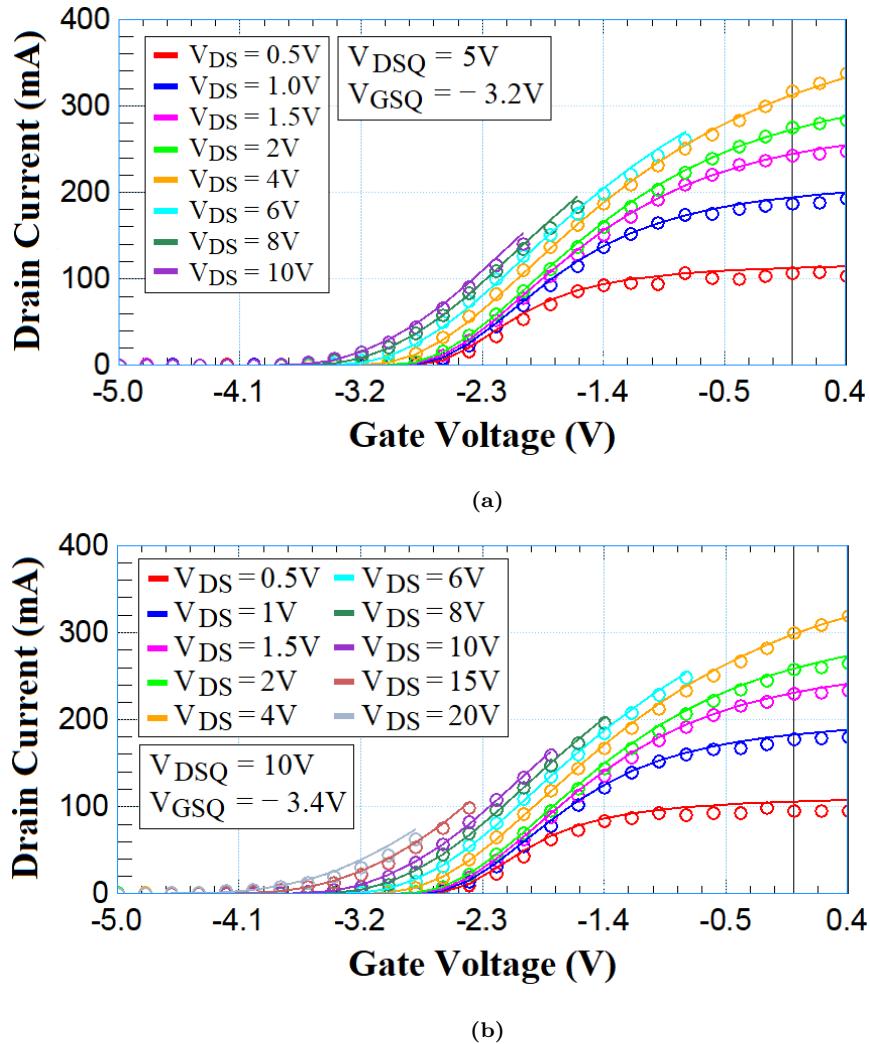


Figure 7.5: Measured (symbol) and modeled (solid line) pulsed output characteristics for the various quiescent bias points indicated in the legends. The gate voltage ranges from -3.2 V to 0.4 V with a step size of 0.2 V.

acceptor type trap center in the channel and access regions (both present in the active GaN layer) and the eventual capture of these injected electrons by these traps will result in increase of the threshold voltage due to the underlying electrostatics associated with traps under 2DEG channel region and decrease in access region carrier densities due to increased trapping of access 2DEG by access region traps. Indeed, as we will show later, it is possible to obtain an excellent fit to the output and transfer characteristics of the device



by letting the trap center of the device to change these two model parameters - V_{OFF} & $NS0ACCD$, as well as the first order mobility degradation parameter UA (see (2.10)), which implies that the ionized traps further decreases the low field surface mobility (which is given by model parameter U_0 in (2.10)) due to increased Coulomb scattering.

Figures 7.5 and 7.6 show the full sets of output and transfer characteristics corresponding to the four different quiescent drain voltages (i.e., $V_{DSQ} = 5\text{ V}$, 10 V , 15 V and 20 V). After reviewing the circuit model developed in [117] and [118], we will show that the observed complicated trapping behaviour in the measured results can be modeled by combining the ASM-GaN model with the SRH-based model of an acceptor trap center

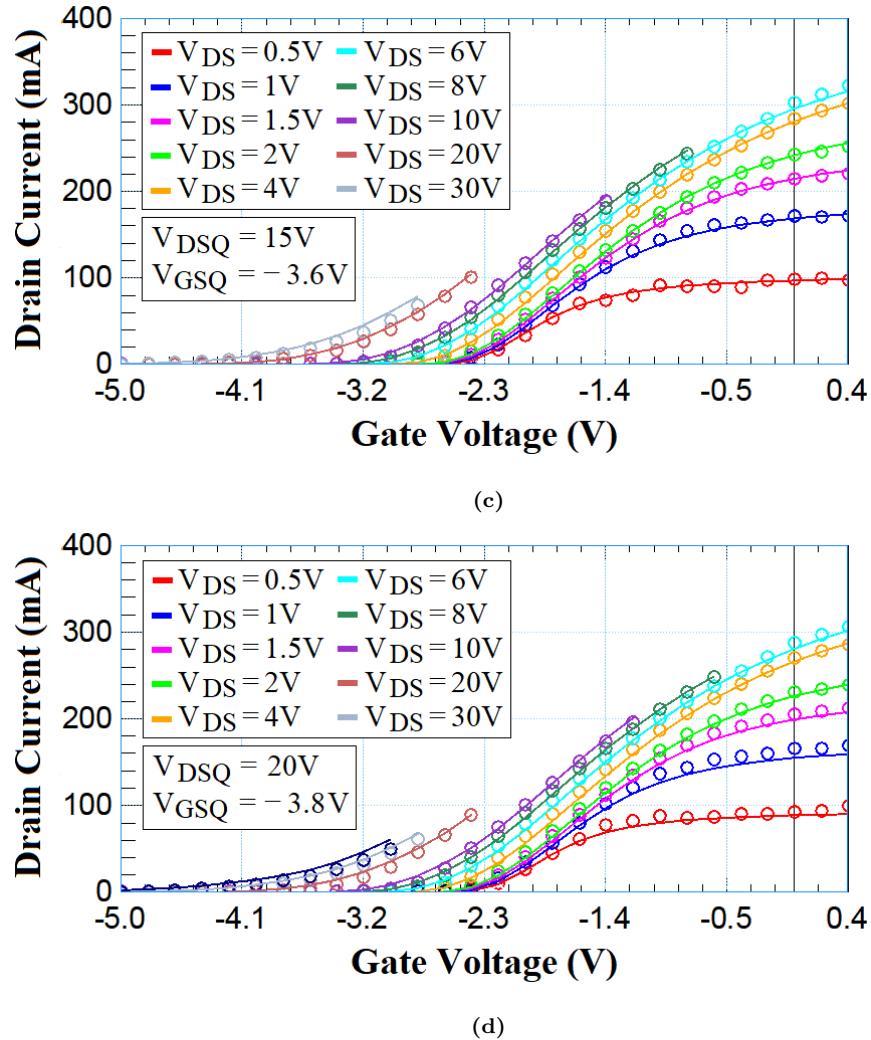


Figure 7.6: Measured (symbol) and modeled (solid line) pulsed transfer characteristics for the various quiescent bias points indicated in the legends. The drain voltages are also indicated in the legends.

which behaves as an electron trap center in the region of operation of the device and is subject to an electron current which is composed of the electrons of the channel which get injected into the trap center through tunneling. The potential of this trap center, which represents the ionization density of the trap centre, modifies three parameters of the ASM-GaN model, namely VOFF , UA and NS0ACCD .

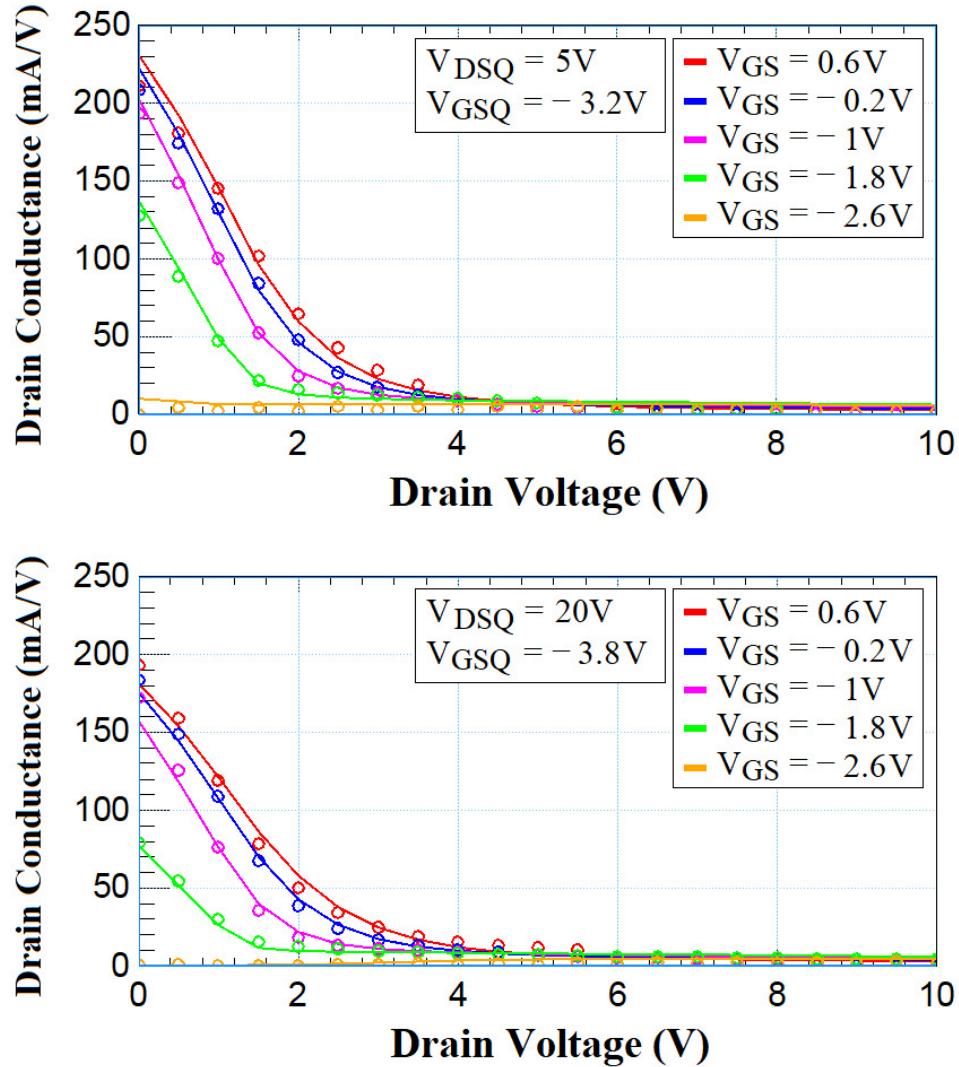


Figure 7.7: Measured (symbol) and modeled (solid line) pulsed output characteristics for the two quiescent bias points indicated in the legends. The gate voltage ranges from -3.2 V to 0.4 V with a step size of 0.2 V.

7.3 Circuit Implementation Of A Trap Center

In this section we review the charge-trapping mechanism in FETs and the SRH-based trap model developed in [117] and [118].

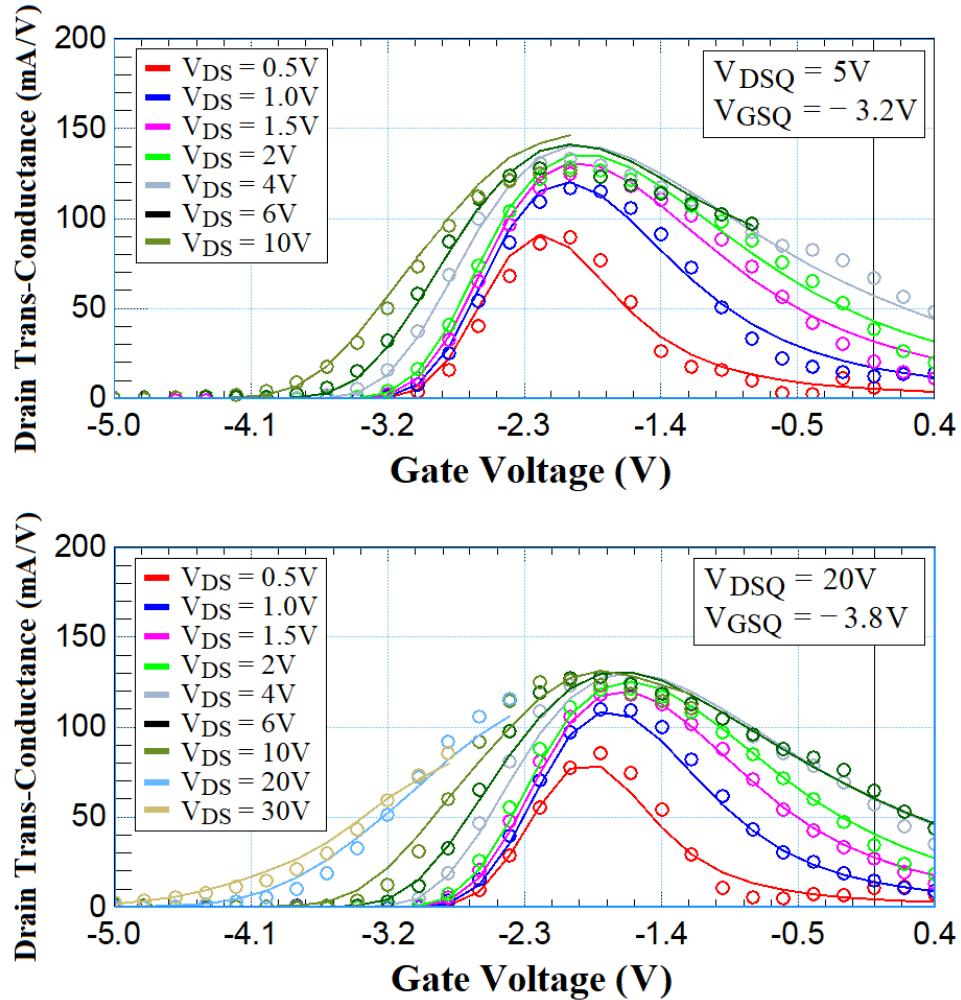


Figure 7.8: Measured (symbol) and modeled (solid line) pulsed transfer characteristics for the two quiescent bias points indicated in the legends. The drain voltages are also indicated in the legends.

7.3.1 Rates Of Charge Capture And Emission At A Trap Center

There exists four competing processes for hole and electron capture and emission at the energy level E_x of a trap center. These processes are electron capture, electron emission, hole capture and hole emission. In a Shockley-Read-Hall (SRH) trapping process [121], which is the concern of this chapter, these processes are governed by Fermi-Dirac statistics. There is a rate associated with each process. These rates are defined, respectively, as the rate of electron capture from the conduction band, R_{cn} , the rate of electron emission to

the conduction band, R_{en} , the rate of hole capture from the valence band, R_{cp} , and the rate of hole emission to the valence band, R_{ep} .

Let n_x [m^{-3}] and p_x [m^{-3}] denote, respectively, the concentrations of the captured electrons and holes at a trap center. For a unit volume of material, the net rate of electron accumulation at the energy levels of a trap center is given by

$$dn_x/dt = U_n - U_p, \quad (7.1)$$

where $U_n \equiv R_{cn} - R_{en}$ and $U_p \equiv R_{cp} - R_{ep}$ are, respectively, the total rate of electron and hole capture at E_x , and are given by [121]

$$U_n = e_n [p_x \exp(\phi_n) - n_x] \text{ and} \quad (7.2)$$

$$U_p = e_p [n_x \exp(\phi_p) - p_x], \quad (7.3)$$

where e_n [s^{-1}] and e_p [s^{-1}] are, respectively, the characteristic frequencies of electron and hole emissions, and

$$\phi_n \equiv (F_n - E_x)/kT \text{ and} \quad (7.4)$$

$$\phi_p \equiv (E_x - F_p)/kT, \quad (7.5)$$

where F_n [eV] and F_p [eV] are, respectively, the quasi-Fermi-levels for electrons and holes, k [J/K] is the Boltzmann constant and T [K] is temperature.

If a trap center is an acceptor*, then (7.1) corresponds to the ionization rate of a trap center, and if it is a donor†, then (7.1) corresponds to the de-ionization rate of a trap center.

*An acceptor trap center is a trap center which is neutral when all the energy levels of the trap center are empty, and negatively charged and, therefore, ionized, when one or more energy levels of the trap center are occupied by electrons.

†A donor trap center is a trap center that is neutral when all the energy levels of the trap center are occupied by electrons, and positively charged and, therefore, ionized, when one or more energy levels of the trap center are empty.

7.3.2 Control Potential Of A Trap Center

The concentrations of electrons and holes available for capture at a trap center, denoted respectively as n [m^{-3}] and p [m^{-3}], are given by [122]

$$n = \hat{n} \exp(\phi_n) \quad \text{and} \quad (7.6)$$

$$p = \hat{p} \exp(\phi_p), \quad (7.7)$$

where \hat{n} [m^{-3}] is the concentration of the electrons in the conduction band when F_n falls at E_x , and \hat{p} [m^{-3}] is the concentration of the holes in the valence band when F_p falls at E_x . From (7.2) and (7.3), ϕ_n and ϕ_p act as controlling potentials for the net rate of electron accumulation at a trap center, normalized to the thermal energy kT . From (7.6) and (7.7), ϕ_n and ϕ_p act as controlling potentials for the available charge for capture at a trap center. This leads to an interpretation of the terms ϕ_n and ϕ_p as the normalized control potentials of a trap center to the thermal energy (in eV). For simplicity, ϕ_n and ϕ_p will be referred to as the control potentials of a trap center.

7.3.3 Current Injection Into A Trap-Center Region

The injection of electrons and holes into a trap center modifies the Fermi levels F_n and F_p at the trap center and, consequently, modifies the control potentials ϕ_n and ϕ_p of the trap center. Let n_o [m^{-3}] and p_o [m^{-3}] be, respectively, the densities of the electrons and holes available for capture at a trap center before carrier injection, and n_J and p_J be, respectively, the densities of the injected electrons and holes in the trap-center region. The densities of the electrons and holes available for capture at a trap center after carrier injection is then given by $n = n_o + n_J$ and $p = p_o + p_J$. Let I_n [A] and I_p [A] be, respectively, the currents of injected electrons and holes into the trap center. The concentrations n_J

and p_J are linearly related to the currents I_n and I_p [‡]. From (7.6) and (7.7), the control potentials of a trap center in the presence of carrier injection are given by

$$\phi_n = \ln \left(n_o / \hat{n} + \alpha_n I_n \right) \text{ and} \quad (7.8)$$

$$\phi_p = \ln \left(p_o / \hat{p} + \alpha_p I_p \right), \quad (7.9)$$

where α_n and α_p are constants. In FETs, the terms n_o , p_o , I_n and I_p are all functions of the gate-source and gate-drain terminal potentials, V_{GS} and V_{GD} , of the FET.

7.3.4 Circuit Model Of A Trap Center

Depending on the bias condition, a trap center can either act as an electron or hole trapping center or as a carrier generation or recombination center. The criteria for electron trapping, hole trapping, carrier recombination and carrier generation are given, respectively, by [122]

$$R_{cp} \ll R_{en} \quad \text{and} \quad R_{cn} \gg R_{ep}; \quad (7.10)$$

$$R_{cp} \gg R_{en} \quad \text{and} \quad R_{cn} \ll R_{ep}; \quad (7.11)$$

$$R_{cp} \gg R_{en} \quad \text{and} \quad R_{cn} \gg R_{ep}; \quad \text{and} \quad (7.12)$$

$$R_{cp} \ll R_{en} \quad \text{and} \quad R_{cn} \ll R_{ep}. \quad (7.13)$$

In general, depending on the bias condition, a trap center, regardless of its polarity, being an acceptor or a donor, acts either as an electron or hole trapping center or as a generation or recombination center. The following describes the comprehensive model of a trap center in an FET developed in [118], suitable for circuit simulators, that can capture the trapping behavior at various bias conditions.

[‡]Consider, for instance, a sheet of trap centers. Let A_X [m^2] be the cross-sectional area perpendicular to the direction of the “injected” current. The currents I_n and I_p are related to n_J and p_J by $I_n = (v_n q A_X) n_J$ and $I_p = (v_p q A_X) p_J$, where v_n [m/s] and v_p [m/s] are the drift velocities of the injected electrons and holes respectively.

A trap capacity per-unit-volume C_x [F m^{-3}] can be defined in terms of a trapping potential v_x [V] and the concentration of the electrons n_x in the trap center as follows:

$$C_x = (-q) n_x / v_x, \quad (7.14)$$

where q [C] is the electron charge. The dynamics of the charge density n_x can be described, substituting (7.14) in (7.1), by a current source i_x [A] driving the capacitor C_x to a potential difference of v_x :

$$i_x = (i_{cn} - i_{en}) - (i_{cp} - i_{ep}), \quad (7.15)$$

where $i_{cn} \equiv (-q) R_{cn}$ and $i_{en} \equiv (-q) R_{en}$ define electron-capture and electron-emission currents respectively, and $i_{cp} \equiv (-q) R_{cp}$ and $i_{ep} \equiv (-q) R_{ep}$ define hole-capture and hole-emission currents respectively. These currents are given by

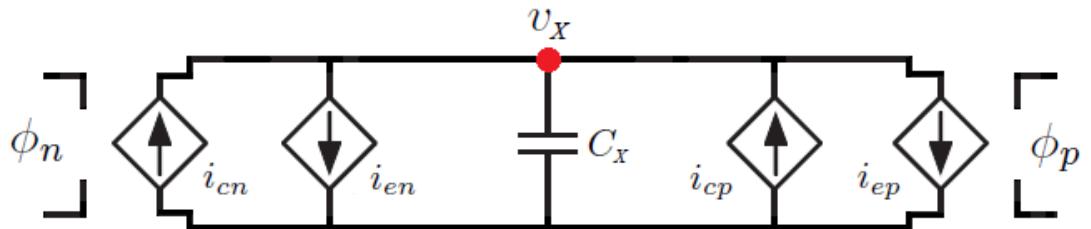


Figure 7.9: Circuit model for a trap center.

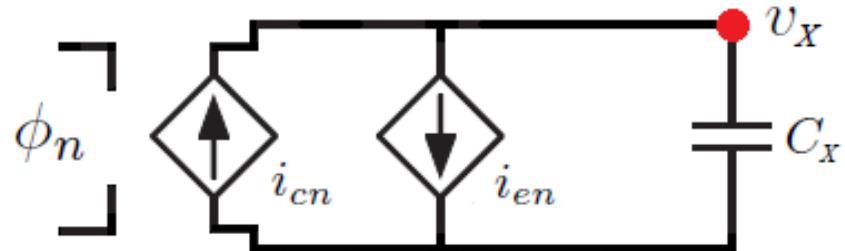


Figure 7.10: Circuit model for a trap center acting as an electron-trapping center.

$$i_{cn} = C_x e_n (V_x - v_x) \exp(\phi_n), \quad (7.16)$$

$$i_{en} = C_x e_n v_x, \quad (7.17)$$

$$i_{cp} = C_x e_p v_x \exp(\phi_p) \text{ and} \quad (7.18)$$

$$i_{ep} = C_x e_p (V_x - v_x), \quad (7.19)$$

where $V_x \equiv (-q N_x) / C_x < 0$ is the potential v_x when the energy levels of the trap center are fully occupied by electrons, where $N_x [\text{m}^{-3}]$ is the number per unit volume of the energy levels E_x at a trap center, and is such that $N_x = n_x + p_x$. If the trap center is an acceptor, then its trapping potential v_x is directly proportional to its ionization density n_x , whereas if the trap center is a donor, then, using (7.14) and the relation $n_x + p_x = N_x$, the potential $v_x - V_x$ is directly proportional to its ionization density p_x . The circuit model is shown in Fig. 7.9.

7.3.5 Steady-State Response

In a steady-state condition, the total emission and capture current i_x (7.15) into a trap center is zero. This leads to the following relation between the trapping potential v_x at a steady-state condition, denoted as \bar{v}_x , and the control potentials ϕ_n and ϕ_p :

$$\bar{v}_x = \frac{[1 + \exp(\phi_n + \varepsilon)]}{[1 + \exp(\phi_n + \varepsilon)] + \eta [1 + \exp(\phi_p - \varepsilon)]} V_x, \quad (7.20)$$

where $\eta \equiv e_n/e_p$ and $\varepsilon \equiv \ln(\eta)$.

7.3.6 Circuit Model For An Electron-Trapping Center

The measurement results of Fig. 7.3 suggest that the observed dispersion in the I-V characteristics of the device under test is caused by a trapping process at an acceptor-like trap center in the channel and access regions of the active GaN layer. Trapping

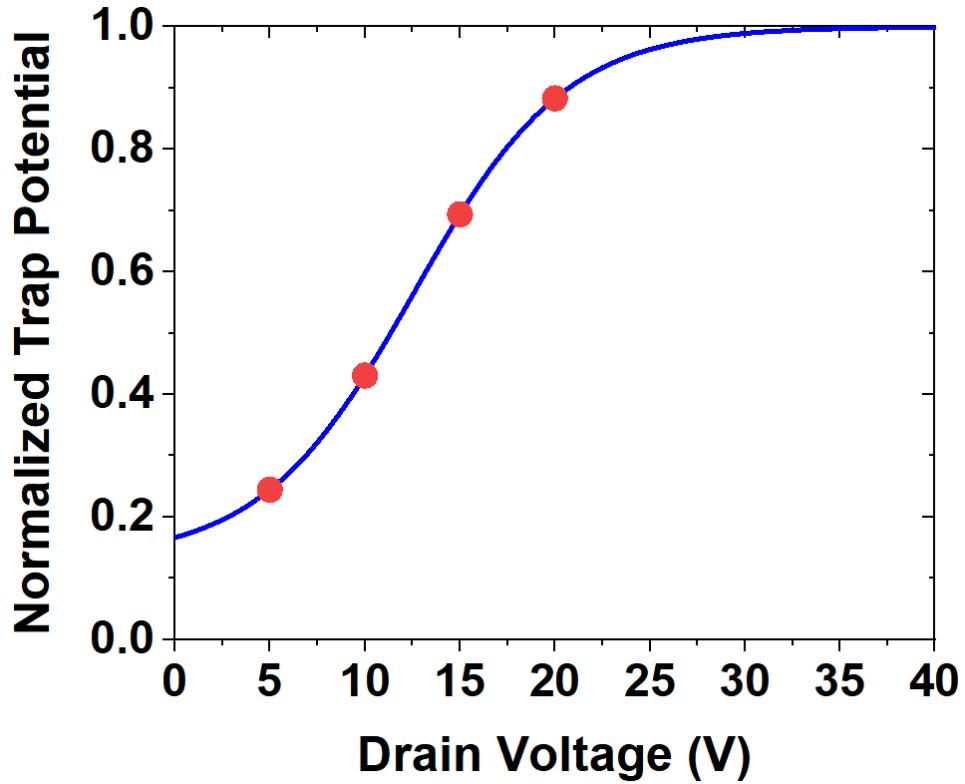


Figure 7.11: The steady-state potential of the trap center in the device under test, normalized to V_X , which is the potential of the trap center when it is fully ionized. The red symbols correspond to the trap potentials at the quiescent bias conditions at which the device under test was held in the pulse measurements. The blue line shows the trap potential at all the drain voltages, ranging from 0 V to 40 V, at which the DC characteristics of the device were measured. The trap potential at zero drain voltage is the initial potential of the trap center in the absence of current injection into the trap center, which is then modified by the current injected into the trap center after turning ON the device. The parameter $D \equiv n_o/\hat{n}$ in (7.22) controls the initial state of the trap center.

was observed for quiescent bias points at which the device was ON, suggesting that the trapping process is triggered by the electrons of the channel which are injected into the trap center through tunneling. This rules out the reverse biased Schottky gate tunneling current mechanism which was discussed earlier in section Section 7.2. It is plausible, therefore, to assume that in the region of operation of the device, the trap center is behaving as an electron trap center. This assumption is further justified by the reasonable

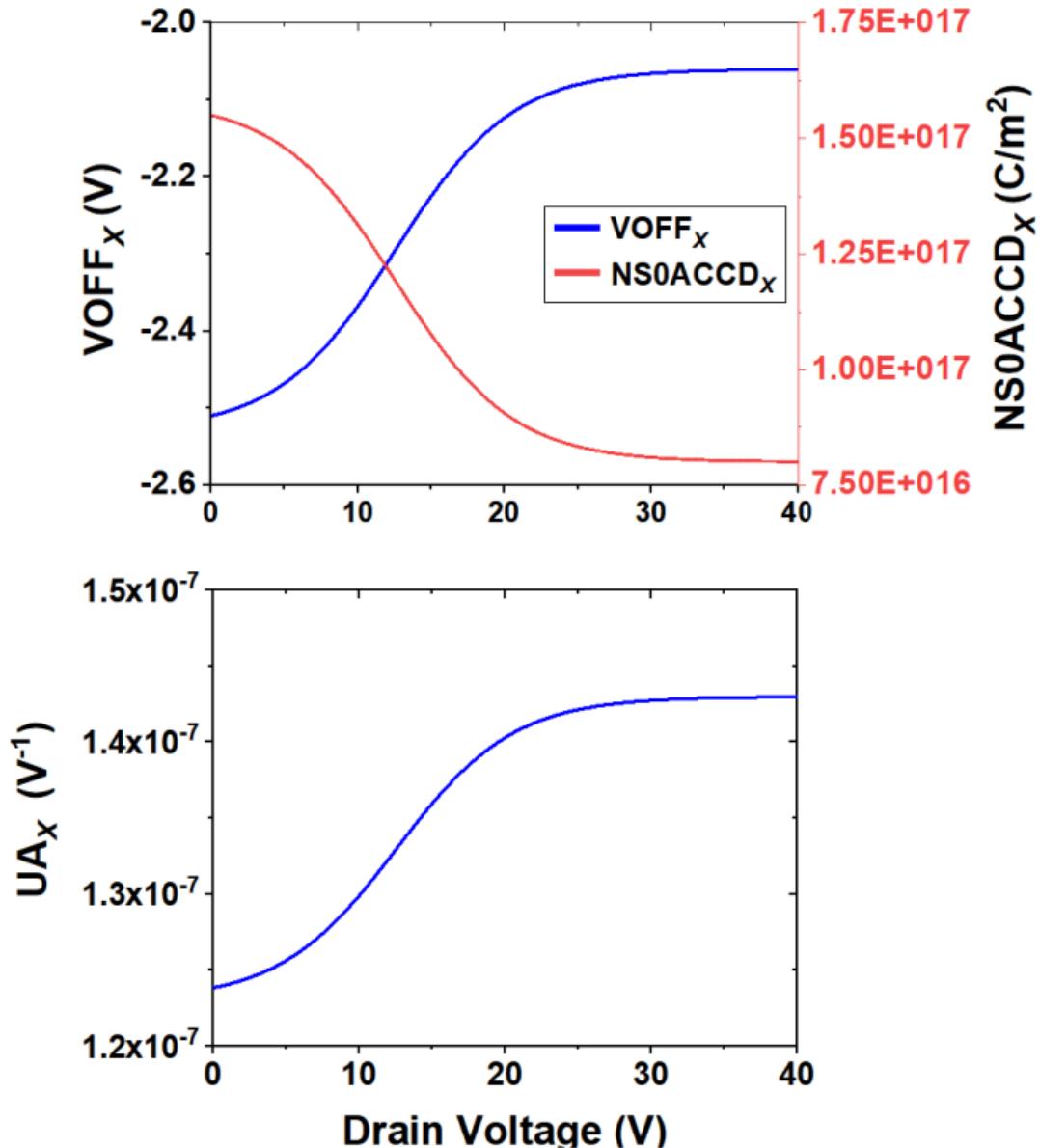


Figure 7.12: The variations of VOFF_X , UA_X and NS0ACCD_X , described by (7.23), (7.24) and (7.25) respectively, with drain voltage.

fit we obtained to the measured data by modeling the observed dispersion assuming that, in the region of operation of the device, the trap center is an electron trapping center.

When the condition of electron trapping (7.10) is satisfied, (7.20) simplifies to

$$\bar{v}_x = V_x / [1 + \exp(-\phi_n)] . \quad (7.21)$$

We can reach this equation by setting the parameter e_p (the characteristic frequency of hole emission) of the trap center to zero. This then simplifies the circuit model of Fig. 7.9 to the one shown in Fig. 7.10.

7.4 Discussion

It is possible to model the observed complicated trapping behaviour in the measured results of Section 7.2 by considering a trap center with a steady-state potential of the form

$$\bar{v}_x = \frac{V_x}{1 + \frac{1}{\exp(AV_{GS} + BV_{DS} + C) + D}}, \quad (7.22)$$

where $A = 0$, $B = 0.25$, $C = -3$ and $D = 0.15$ and letting the trap potential modify the three parameters VOFF, UA and NS0ACCD of the ASM model in a linear manner as:

$$\text{VOFF}_x = \text{VOFF} + \kappa_1 \tilde{v}_x, \quad (7.23)$$

$$\text{UA}_x = \text{UA} + \kappa_2 \tilde{v}_x \quad \text{and} \quad (7.24)$$

$$\text{NS0ACCD}_x = \text{NS0ACCD} + \kappa_3 \tilde{v}_x, \quad (7.25)$$

where $\tilde{v}_x = v_x/V_x$ is the normalized trap potential, $\text{VOFF} = -2.6$, $\kappa_1 = 0.54$, $\text{UA} = 120 \times 10^{-9}$, $\kappa_2 = 23 \times 10^{-9}$, $\text{NS0ACCD} = 1.7 \times 10^{17}$ and $\kappa_3 = -9 \times 10^{16}$. This implies that first-order modification to VOFF, UA and NS0ACCD is sufficient to capture the effect of trapping. The variations of VOFF_x , UA_x and NS0ACCD_x with drain voltage is illustrated in Fig. 7.12.

In a pulse measurement, the trap potential that modifies the electrical performance of the device is a single potential given by (7.22) where V_{GS} and V_{DS} are the quiescent gate and drain potentials. In a DC measurement, the trap potential which modifies the electrical performance of the device varies with the bias point. The simulation results

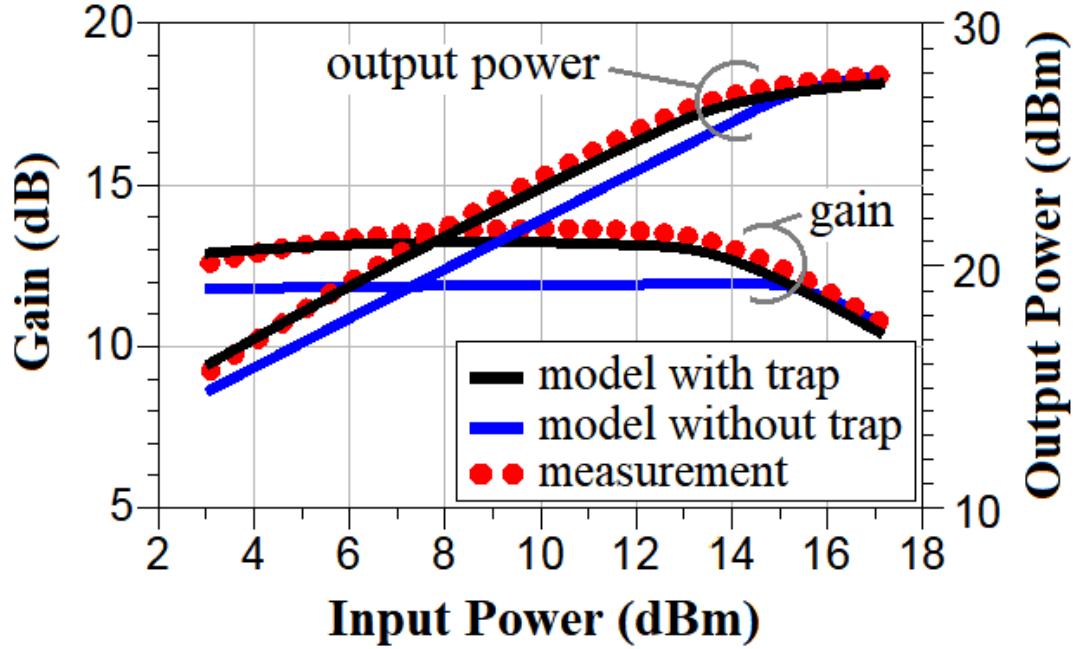


Figure 7.13: High frequency (10 GHz) large signal RF validation of the model presented in this work for a quiescent operating point of $(V_{DS}, V_{GS}) = (15 \text{ V}, -3.6 \text{ V})$ and optimal complex load condition.

with the parameters listed above are shown in Figs 7.1, 7.2, 7.3, 7.5, 7.6, 7.7 and 7.8. Also, high frequency (10 GHz) large signal RF validation of the model for a quiescent operating point of $(V_{DS}, V_{GS}) = (15 \text{ V}, -3.6 \text{ V})$ and for optimal complex load condition is shown in Fig. 7.13.

The above steady-state form for the trap potential, which is illustrated in Fig. 7.11, can be explained theoretically in the following manner. There exists an acceptor-like trap center in the device under test which, in the region of operation of the device, behaves as an electron trap center. The current injected into the trap center is the current composed of the electrons of the channel which are injected toward the trap center by a tunneling process, and so have an exponential dependence on the terminal potentials:

$$I_n = I_o \exp(AV_{GS} + BV_{DS}), \quad (7.26)$$

where I_o , A and B are constants. The measurement results show negligible dependence

on the gate-source potential, so we can set $A = 0$. The control potential ϕ_n , given by (7.8), becomes, using (7.26),

$$\phi_n = \ln [\exp (BV_{DS} + C) + D], \quad (7.27)$$

where $C \equiv \ln (\alpha_n I_o)$ and $D \equiv n_o/\hat{n}$. Substituting (7.27) in (7.21) we recover (7.22).

In order to find the model parameters of the ASM-GaN model that are affected by the trap potential, we took the following approach. We considered the output and transfer characteristics for one of the quiescent bias points (in particular $(V_{DSQ}, V_{GSQ}) = (20\text{V}, -3.8\text{V})$) as a reference set of characteristics. Self-heating in the ASM-GaN model was turned off, and the model parameters for the ASM-GaN model were optimized to obtain a reasonable fit to the reference output and transfer characteristics. The measurement results of Fig. 7.3 clearly show that there is a shift in the threshold voltage with quiescent drain voltage, so we began by tuning VOFF of the model to obtain reasonable fits to the output and transfer characteristics for the other quiescent conditions. However, we found that to obtain the excellent fits shown in Figs 7.3, 7.5 and 7.6, NS0ACCD and UA must also be tuned. We then turned on the self-heating process in the ASM model and fine tuned some of the parameters of the ASM model for a global optimization for the set of parameters which give excellent fits to both DC, shown in Fig. 7.1, and pulsed output and transfer characteristics.

We extracted the parameters of the trap model in the following manner. We plotted the parameters VOFF, UA and NS0ACCD versus quiescent bias point, and by fitting to these curves an equation of the form given by (7.22) we extracted the parameters A , B , C of (7.22) and the parameters κ_1 , κ_2 and κ_3 of (7.23), (7.24) and (7.25).

7.5 Conclusion

A comprehensive model for GaN HEMTs was presented in this chapter which combines the ASM-GaN model with a Shockley-Reed-Hall based trap model. This model was validated against results of DC and pulsed DC measurements performed on a commercially available d-mode GaN HEMT. Trapping behavior of the device under test was captured by including an SRH-based model of an acceptor trap center in the ASM-GaN model, which behaves, in the region of operation of the device, as an electron trap center, and is triggered by an electron current composed of the electrons which are injected from the channel through tunnelling into the trap center. Excellent fit to the measurement results was obtained over a large range of quiescent bias points and gate and drain voltages.

8

Extreme Environment Modeling Of AlGaN/GaN HEMTs

“Nature prefers the more probable states to the less probable because in nature processes take place in the direction of greater probability. Heat goes from a body at higher temperature to a body at lower temperature because the state of equal temperature distribution is more probable than a state of unequal temperature distribution.”

– Max Plank

8.1 Introduction

In the last chapter, we modeled the charge trapping phenomenon present in a commercially available GaN HEMT. This chapter further utilizes the trapping model developed and implemented in ASM-GaN to model the extreme environment conditions that these devices might end up operating in. The deterioration in a HEMT’s characteristics due to extreme environment operation is further exacerbated by the recent trend which shows

increasingly aggressive scaling[123–125] of GaN HEMTs. At one hand, this aggressive scaling has resulted in very promising high-speed devices with gate lengths as small as 20 nm and f_T/f_{max} exceeding 400 GHz [126], however it also results in increased electric field inside the HEMTs, which can accelerate any degradation mechanism originating from a particular extreme environment such as a nuclear plant or an internal combustion engine. Furthermore, the problem of increased electric field in the channel and access regions can arise from a different source besides scaling - GaN power devices which can reliably operate with very high drain-source voltage (V_{DS}) values of 600-650 V are widely available, where they set the current benchmark for commercial GaN power devices. Such devices too will face extra degradation due to increased V_{DS} when additionally coupled with extreme environments existing in particular applications. Current research [127–129] indicates that the focus for GaN power devices is aimed towards increasing device reliability whilst achieving V_{DS} values in the kilovolt (KV) range.

While these technology trends bode well for the future of GaN based technologies, there are certain device modeling challenges which arise with such advancements, especially when these devices are operated in following extreme environments, which have been addressed in this chapter:

1. One such challenge relates to extreme-temperature modeling of these devices. Such extreme temperatures exceeding values of 500 °C and more can be easily reached in certain niche applications such as automotives, turbine engines, and Venus and Mercury inter-planetary missions[18, 130, 131]. It has been discussed in section 1.3 of chapt.1 that Si based conventional MOSFETs can work till a maximum of 300 °C due to their lower band gap, while wide band gap semiconductors such as GaN can theoretically be operated beyond 600 °C. The modeling of these devices at these extreme temperatures remains a challenge to be solved using shift in appropriate model parameters based on sound physical understanding of the underlying physics.

2. Another challenge is when these devices are operated in nuclear radiation rich environment, where they might be subjected to a plethora of different types of radiations such as fluxes of neutrons or gamma rays, when used in radiation-hard electronics for nuclear or military systems, to fluxes of high energy protons and electrons when used in low earth orbit satellites[132]. This is shown in the device schematic of Fig. 1.3, where a boundary condition that dictates an absence of any external source of electromagnetic field other than electrical supplies (both AC and DC) and absence of any radiation source is imposed in order to define the device modeling problem. However, for extreme environment conditions such as nuclear plants or space applications, the device can no longer be considered perfectly isolated. Under such circumstances, in order to model the degradation in device's performance, we have to consider the effects of external fields/particles on the various, physically grounded model parameters of the device that show maximum sensitivity to the measured degraded characteristics, by relaxing the boundary condition described above.

From the above discussion, it can be inferred that the problem of modeling the measured characteristics at extreme temperatures and the degradation effects due to radiation exposure of a HEMT device are similar when it comes to the device level (physical) changes, which are represented by the corresponding shift in model parameters. These model parameters represent the physical phenomena which respond to these external stimuli (temperature, radiation etc). Examples of such model parameters could be the threshold voltage (which represents the barrier voltage and charge in between the gate and 2DEG channel), mobility (which represents the ease with which carriers can drift along the applied electric field), access region densities (which represent the amount of free 2DEG charge in the access regions available for conduction) etc.

High temperature operation of AlGaN/GaN HEMTs up to 500 °C has been attempted

in [133–138] using both Si and Sapphire as substrates. At the same time, there have been reports of analytical modeling of the high temperature operation of these HEMTs using hydrodynamic equations[139], Monte Carlo simulations of electron transport in GaN[140] and charge control analysis[141]. Measurement results of the DC characteristics of a GaN HEMT device fabricated at Stanford’s XLab across a wide temperature range from 22 °C to 500 °C [138] show a need for modifying the temperature-scaling equations of the model parameters of ASM-GaN compact model, in order to model GaN HEMTs operating at these extreme temperatures.

On the other hand, an extensive study was carried out on the effect of proton irradiation on the DC and Radio Frequency (RF) characteristics of two different AlGaN/GaN HEMTs in [142]. In particular, the effects of 1.8-MeV proton irradiation up to a fluence of $10^{14} \frac{1}{\text{cm}^2}$ on different electrical parameters, such as *S*-parameters, current gain, current-gain cutoff frequency (f_T), and maximum oscillation frequency (f_{max}) of AlGaN/GaN HEMTs were reported. It was shown that the devices under test exhibit degradation in their DC and RF characteristics. These degradations were attributed to creation of deep acceptor-like traps, causing a positive shift in the pinch-off or threshold voltage and a drop in the ON-state current.

By varying three model parameters of the ASM-GaN model, namely the threshold/cut-off voltage (VOFF) and the densities of the two-Dimensional Electron Gas (2DEG) in the source and drain access regions of the device (NS0ACCS and NS0ACCD or NS0ACC in general for access region 2DEG carrier density), we were able to fit the different DC I-V characteristics for -

1. the extreme temperatures ranging from 22 °C to 500 °C, for measurements performed on an AlGaN/GaN HEMT manufactured and characterized at XLab, Stanford[138], with the additional temperature dependence of low-field surface mobility (U0), saturation velocity (VSAT) and contact resistance (RC),

&

2. those measurements performed on two sets of AlGaN/GaN HEMTs, both of which were irradiated with 1.8-MeV protons to a maximum fluence of $10^{14} \frac{1}{\text{cm}^2}$. The first set consisted of HEMTs fabricated with Ga rich environment and the second set consisted of HEMTs fabricated with NH₃ rich environment, both existing as a part of the MBE (Molecular Beam Epitaxy) growth process of AlGaN/GaN hetero-structures on 4H-SiC substrates[142].

In order to maximize the utility of GaN transistors in power electronics and RF domains, their accurate and speedy simulation is needed. Both these metrics of circuit simulation, i.e., accuracy and speed, are determined by the compact model describing the device. Many empirical models have been proposed for GaN HEMTs, but they are not physics-based in nature [143, 144]. Physics-based models [45, 46, 67, 145] have the intrinsic advantage of having few parameters. These parameters are directly or indirectly linked to the physical effects governing the device dynamics. Hence, their extraction in a physics-based model is relatively easier than in the other models. The ASM-GaN physics-based compact model [45, 46, 67] has recently been selected by the compact-model-coalition standardization process as an industry standard model for GaN devices. The model showcases as a promising tool for improving the accuracy and versatility of today's power GaN-based circuit simulations. In addition to the core modeling of DC-IV and intrinsic capacitances, in the ASM-GaN compact model, flicker noise, thermal noise, gate current in AlGaN/-GaN HEMTs [146–148], trapping [46] and a capacitance model in the presence of different combinations of gate and source field plates [149, 150] are also modeled.

In this chapter, we enhance the ASM-GaN compact model to capture the observed variations in the characteristics of the device with temperature and nuclear radiation exposure. This chapter is organized as follows: Section 8.2 describes the structure of the XLab's device under test and presents the measurement results of the transfer charac-

teristics of this device at various temperatures. Sub-section 8.2.1 describes the modeling of the temperature dependencies of key model parameters of ASM-GaN model for the above device and presents an excellent fit of the enhanced model to the measurement results. Sub-section 8.2.2 presents the temperature simulation results of enhanced ASM-GaN model, and discusses several aspects of the modeling approach presented in this work. Section 8.3 describes the modeling due to creation of acceptor like traps in the GaN layer and the simulation vs measurement results for AlGaN/GaN HEMTs irradiated with proton particle radiation. Finally Section 8.4 draws conclusions based on the work done on extreme environment modeling.

8.2 XLab's HEMT Struture And Measurement Results

The various geometries associated with normally ON (d-type) AlGaN-GaN HEMT device fabricated at Stanford's XLab on Si substrate, used in this study, are as follows (please refer Fig. 2.2 for a well labeled 3D section of such a HEMT device):

- AlGaN-barrier thickness, $T_{BAR} = 30 \text{ nm}$
- Gate length, $L = 3 \mu\text{m}$
- Gate width, $W = 20 \mu\text{m}$
- Length of the gate-source access region, $L_{SG} = 7 \mu\text{m}$
- Length of the gate-drain access region, $L_{DG} = 7 \mu\text{m}$
- Number of gate fingers, $NF = 1$

We measured the DC drain-to-source current (I_{DS})-gate-to-source voltage (V_{GS}) (transfer) characteristics of the above device at a wide range of ambient temperatures (T),

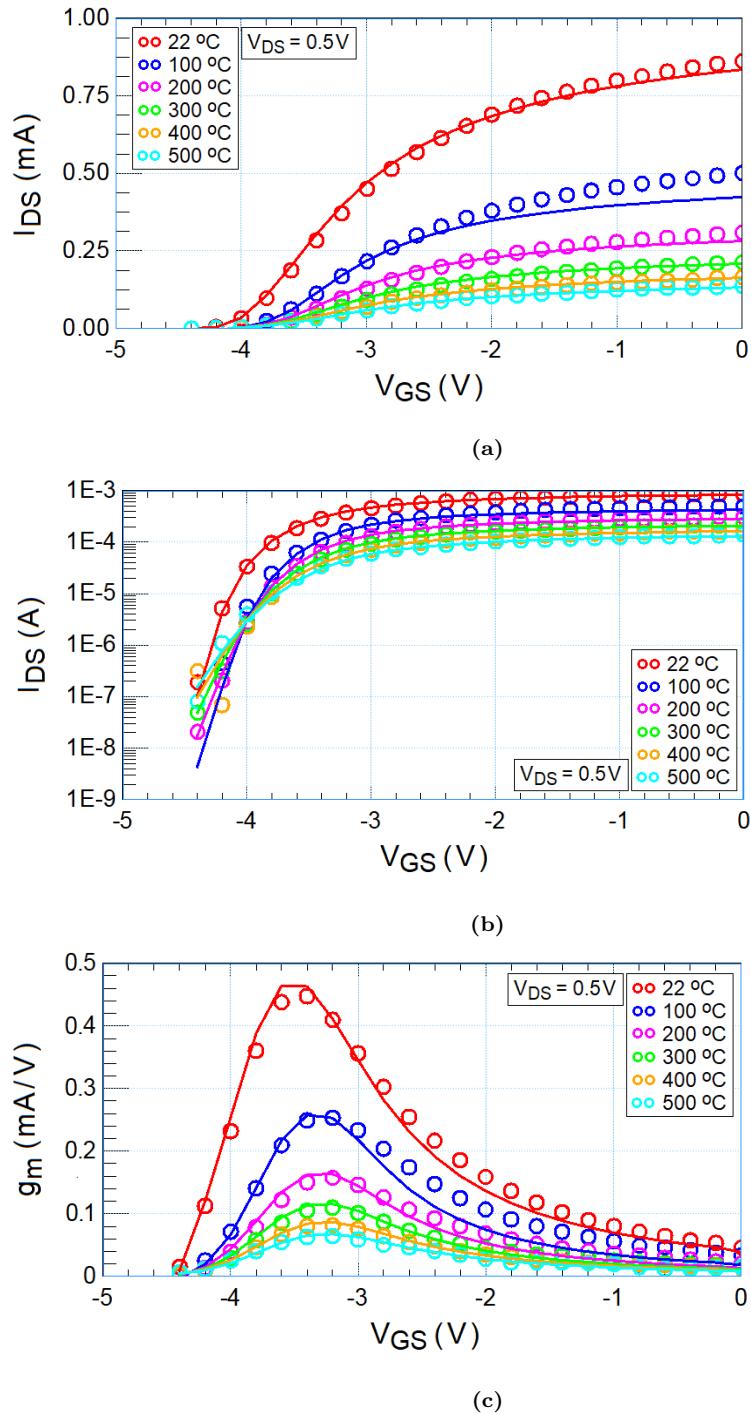


Figure 8.1: Measured (symbol) and simulated (line) (a) I_{DS} - V_{GS} characteristics in linear scale (b) I_{DS} - V_{GS} characteristics in semi-logarithmic scale (c) g_m - V_{GS} characteristics, for temperatures ranging from 22 °C to 500 °C, with V_{GS} varying from -4.4 V to 0 V and $V_{DS} = 0.5$ V.

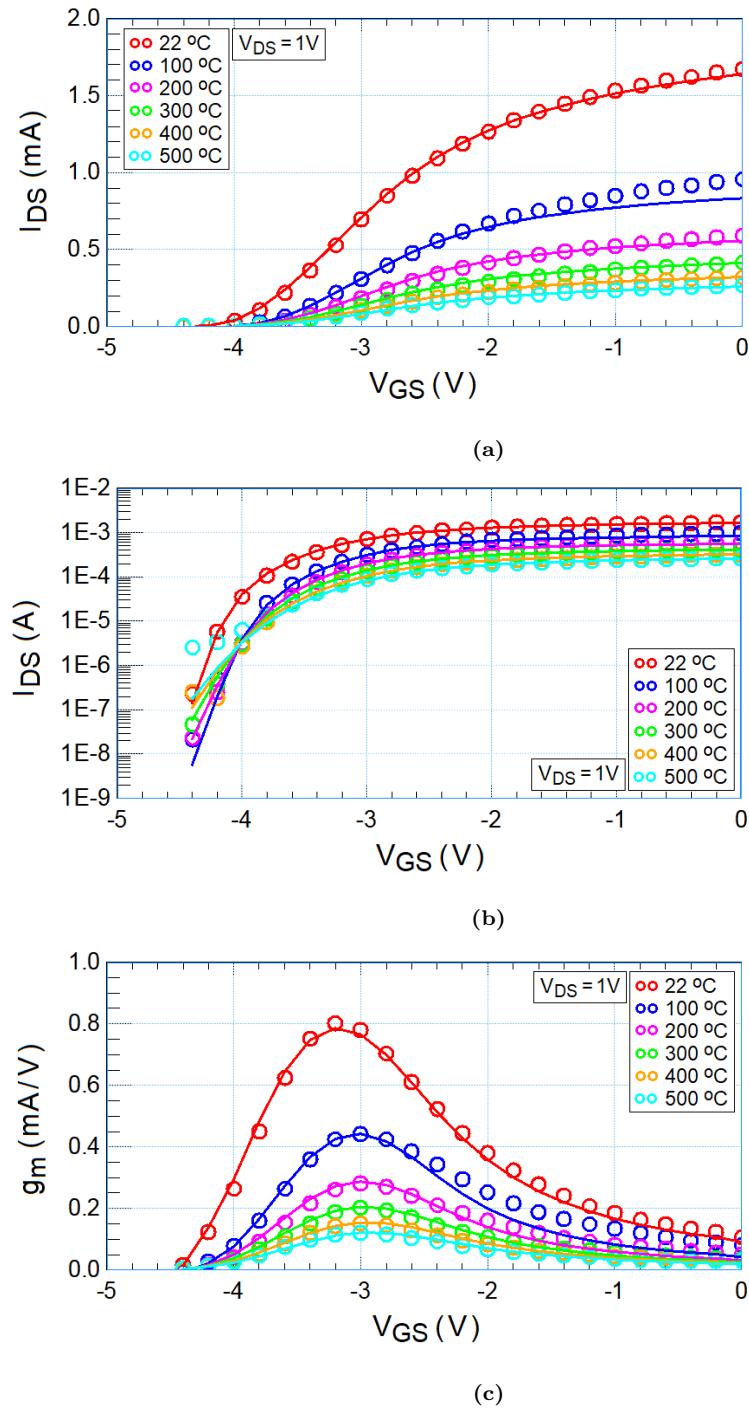


Figure 8.2: Measured (symbol) and simulated (line) (a) I_{DS} - V_{GS} characteristics in linear scale (b) I_{DS} - V_{GS} characteristics in semi-logarithmic scale (c) g_m - V_{GS} characteristics, for temperatures ranging from 22 °C to 500 °C, with V_{GS} varying from -4.4 V to 0 V and $V_{DS} = 1\text{ V}$.

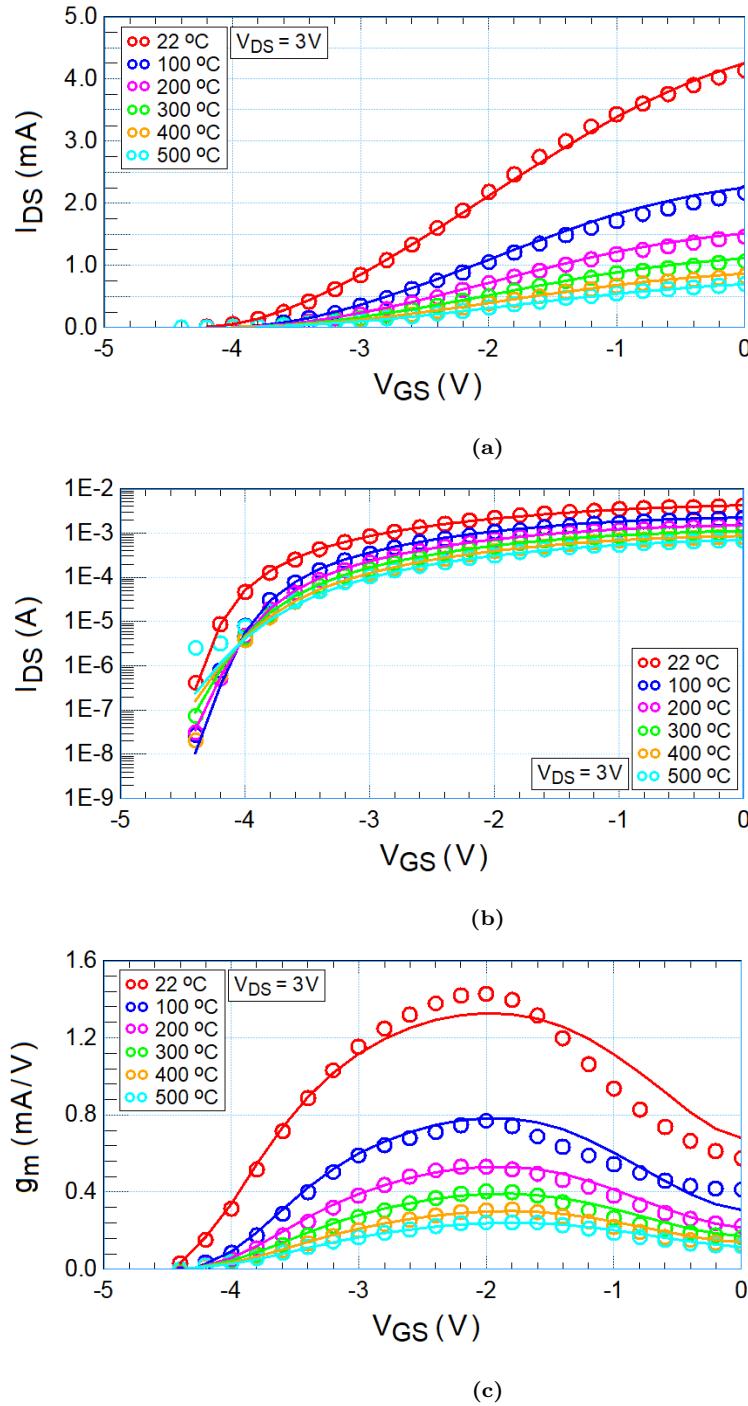


Figure 8.3: Measured (symbol) and simulated (line) (a) I_{DS} - V_{GS} characteristics in linear scale (b) I_{DS} - V_{GS} characteristics in semi-logarithmic scale (c) g_m - V_{GS} characteristics, for temperatures ranging from 22 °C to 500 °C, with V_{GS} varying from -4.4 V to 0 V and $V_{DS} = 3$ V.

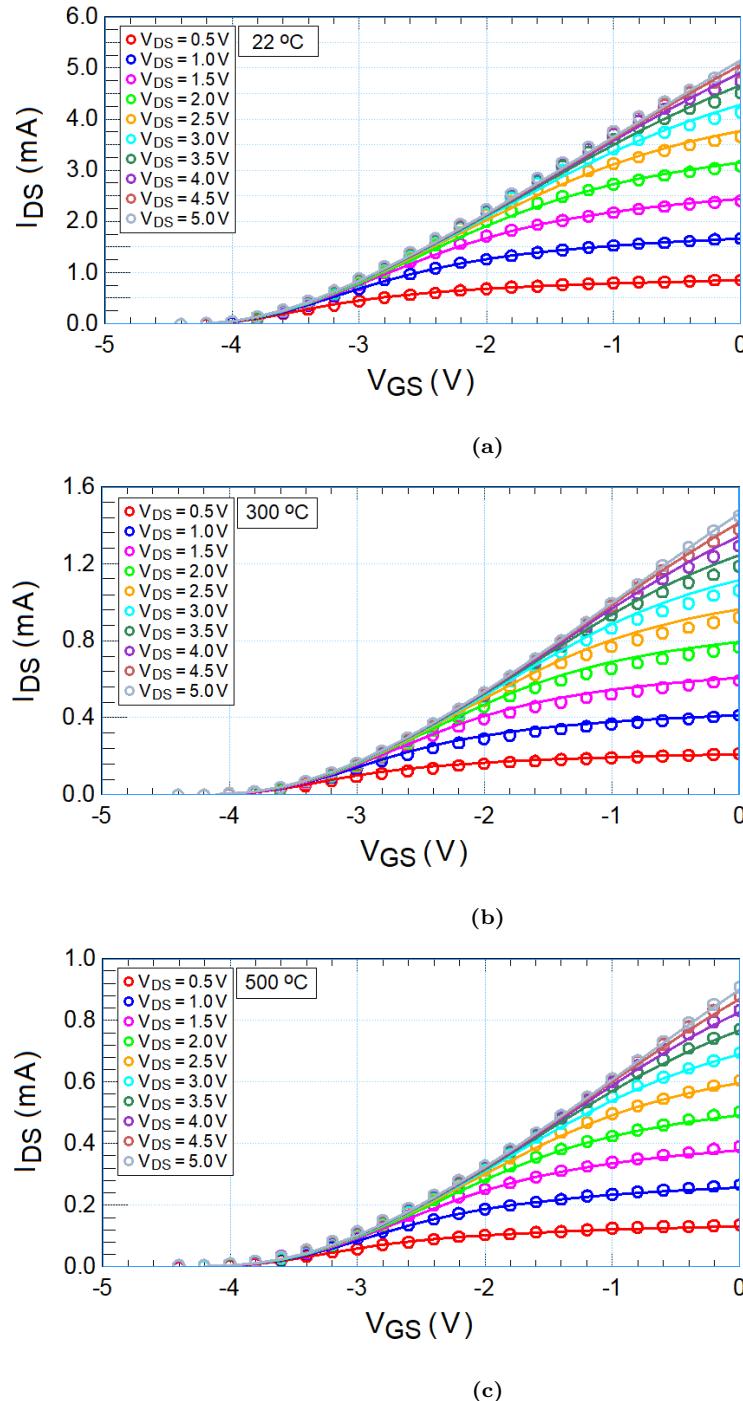


Figure 8.4: Measured (symbol) and simulated (line) I_{DS} - V_{GS} characteristics in linear scale, at ambient temperatures of (a) $T = 22$ °C (b) $T = 300$ °C (c) $T = 500$ °C, for drain-to-source voltages V_{DS} varying from 0.5 V to 5 V.

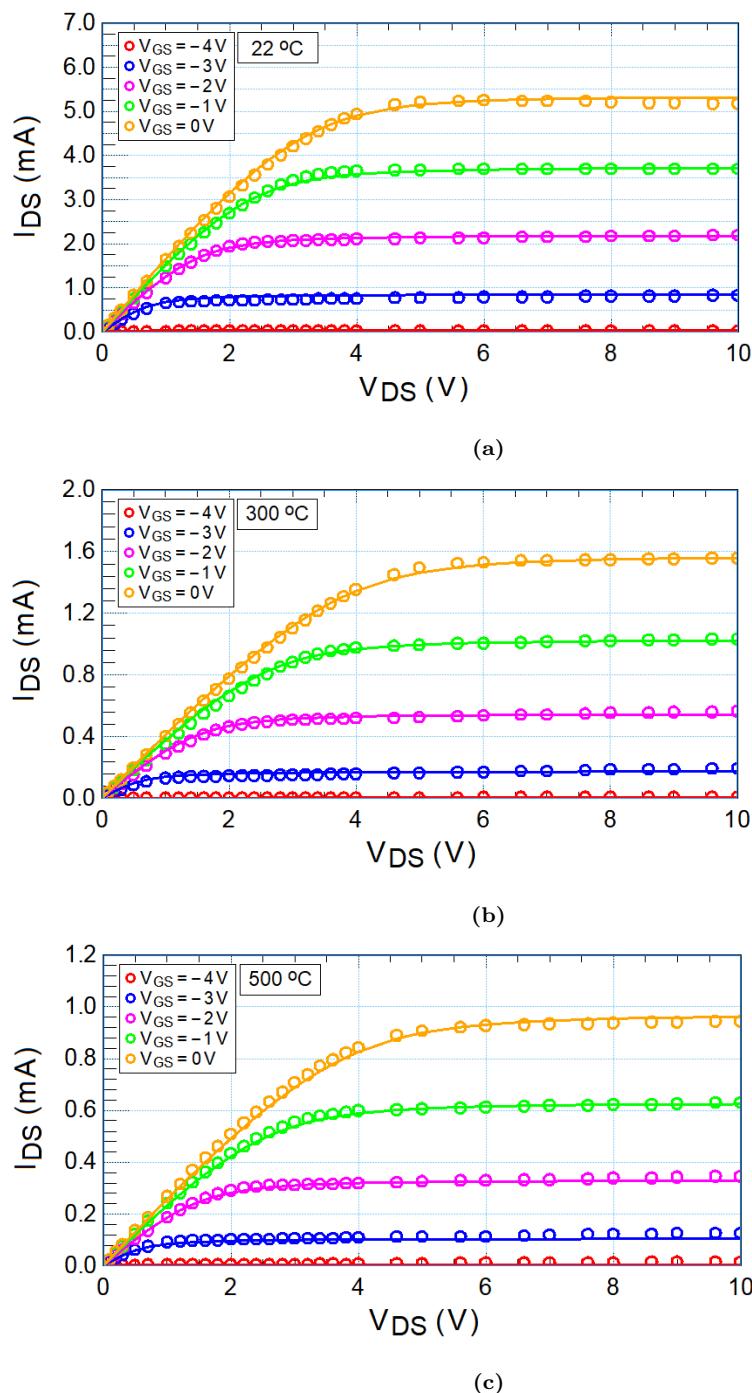


Figure 8.5: Measured (symbol) and simulated (line) I_{DS} - V_{DS} characteristics in linear scale, at ambient temperatures of (a) $T = 22^{\circ}\text{C}$ (b) $T = 300^{\circ}\text{C}$ (c) $T = 500^{\circ}\text{C}$, for gate-to-source voltages V_{GS} varying from -4 V to 0 V .

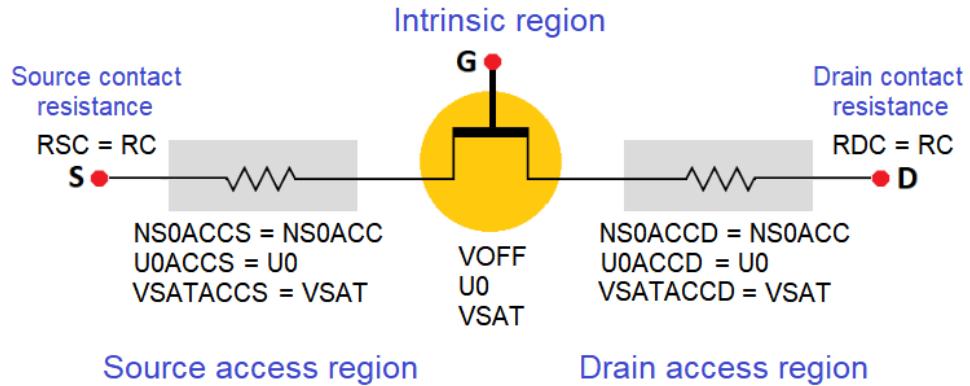


Figure 8.6: A schematic of the model used to describe the device under test, showing the temperature-dependent parameters associated with the different regions of the device.

ranging from $T = 22^\circ\text{C}$ to 500°C . The results are shown in Figs 8.1-8.5. Figures 8.1-8.3 show the measured transfer trans-conductance- V_{GS} characteristics for three different drain-to-source voltages (V_{DS}). Each figure shows the measured characteristics at various temperatures. Figure 8.4 shows the transfer characteristics at ambient temperatures $T = 22^\circ\text{C}$, 300°C and 500°C , for drain-to-source voltages ranging from $V_{DS} = 0.5\text{ V}$ to 5 V . Furthermore, Fig. 8.5 shows the I_{DS} - V_{DS} (output) characteristics at ambient temperatures $T = 22^\circ\text{C}$, 300°C and 500°C , for gate-to-source voltages ranging from $V_{GS} = -4\text{ V}$ to 0 V , and drain-to-source voltages ranging from $V_{DS} = 0\text{ V}$ to 10 V .

8.2.1 High Temperature Device Modeling Using ASM-GaN Compact Model

The ASM-GaN compact model in its current version incorporates temperature scaling equations for several model parameters, namely: the channel's threshold voltage (VOFF), the low-field carrier mobility (U_0) and saturation velocity (VSAT) in the intrinsic and the drain and source access regions of the HEMT, the drain and source access regions' carrier densities (NS0ACC), and the drain/source contact resistances (RC). The temperature

scaling equations for these model parameters are as follows:

$$\text{VOFF}_t = \text{VOFF} \left(1 - K_{T1} \Delta \bar{T} \right), \quad (8.1)$$

$$U0_t = U0 \bar{T}^{\text{UTE}}, \quad (8.2)$$

$$\text{VSAT}_t = \text{VSAT} \bar{T}^{\text{AT}}, \quad (8.3)$$

$$\text{NS0ACC}_t = \text{NS0ACC} \left(1 + K_{\text{NS0}} \Delta \bar{T} \right), \quad (8.4)$$

$$\text{RC}_t = \text{RC} \left(1 + K_{\text{RC}} \Delta \bar{T} \right), \quad (8.5)$$

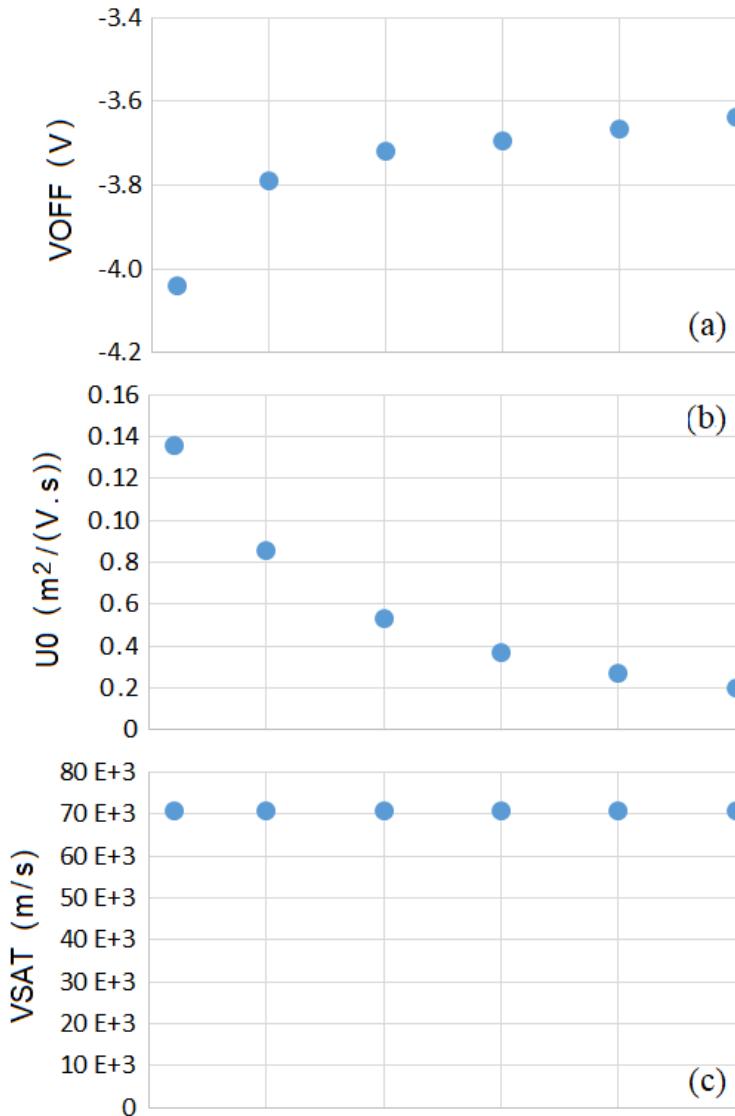
where

$$\bar{T} = T_{dev}/T_{nom}, \quad (8.6)$$

$$\Delta \bar{T} = T_{dev}/T_{nom} - 1, \quad (8.7)$$

where T_{dev} [K] is the device temperature, which is the ambient temperature T plus the temperature due to self-heating, T_{nom} [K] is the nominal temperature, VOFF, U0, VSAT, NS0ACC and RC are the model parameters at $T = T_{nom}$, and K_{T1} , UTE, AT, K_{NS0} and K_{RC} are temperature parameters.

A schematic of the model used to describe the device under test, showing the temperature-dependent parameters associated with the different regions of the device, is shown in Fig. 8.6. As can be noted, the source and drain access regions are modeled in an identical manner, setting the 2-DEG density in both regions, denoted as NS0ACCS and NS0ACCD, equal to NS0ACC. Moreover, the electron mobility and saturation velocity of the source and drain access regions are set equal to those of the intrinsic region: $U0ACCS = U0ACCD = U0$ and $VSATACCS = VSATACCD = VSAT$. Furthermore, the temperature parameters associated with NS0ACCS and NS0ACCD, denoted as K_{NS0S} and K_{NS0D} , are set equal to K_{NS0} , and the temperature parameters associated with the electron mobility and saturation velocity of the source and drain access regions are set equal to those of the intrinsic region: $UTES = UTED = UTE$ and $ATS = ATD = AT$. Similarly, the source



and drain access resistances are set equal to each other: $R_{SC} = R_{DC} = R_C$, and the temperature parameters associated with these two parameters are also set equal to each other: $K_{RSC} = K_{RDC} = K_{RC}$. All these different parameters have been introduced in the ASM-GaN model to capture possible non-idealities within the device.

Another aspect of temperature modeling in the current version of the ASM-GaN model is as follows. High lateral electric field in the channel results in the saturation of the velocity of the electrons in the channel. Velocity saturation is modeled by modifying the

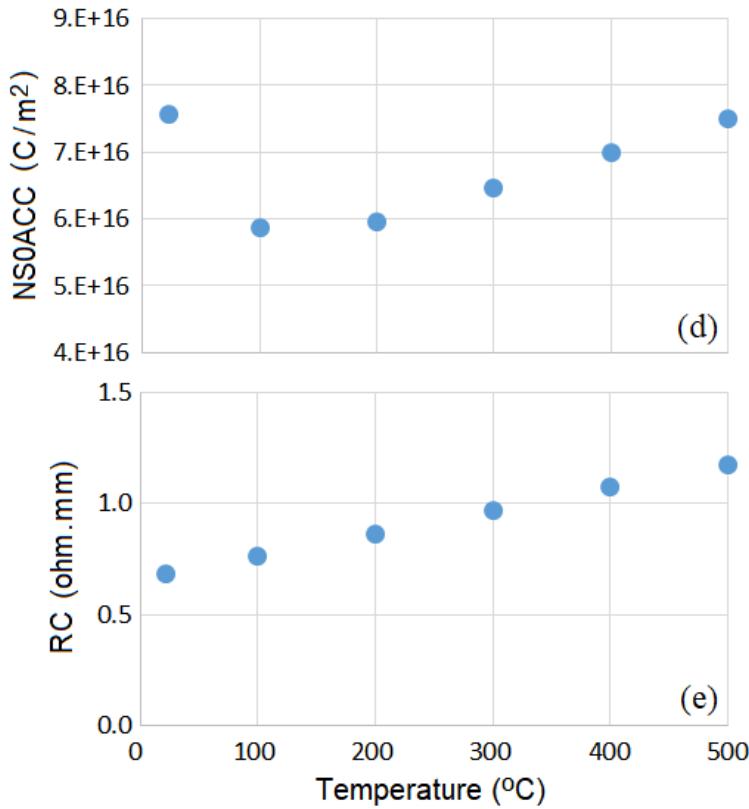


Figure 8.7: The extracted values of (a) VOFF (b) U0 (c) VSAT (d) NS0ACC for the device under test at $T = 22\text{ }^{\circ}\text{C}$, $100\text{ }^{\circ}\text{C}$, $200\text{ }^{\circ}\text{C}$, $300\text{ }^{\circ}\text{C}$, $400\text{ }^{\circ}\text{C}$ and $500\text{ }^{\circ}\text{C}$.

expression for mobility as [150]

$$\mu_{eff} = \beta_{||} (\beta_{\perp} U_{0t}), \quad (8.8)$$

where μ_{eff} is an effective mobility (which is different from the vertical effective mobility as defined in (2.10) by the factor of $\beta_{||}$, or in other words (2.10) defines the product $\beta_{\perp} U_{0t}$ in (8.8)), U_{0t} is the low-field mobility, and is given by (8.2), β_{\perp} is the mobility-degradation coefficient due to the vertical electric field in the channel, neglecting the lateral electric field in the channel, and $\beta_{||}$ is the mobility-degradation coefficient due to the lateral electric field in the channel, and is given by (and is same as the factor multiplying the numerator

Table 8.1: Extracted model parameters of the ASM-GaN model

Model Parameter	Description	Value
RTH0	Thermal Resistance (K/W)	25
EPSILON	Dielectric permittivity of AlGaN layer (F/m)	106.6×10^{-12}
VOFF	Cut-off voltage (V)	-4.04
NFACTOR	Sub-voff slope parameter	0.85
ETA0	DIBL Parameter	35.8×10^{-3}
VDSCALE	DIBL Scaling V_{DS}	2
U0	Low field mobility ($\text{m}^2/(\text{V.s})$)	135.5×10^{-3}
UA	Mobility degradation coefficient-first order	0
UB	Mobility degradation coefficient-second order	0
VSAT	Saturation velocity (m/s)	70.7×10^3
NS0ACC	2-DEG charge density in the Source/Drain access region (C/m^2)	7.8×10^{16}
RC	Source/Drain contact resistance ($\Omega.\text{m}$)	0.68×10^{-3}

of (2.12) & (2.13))

$$\beta_{\parallel} = \frac{1}{\sqrt{1 + \left(\frac{\beta_{\perp} U_{0t}}{V_{SAT_t}} E_{\parallel} \right)^2}}, \quad (8.9)$$

where V_{SAT_t} , given by (8.3), is the saturation velocity, and E_{\parallel} is the lateral electric field, which can be taken as

$$E_{\parallel} = (\psi_d - \psi_s) / L, \quad (8.10)$$

where ψ_d and ψ_s are the surface potentials at the drain end and the source end of the channel respectively, and L is the gate length. Using (8.10) in (8.9), (8.8) can be written

Table 8.2: Temperature parameters

Model Parameter	Description	Value
UTE	Temperature dependence of mobility	-1.975
AT	Temperature Dependence for saturation velocity	0
K _{RC}	Temperature dependence of Source (Drain) contact resistance	0.45
K _{T1}	Temperature dependence for VOFF	22 × 10 ⁻³
K _{NS0}	Temperature dependence for 2-DEG charge density at Source (Drain) access region	300.6 × 10 ⁻³

as

$$\mu_{eff} = \frac{\beta_{\perp} U0_t}{\sqrt{1 + [(\psi_d - \psi_s)/V_{Dsat}]^2}}, \quad (8.11)$$

where,

$$V_{Dsat} = \frac{VSAT_t L}{\beta_{\perp} U0_t}. \quad (8.12)$$

The term V_{Dsat} , which clearly is temperature dependent, is also used in the ASM-GaN model to calculate an effective drain-source potential

$$V_{Deff} = \frac{V_{DS}}{\sqrt{1 + (V_{DS}/V_{Dsat})^2}}, \quad (8.13)$$

which is used in place of the drain-source potential V_{DS} in the calculation of ψ_d . This has already been discussed in detail in sub-section 2.2.4 resulting in equations (2.19), (2.20) & (2.21). (8.13) can be retrieved by putting the exponent $\Delta = 2$ in (2.21).

The expression for μ_{eff} in (8.11) has been approximated in the ASM-GaN model as

$$\mu_{eff} = \frac{\beta_{\perp} U0_t}{\sqrt{1 + [\text{THESAT } (\psi_d - \psi_s)]^2}}, \quad (8.14)$$

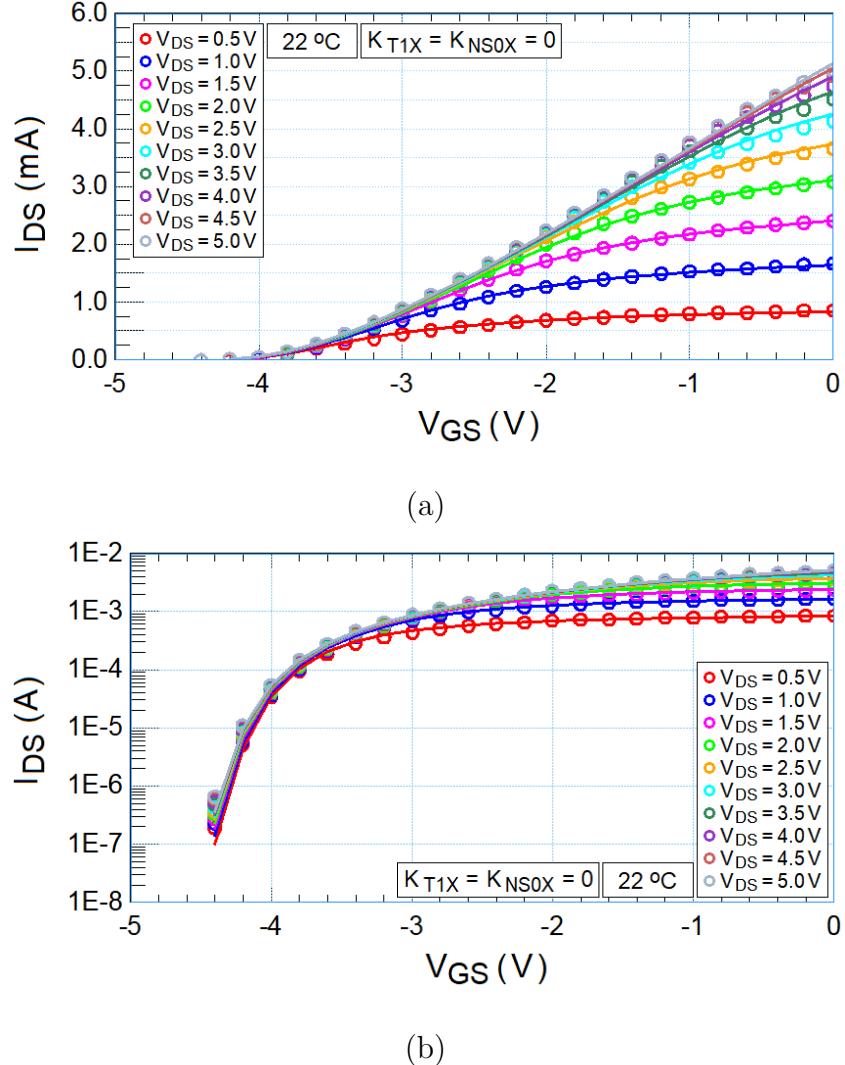


Figure 8.8: Measured (symbol) and simulated (line) I_{DS} - V_{GS} characteristics in (a) linear scale (b) semi-logarithmic scale, at ambient temperature $T = 22^\circ\text{C}$, with V_{DS} varying from 0.5 V to 5 V, where the model is for when $K_{T1X} = K_{NS0X} = 0$.

where THESAT, which equals $\frac{1}{V_{D_{sat}}} = \frac{\beta_\perp U_{0t}}{V_{SAT_t} L}$, has been set as a temperature independent model parameter. As can be noted, this approximation amounts to neglecting the temperature dependence of THESAT. To accurately model extreme-temperature conditions, we implemented (8.11) in the enhanced version of the ASM-GaN model, which we are presenting in this work.

In order to investigate the behavior of the device under test with temperature, we set

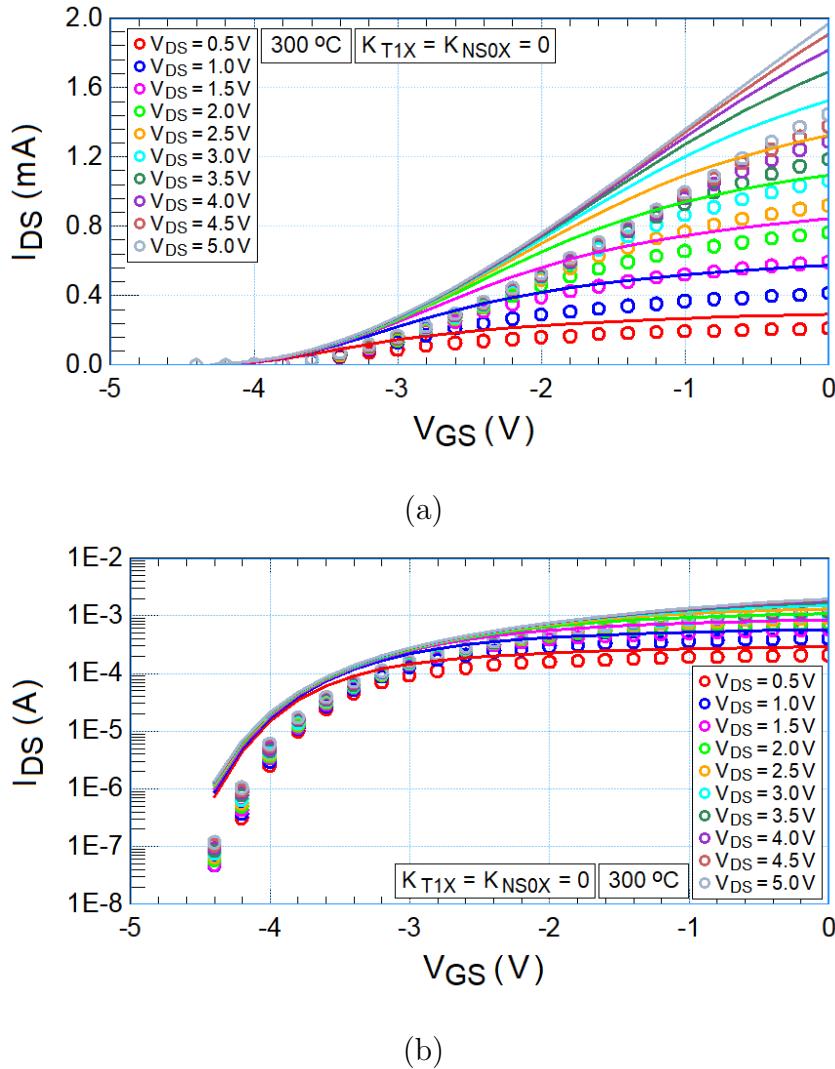


Figure 8.9: Measured (symbol) and simulated (line) I_{DS} - V_{GS} characteristics in (a) linear scale (b) semi-logarithmic scale, at ambient temperature $T = 300 \text{ }^{\circ}\text{C}$, with V_{DS} varying from 0.5 V to 5 V, where the model is for when $K_{T1X} = K_{NS0X} = 0$.

the temperature parameters K_{T1} , UTE, AT and K_{NS0} to zero, and the parameters RC and K_{RC} to their measured values of $0.68 \Omega\text{-mm}$ and 0.45, and extracted the parameters of the model at each temperature, using the same values for all the model parameters, except for the four parameters: VOFF, U0, VSAT and NS0ACC. To avoid the influence of self-heating, we extracted these parameters at relatively low values of V_{DS} , in particular, at $V_{DS} = 0.5 \text{ V}$ to 5 V . The variations of these parameters are shown in Fig. 8.7.

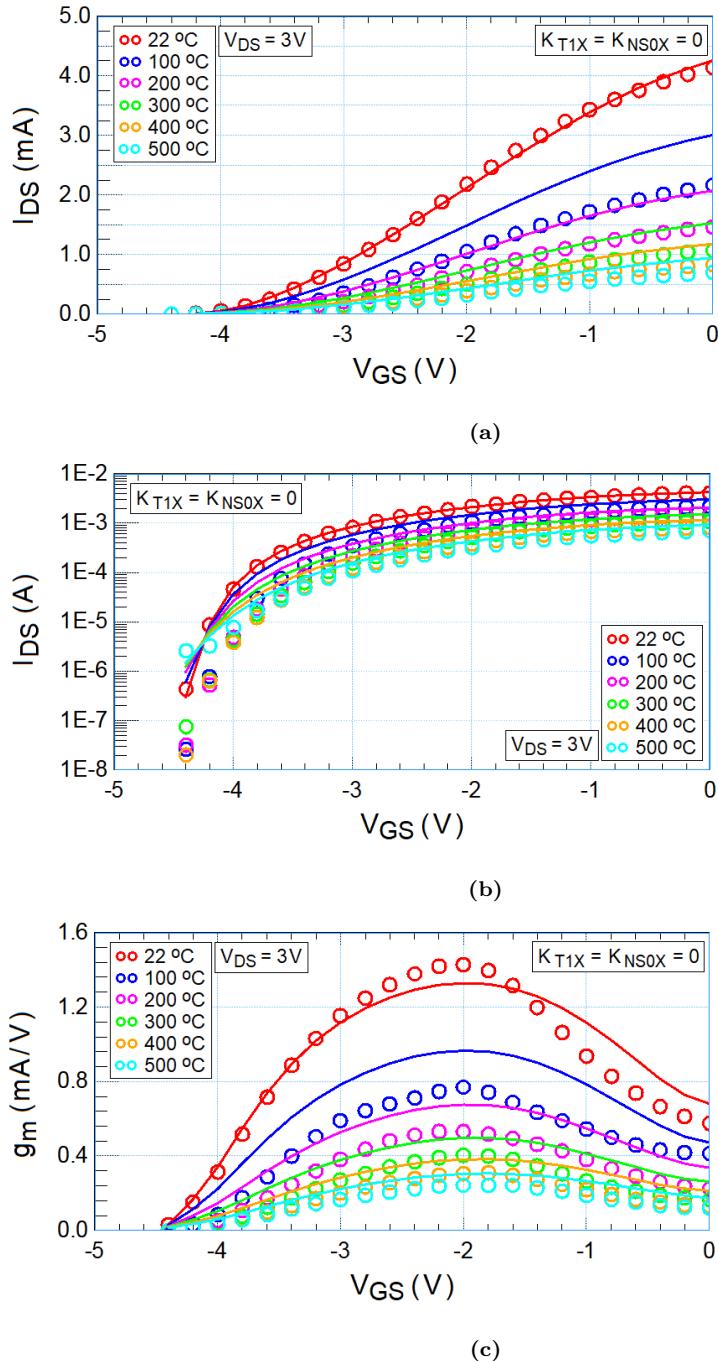


Figure 8.10: Measured (symbol) and simulated (line) (a) I_{DS} - V_{GS} characteristics in linear scale (b) I_{DS} - V_{GS} characteristics in semi-logarithmic scale (c) g_m - V_{GS} characteristics at $V_{DS} = 3$ V, for temperatures ranging from 22 °C to 500 °C, where the model is for when $K_{T1X} = K_{NSOX} = 0$.

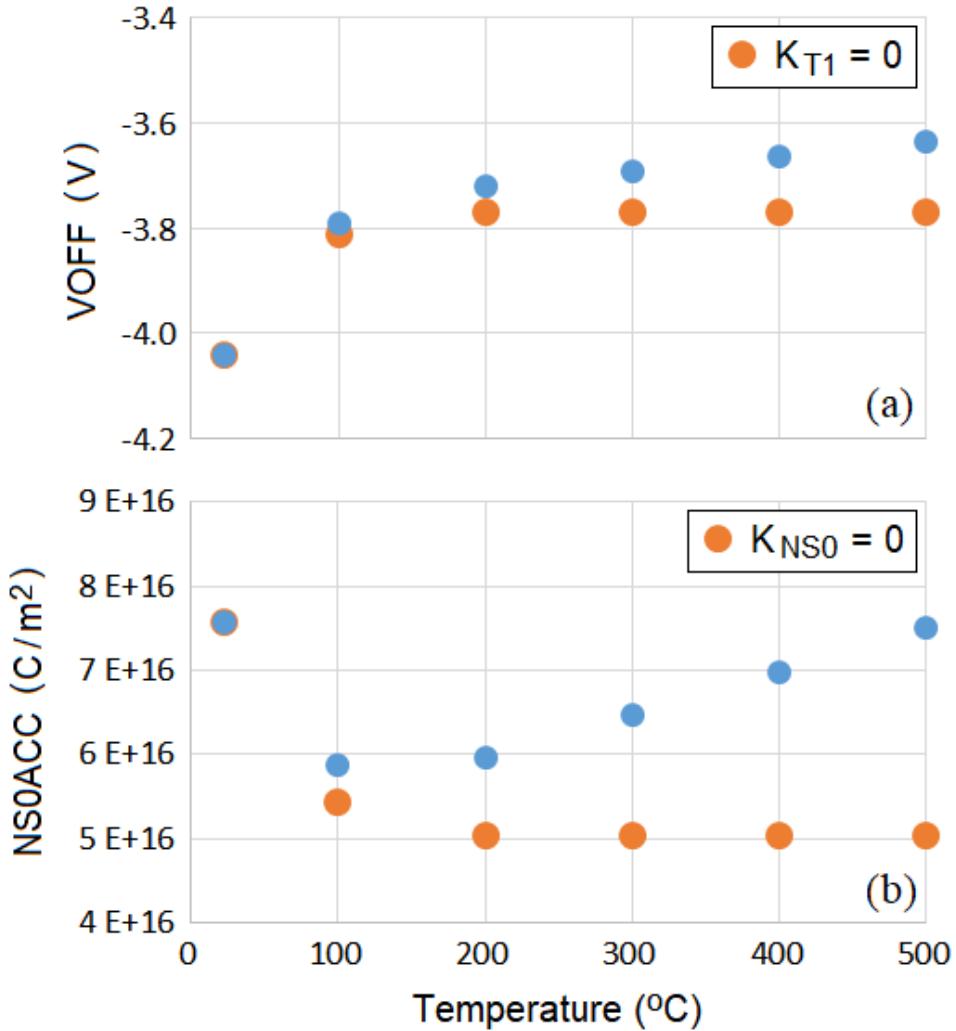


Figure 8.11: The variations of the parameter (a) V_{OFF} (b) $NS0ACC$ of the model with temperature, setting the temperature parameter (a) K_{T1} & (b) K_{NS0} to zero. The variations of V_{OFF} and $NS0ACC$ in orange, thus show the temperature dependence on trapping only i.e. the values in orange are variations in intermediate model parameters - V_{OFF}_x and $NS0ACC_x$. The actual extracted variations of V_{OFF} and $NS0ACC$ are shown in blue. This shows that the temperature variation given by trapping is a dominant factor in determining the characteristics of AlGaN/GaN HEMTs.

Equations (8.2) and (8.3) fit well to the variations of the extracted values of U_0 and VSAT respectively, with $UTE = -1.975$ and $AT = 0$. It remains, therefore, to modify the temperature-scaling equations of V_{OFF} and $NS0ACC$.

The non-linear variations of VOFF and NS0ACC with temperature, which for NS0ACC is non-monotonic, can be modeled by considering the presence of an acceptor type trap center in the channel and access regions of the active GaN layer of the device under test, which is subject to injection of electrons, resulting in ionization of this trap center, and hence variation in the 2-DEG density in the channels of the intrinsic (affecting VOFF) and the access regions (affecting NS0ACC) of the device under test.

Following the approach we presented in previous chapter (chapt.7) for modeling of the trapping effect, the steady-state potential \bar{v}_x introduced by traps acting as an electron-trapping center is given by (7.21):

$$\bar{v}_x = V_x / [1 + \exp(-\phi_n)] , \quad (8.15)$$

where V_x is the trap potential when the traps are fully ionized and ϕ_n which is given by (7.8) reduces to following with the assumption that $n_o \ll \hat{n}$

$$\phi_n = \ln (\alpha |I_{Inj}|) , \quad (8.16)$$

where α is a constant and I_{Inj} is the electron current injected toward the trap center. We have found that an excellent fit to the measurement results can be obtained with an injection current of the following form:

$$I_{inj} = \alpha T_{dev}^2 \exp(-q\phi/V_{th}) , \quad (8.17)$$

where $V_{th} = K_B T_{dev}$, is the thermal voltage, where K_B is the Boltzmann's constant and T_{dev} is the device temperature, and α and the potential barrier ϕ are model parameters. It is worth noting that thermionic-emission current, which is given by the equation below [151], reduces to the above equation under the bias conditions at which the device under test was measured:

$$I_{TE} = NFW L J_{TE0} \left[\exp(V/(\eta V_{th})) - 1 \right] , \quad (8.18)$$

Table 8.3: Trapping-related parameters

Model Parameter	Description	Value
ϕ	Potential barrier (eV)	0.99
α	Proportionality constant in the equation of injection current (A/K^2)	862.6×10^6
K_{T1X}	Constant relating trap potential to VOFF	-66.9×10^{-3}
K_{NS0X}	Constant relating trap potential to NS0ACC	-334.8×10^{-3}

where NF is the number of fingers, η is the ideality factor, V is the applied voltage across the Schottky barrier, which can be set equal to the average of the intrinsic gate-to-source voltage, $V_{G_iS_i}$, and gate-to-drain voltage, $V_{G_iD_i}$, and J_{TE0} is the reverse saturation current density, and is given by

$$J_{TE0} = A^* T_{dev}^2 \exp(-q\phi_{TE}/V_{th}), \quad (8.19)$$

where A^* is the effective Richardson's constant and ϕ_{TE} is the Schottky barrier height. In particular, for $V_{G_iS_i}, V_{G_iD_i} < 0$,

$$|I_{TE}| \approx NFWL J_{TE0}. \quad (8.20)$$

We then let the trap potential modify the parameters VOFF and NS0ACC of the ASM-GaN model in a linear manner as

$$VOFF_x = VOFF(1 + K_{T1X} \bar{v}_x), \quad (8.21)$$

$$NS0ACC_x = NS0ACC(1 + K_{NS0X} \bar{v}_x), \quad (8.22)$$

where $\bar{v} = \bar{v}/V_x$ is the normalized steady-state trap potential to the potential V_x , and K_{T1X} and K_{NS0X} are model parameters, implying that first-order corrections to VOFF and NS0ACC are sufficient to capture the effect of trapping. The non-linear variations of

VOFF and NS0ACC with temperature, which for NS0ACC is non-monotonic, are then modeled by modifying (8.1) and (8.4) as

$$\text{VOFF}_t = \text{VOFF}_x \left(1 - K_{T1} \Delta \bar{T} \right), \quad (8.23)$$

$$\text{NS0ACC}_t = \text{NS0ACC}_x \left(1 + K_{NS0} \Delta \bar{T} \right). \quad (8.24)$$

8.2.2 Results And Discussion On Extreme Temperature Model

The results of the fit of the ASM-GaN compact model with the modified temperature-scaling equations to the measurement results are shown in Figs 8.1-8.5. The different model parameters associated with this model are tabulated in Tables 8.1, 8.2 and 8.3.

In order to show the effect of the temperature dependence of trapping, we simulated the transfer characteristics (plotted vs data) of the model at $T = 22$ °C and 300 °C, at drain-to-source voltages ranging from $V_{DS} = 0.5$ V to 5 V, with the trapping parameters K_{T1X} and K_{NS0X} set to zero. The results are shown in Figs 8.8 and 8.9. Note from Fig. 8.8 that at $T = 22$ °C, at which thermionic-emission current, which possibly is the injection current leading to charge trapping in the device under test, is very low, a good fit of the model to the measurement results is still obtained after setting K_{T1X} and K_{NS0X} to zero. Furthermore, we simulated the model at $V_{DS} = 3$ V, at ambient temperatures ranging from $T = 22$ °C to 500 °C, with the trapping parameters K_{T1X} and K_{NS0X} set to zero. The results are shown in Figs 8.10.

In order to show the variations of VOFF_x and NS0ACC_x , given by (8.21) and (8.22), with temperature, we simulated the model with the temperature parameters K_{T1} and K_{NS0} set to zero. The results are shown in Fig. 8.11 from which it can be inferred that the temperature variation given by trapping is a dominant factor in determining the characteristics of AlGaN/GaN HEMT's.

The non-linear behaviour depicted in Figs 8.7(a) and 8.7(d) (and also in Fig. 8.11),

which in Fig. 8.7(d) is non-monotonic, is modeled with the application of the trapping model presented in the previous chapter, assuming the presence of a trap center with a given energy level. While we can model the data quite well with that model, it is to be noted that the trapping model used here does not account for the trapping time constant, which requires performing measurements such as pulsed measurements, nor it accounts for multiple traps and their time constants. Nevertheless, we were able to model the DC behavior of the device under test over a wide range of temperatures with this simple trapping model. For the purposes of the studies performed on the device under test, (8.23) and (8.24) may also be viewed as empirical extensions of the temperature equations used in the current version of the ASM-GaN model for the two model parameters - VOFF and NS0ACC.

8.3 Modeling Of AlGaN/GaN HEMTs Subjected To Proton Radiation

AlGaN/GaN HEMTs used in [142] were fabricated on AlGaN/GaN hetero-structures grown by molecular beam epitaxy (MBE) on 4H-SiC substrates. The MBE growth of the AlGaN/GaN hetero-structures was performed under Ga-rich and NH₃-rich conditions, thus forming two different sets of devices. Both of the devices were irradiated under similar conditions with 1.8-MeV protons to a maximum proton fluence of $10^{14} \frac{1}{\text{cm}^2}$. The model (ASM-GaN) vs data fits for transfer & trans-conductance (g_m) characteristics of both Ga-rich and NH₃-rich devices, measured for fresh (pre-irradiation) condition and post-irradiation with different proton dose levels are shown in Fig. 8.12 and Fig. 8.13. The excellent fit shown in these figures was obtained by first extracting the model parameters for the fresh devices, and then changing three parameters of the model: VOFF, NS0ACCS and NS0ACCD (both kept equal and hence represented as NS0ACC) to mimic the impact

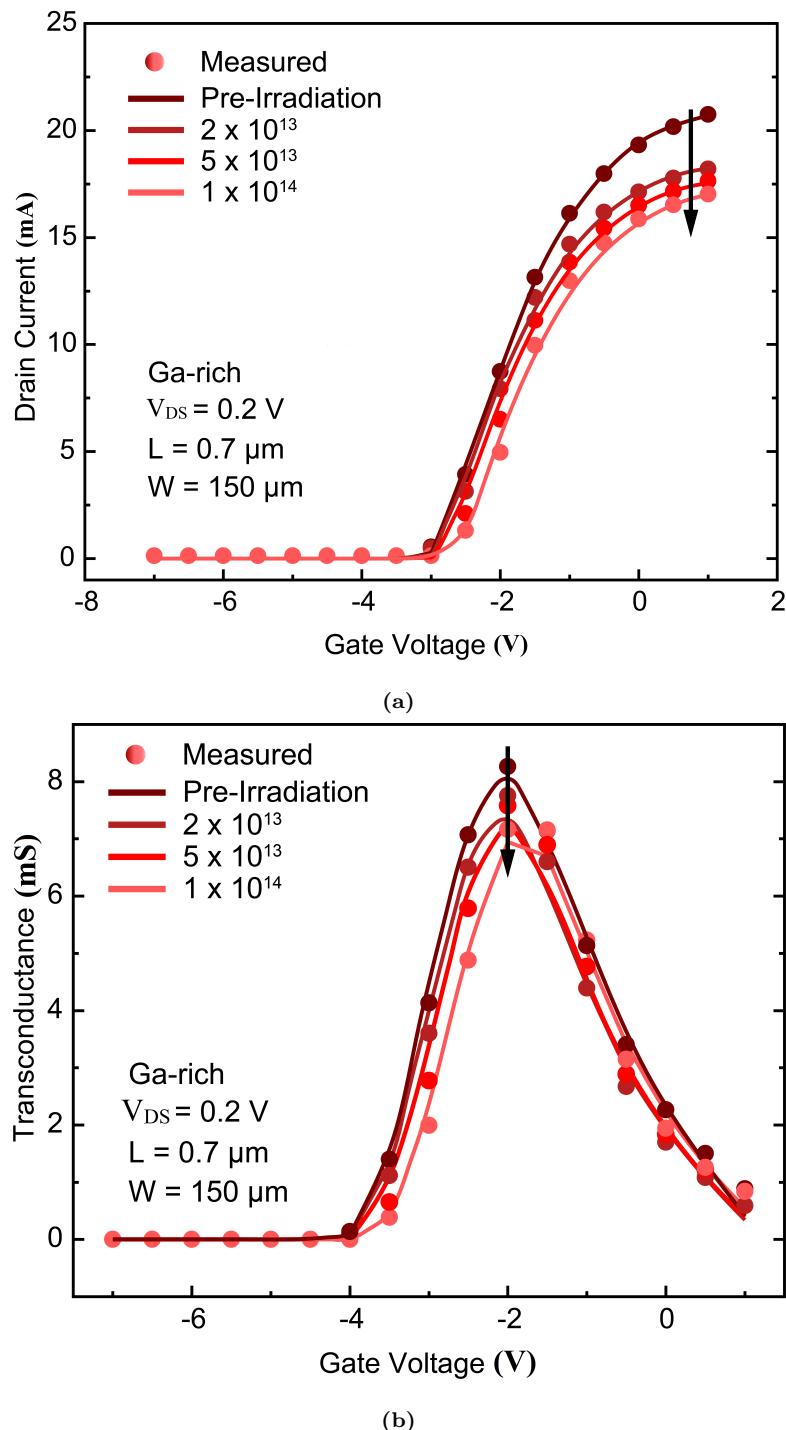


Figure 8.12: The measured and modeled (a) transfer characteristics & (b) trans-conductance plot for Ga-rich AlGaN/GaN HEMT with increasing proton radiation dose levels.

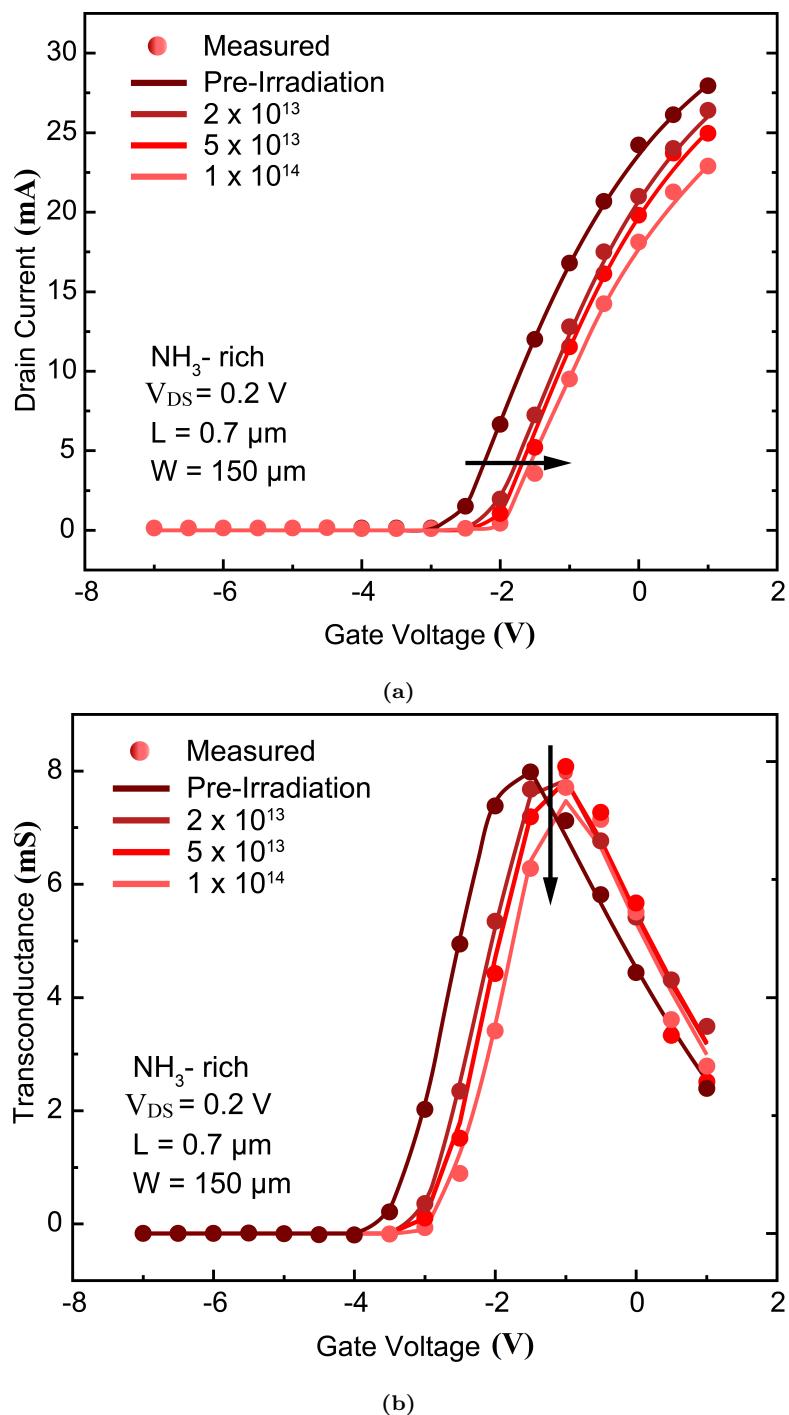


Figure 8.13: The measured and modeled (a) transfer characteristics & (b) trans-conductance plot for NH₃-rich AlGaN/GaN HEMT with increasing proton radiation dose levels.

Table 8.4: Extracted model parameters for Ga-rich device

Proton Radiation Dose (1/cm²)	VOFF (V)	NS0ACC (1/m³)
0	-3.02	5×10^{17}
2×10^{13}	-2.99	1.9×10^{17}
5×10^{13}	-2.9	1.6×10^{17}
1×10^{14}	-2.7	1.43×10^{17}

of radiation in terms of increase in cut-off voltage and decrease in drain and source access region 2DEG charge densities of a HEMT. The corresponding model parameters extracted for Ga-rich device are shown in Table. 8.4 and for NH₃-rich device in Table. 8.5.

Table 8.5: Extracted model parameters for NH₃-rich device

Proton Radiation Dose (1/cm²)	VOFF (V)	NS0ACC (1/m³)
0	-2.7	5×10^{17}
2×10^{13}	-2.25	4.5×10^{17}
5×10^{13}	-2.15	3.8×10^{17}
1×10^{14}	-2.0	2.5×10^{17}

At this juncture, we have an interesting observation - for extreme temperature modeling of HEMTs, we had to scale the model parameters VOFF and NS0ACC after adding the effect of trapping of Schottky gate reverse bias thermionic emission current into the acceptor type traps present in the active GaN layer, while in the case of modeling the degradation in device performance due to proton irradiation of HEMTs, we had to vary the same model parameters, which implies that these variations are indeed due to the cre-

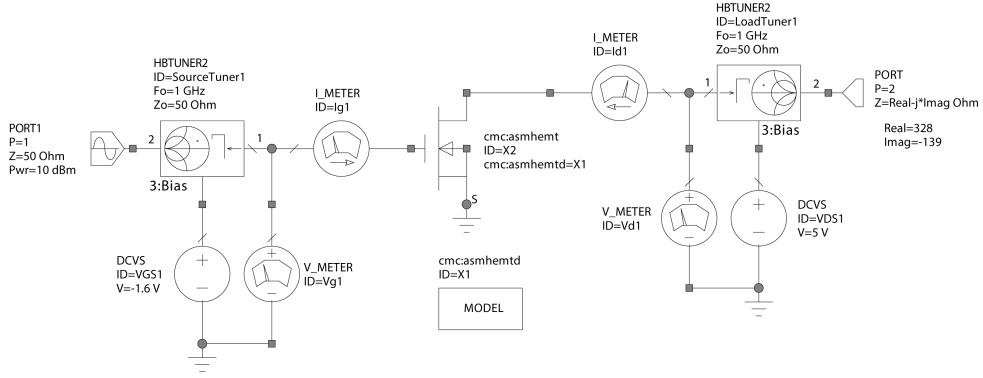


Figure 8.14: Circuit simulation setup in AWR for simulating the large-signal, single tone PA characteristics using harmonic balance (hb) simulation.

ation of acceptor type traps as observed in [142]. A detailed physical explanation of how these acceptor type trap centres form after exposure to proton radiation could be a topic of further research. A preliminary guess could be that the proton recombines with the 2DEG electrons to create hydrogen interstitials in the GaN lattice, which further act as trap centres. The creation of these traps is accompanied by a corresponding reduction in the overall 2DEG charge in both the channel and access regions, which in turn reflects in the direction of variation of model parameters VOFF (increase) and NS0ACC (decrease).

Fig. 8.14 shows the setup and Fig. 8.15 shows the large-signal single tone RF simulations (hb) of a PA with output power (P_{out}), Gain and Power Added Efficiency (PAE) as functions of available input power (P_{in}) for $V_{DD} = 5$ V with two gate bias conditions, one for Ga-rich and another for NH_3 -rich device; with bias current values of $I_{DS} = 22.4$ mA/mm and $I_{DS} = 28.6$ mA/mm respectively. The frequency of the 10 dBm RF input signal was set to 1 GHz and the value of the load impedance was set for maximum PAE. It can be inferred from these large-signal simulations that the fresh NH_3 -rich device shows slightly higher Gain, P_{out} and PAE as compared to the fresh Ga-rich device. However, it shows higher degradation in the chosen model parameters with respect to increasing irradiation dose as shown in Table. 8.5. Hence when compared with NH_3 -rich devices,

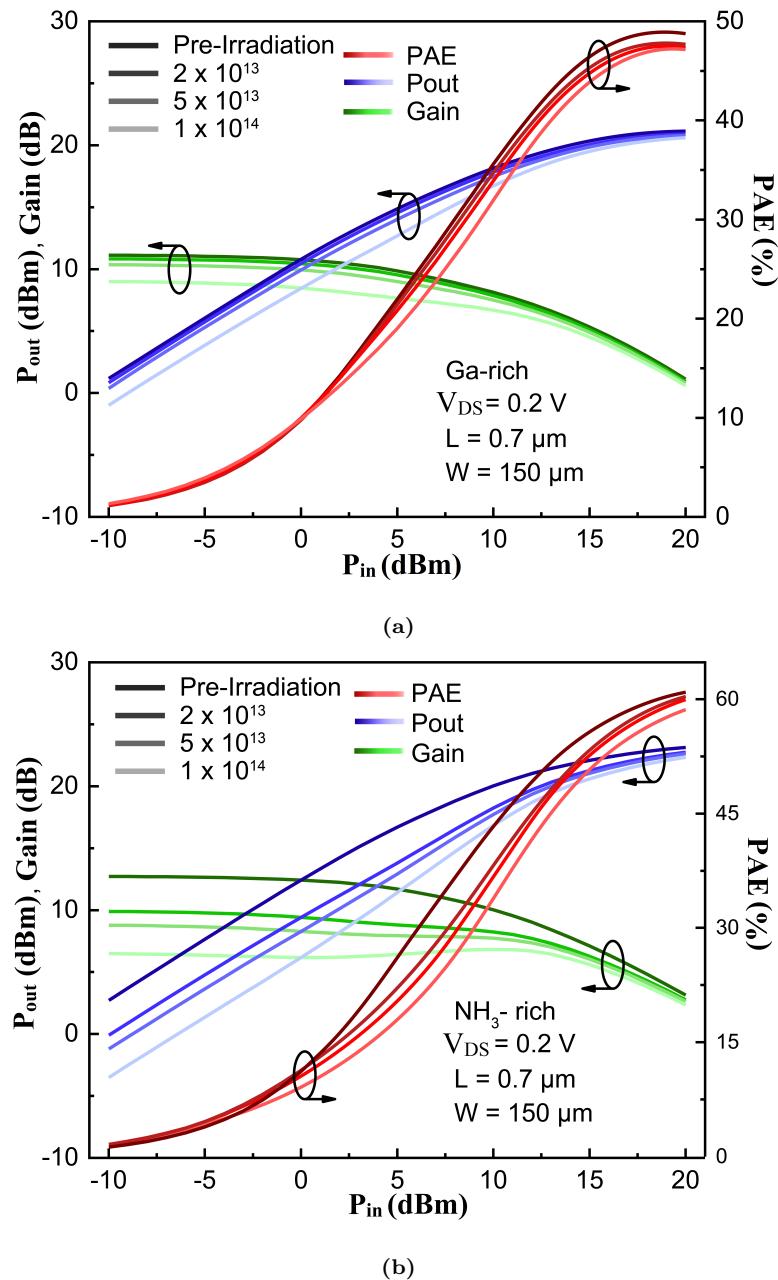


Figure 8.15: The output of large-signal RF (hb) simulations containing output power (P_{out}), Gain and Power Added Efficiency (PAE) as functions of available input power (P_{in}) with $V_{DS} = 5$ V for (a) Ga-rich and (b) NH₃-rich GaN devices, with $I_{DS} = 22.4$ mA/mm and $I_{DS} = 28.6$ mA/mm, respectively.

Ga-rich devices offer more resilience to the proton radiation environment at the cost of slightly reduced performance.

8.4 Conclusion

In this chapter, we modeled two extreme scenarios that can arise during the operation of a depletion type (d-type) AlGaN/GaN HEMT. The overall work is summed up below:

1. Extreme temperature modeling of the measured DC transfer and output characteristics of an AlGaN/GaN HEMT was performed by enhancing the temperature-modeling aspect of the industry-standard ASM-GaN compact model. This was achieved by considering the temperature dependence of the trapping behavior of the device under test, as well as not using an approximation, which is due to the effect of lateral electric field in the calculation of effective mobility (μ_{eff}) via an intermediate model parameter V_{Dsat} in the current version of ASM-GaN model. Thus, the variance of this intermediate model parameter V_{Dsat} w.r.t temperature, which was neglected in the current version of ASM-GaN, was included in order to improve the temperature modeling in ASM-GaN. A detailed description of the modeling approach, and the excellent fits of the simulation results of the enhanced ASM-GaN model to the measurement results were presented. This new model, which is capable of modeling devices for a wide temperature range, from 22 °C to 500 °C, can thus be effectively used in designing circuits and systems targeted at applications ranging from space to automobiles.
2. A robust industry standard compact model (ASM-GaN) was used for modeling and predicting the RF performance of AlGaN/GaN HEMT designed for extreme radiation environment conditions, such as low earth orbit satellites, where the HEMT can potentially be subjected to varying doses of proton radiation. Two different types of GaN devices exposed to different levels of proton radiation dose were modeled with the ASM-GaN model, and the degradation in the large signal RF performance of a power amplifier (PA) designed using the models extracted for the two types of

devices was predicted.

A common thread between the above two different models is that both involve variation in a common set of model parameters, viz. threshold voltage and access region 2DEG carrier densities. Thus, a variation in these model parameters implies presence or signature of trapping phenomenon. The cause of these variations can be traced back to the charging of traps due to reverse biased Schottky diode's thermionic emission gate current in case of extreme temperature modeling and creation of acceptor type trap centres in case of extreme radiation environment modeling.

9

Modeling Of Charge In AlGaN/GaN HEMTs With p-GaN Layer

“Innovation is not the product of logical thought, even though the final product is tied to a logical structure.”

– Albert Einstein

9.1 Introduction

AlGaN/GaN High Electron Mobility Transistors (HEMTs) are emerging as a promising choice for power conversion and high-speed applications because of their high electron mobility and high breakdown electric field [152] [65]. Due to the two-dimensional electron gas (2DEG) formed at zero gate bias, these devices are inherently depletion mode (d-mode). However, when power devices are used as switches, enhancement mode (e-mode) devices are preferred because of simple gate control design and a fail-safe operation [153]. Several architectures to achieve this e-mode operation have been successfully demonstrated in [154–156] using a p-GaN layer, which is a Mg doped GaN layer, grown on the top of

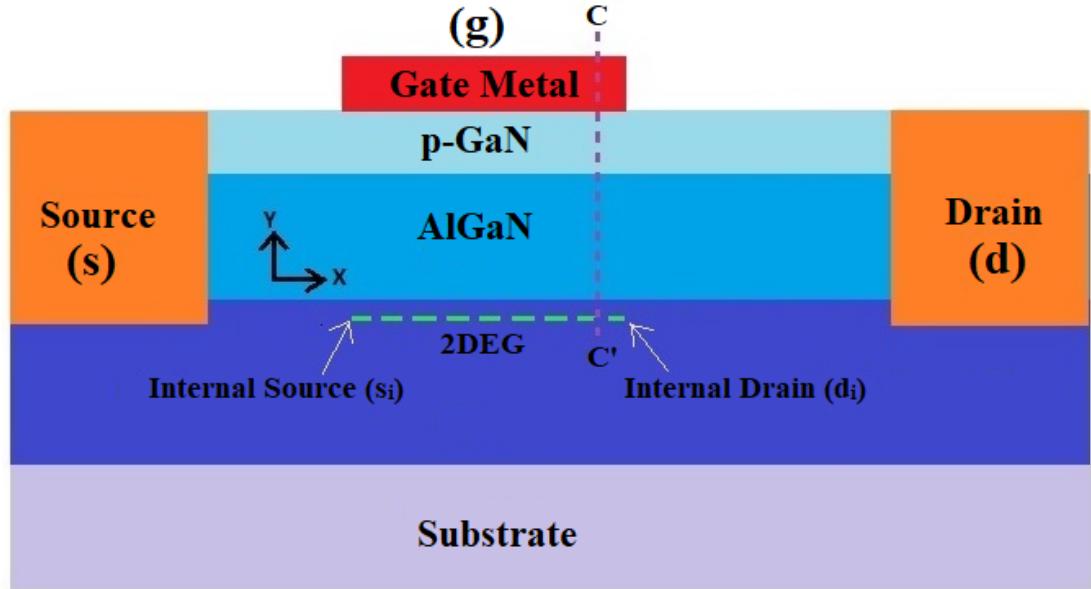


Figure 9.1: Cross section of a typical p-GaN HEMT(not to scale, just for illustration purpose).

AlGaN layer. A Schottky contact is established with top metal layer to form the gate contact. The gate capacitance of such a device is found to decrease at high gate voltages because of the junction capacitance of Schottky metal/p-GaN junction being in series with the AlGaN layer capacitance. This effect has yet not been taken into consideration in compact models nor has its impact on important power device metrics such as ON resistance and gate charge been studied. In this chapter, we have derived a new analytical model by using an effective gate voltage obtained from the underlying device electrostatics, under simplified assumptions. Furthermore, we implemented it in the physics-based compact model for GaN devices: ASM-GaN [43,44,53,56,58,66,146–148,157–159], whose development and extension to power semiconductor HEMTs is the main theme of this thesis.

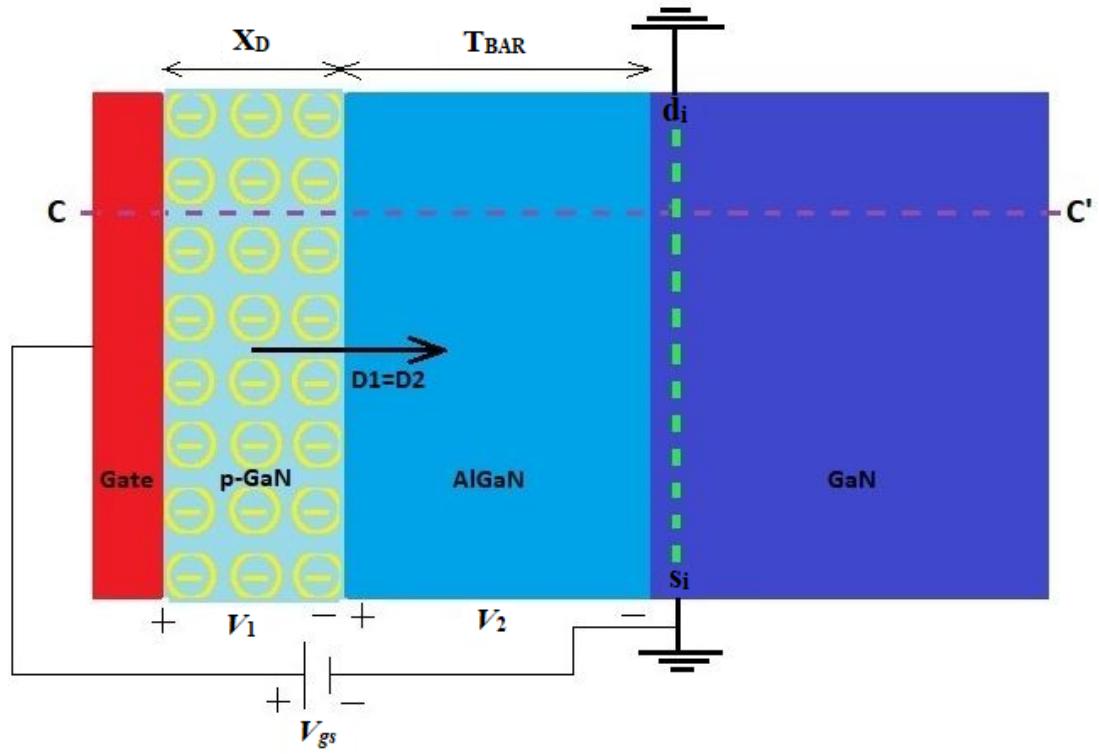


Figure 9.2: A detailed setup along section CC' for deriving $V_{g\text{eff}}$ showing the voltage drop across various layers such as p-GaN (V_1) and AlGaN (V_2).

9.2 Model Description

A typical cross section of p-GaN HEMT is shown in Fig. 9.1. An external gate voltage is applied between the gate and grounded source of the device as shown in Fig. 9.2. Note that in this chapter, there is an implicit assumption that source is always grounded and hence any other voltage such as gate voltage (V_g) or drain voltage (V_d) are voltages referenced to grounded source. Let V_1 and V_2 be the voltage drops across the p-GaN and AlGaN layers respectively, while X_D and T_{BAR} are widths of p-GaN and AlGaN layers respectively.

Let $V_{g\text{eff}}$ be the effective gate voltage seen across gate to source which considers the voltage drop across the fully depleted p-GaN layer i.e. $V_{g\text{eff}} = V_{gs} - V_1$. Considering the voltage rise due to applied gate voltage and voltage drops across each layer of section

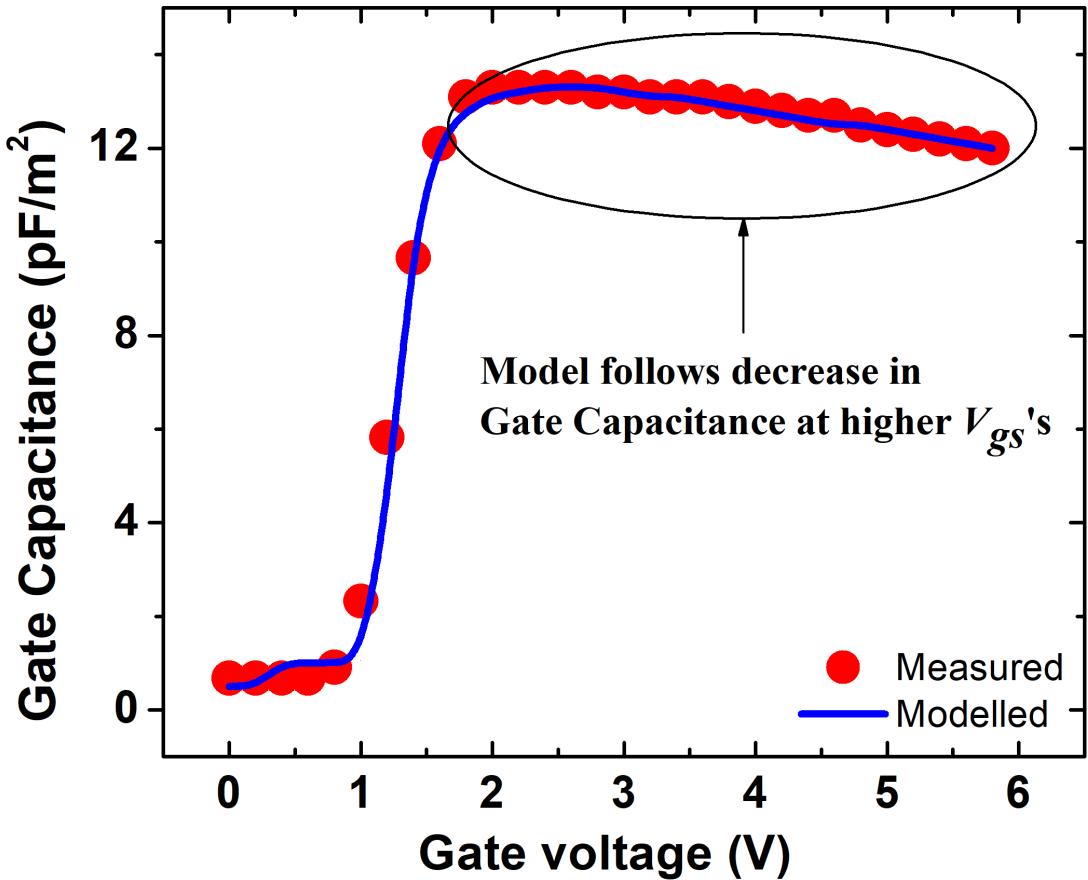


Figure 9.3: C-V fit for Sample A with p-GaN depletion model showing decrease in capacitance at high gate voltage.

CC' we get following expression for the potential balance[52]

$$V_{gs} - V_1 - V_2 - E_f = 0 \quad (9.1)$$

where Fermi level E_f is the potential drop across the 2DEG for zero drain and source bias as shown in Fig. 9.2. The magnitude of displacement electric field in p-GaN layer is D_1 , while in AlGaN layer it is D_2 . If there are no surface traps or charges present in between p-GaN/AlGaN interface, we can apply the boundary condition $D_1=D_2$. Thus, we can write

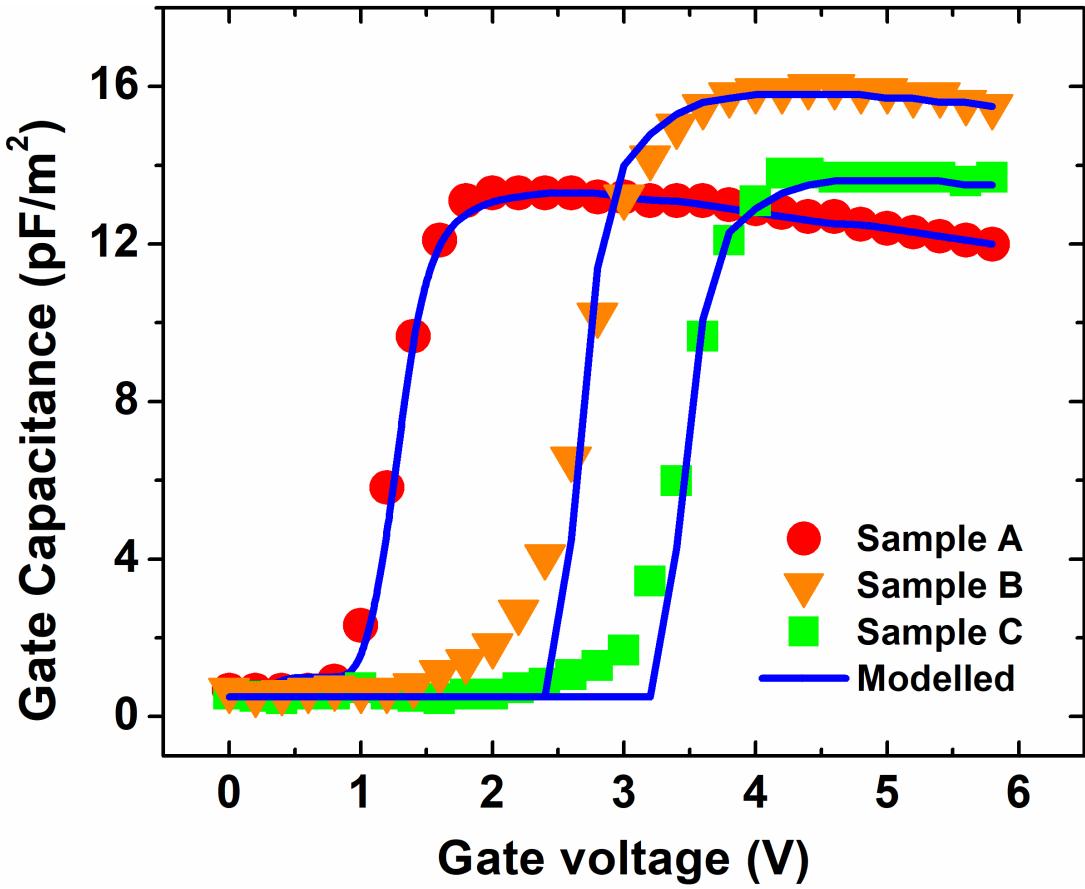


Figure 9.4: C-V fits for all the samples demonstrating effect of p-type doping in p-GaN layer on the behavior of gate capacitance.

$$\varepsilon_1 E_1 = \varepsilon_2 E_2 \quad (9.2)$$

where ε_1 and ε_2 are the permittivities and electric field magnitudes in p-GaN and AlGaN layers respectively. The potential drop in fully depleted p-GaN region with doping N_A can be calculated as

$$V_1 = \frac{1}{2} X_D E_1 = \frac{q N_A X_D^2}{2 \varepsilon_1} \quad (9.3)$$

Substituting (9.3) in (9.2) and then rearranging (9.1), we get

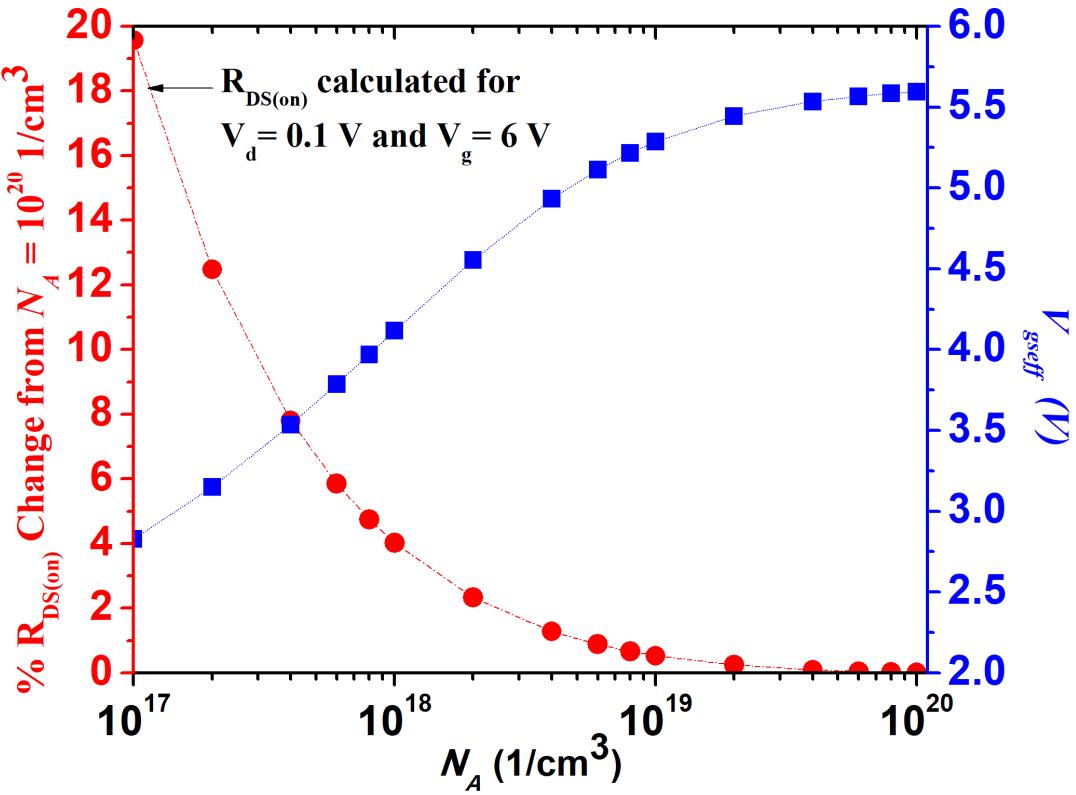


Figure 9.5: Variation of ON resistance and effective gate voltage with p-GaN doping parameter N_A for a device of $W = 5.5 \text{ mm}$ and $L = 1 \mu\text{m}$.

$$V_{gs} - V_1 - E_f = \frac{\sqrt{2q\varepsilon_1 N_A V_1}}{\frac{\varepsilon_2}{T_{BAR}}} \quad (9.4)$$

Solving Eq. 9.4 by squaring both the sides and re-substituting $V_{gs} - V_1 = V_{gseff}$, we get

$$V_{gseff} = E_f + \frac{1}{2k} \left[\sqrt{1 + 4k(V_{gs} - E_f)} - 1 \right] \quad (9.5)$$

where,

$$k = \frac{\varepsilon_2^2}{2q\varepsilon_1 N_A T_{BAR}^2} \quad (9.6)$$

This effective gate voltage V_{gseff} is responsible for modulating the 2DEG charge, which in turn changes both the capacitance and the current of the device, thus affecting its

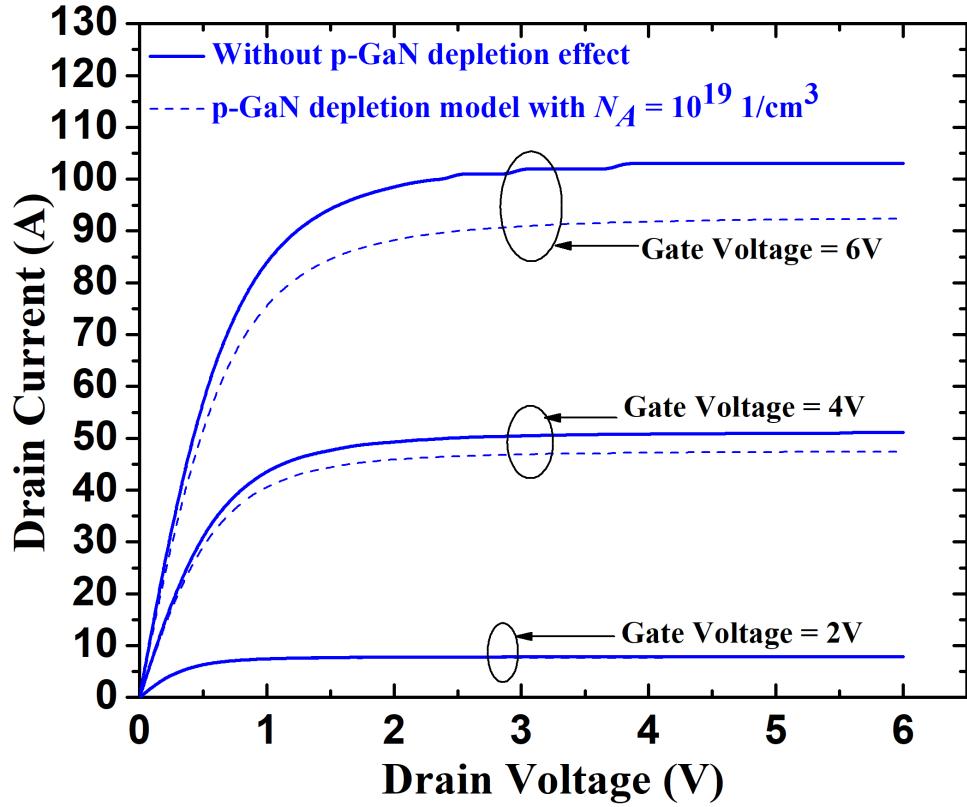


Figure 9.6: Output characteristics of Sample A with and without p-GaN depletion model for different gate voltages for a device of $W = 5.5 \text{ mm}$ and $L = 1 \mu\text{m}$.

switching performance. We implemented this depletion approximation-based equation for V_{gseff} in conjunction with ASM-GaN compact model [43,44,53,56,58,66,146–148,157–159] as core and used this new model to fit the experimental data from [153]. Furthermore, this newly developed model was used to study the impact of p-type doping on the ON resistance $R_{DS(on)}$ and gate charge Q_g of the device because their product is one of the key figure of merit for switching power semiconductor devices.

9.3 Results And Discussions

In Figs. 9.3 and 9.4, we model the C-V data for three different devices A, B and C (from [153]) which have a geometry of $W = 75 \mu\text{m}$ and $L = 75 \mu\text{m}$ with varying amount of

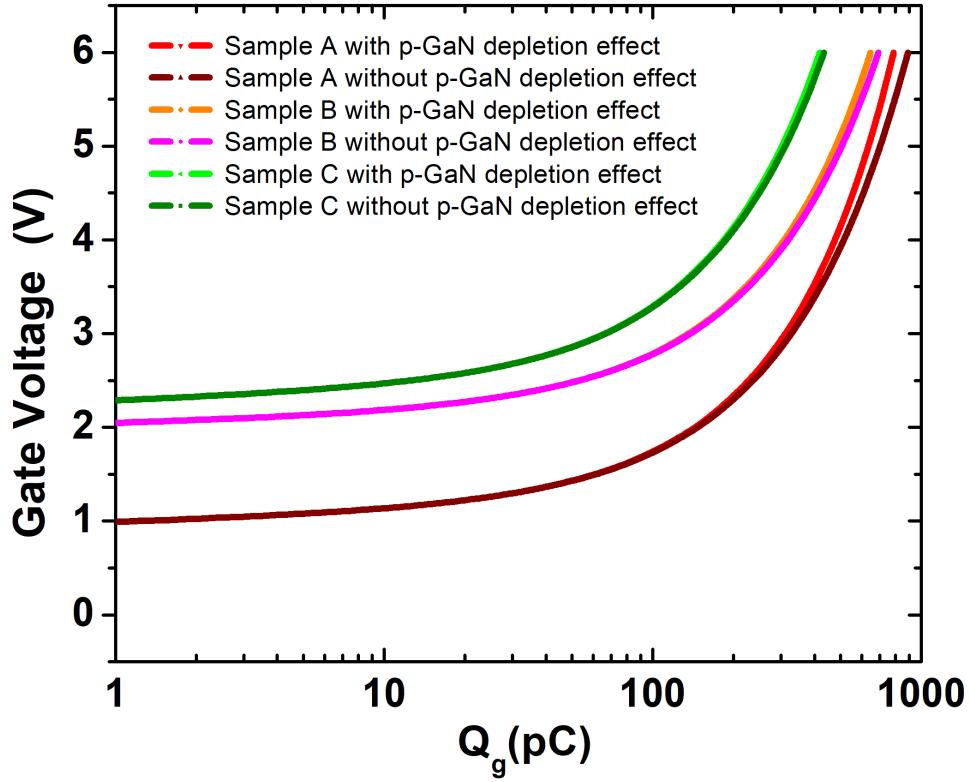


Figure 9.7: Gate Charge simulation for all the samples from static I-V characteristics for a device of $W = 5.5$ mm and $L = 1 \mu\text{m}$.

p-GaN layer doping. An excellent agreement with experimental data can be seen from Fig. 9.4 for all the devices. The reduction of capacitance in Fig. 9.3 is because V_{gseff} calculated by (9.5) reduces as p-GaN doping N_A reduces, which in turn reduces the internal gate charge Q_g . Please note that for sample A, doping N_A is $7 * 10^{18} \frac{1}{\text{cm}^3}$, which is minimum of the three devices. Any capacitance between terminals a and b is determined in the model as (see (2.27))

$$C_{ab} = \gamma \frac{\partial Q_a}{\partial V_b}. \quad (9.7)$$

Hence the gate-source and gate-drain terminal small-signal capacitances C_{gs} and C_{gd} , as calculated from (9.7), and which play a major role in determining the switching characteristics, are already predicted in the model. The addition of these two capacitances gives

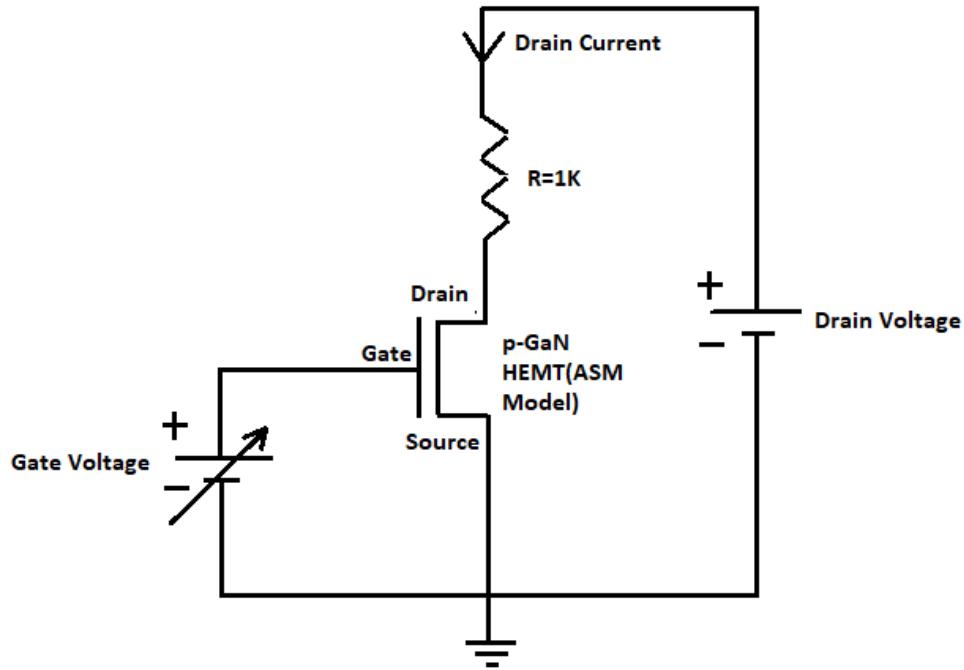


Figure 9.8: Circuit schematic for simulating Gate Charge in Fig.7.

the total gate capacitance (i.e. Gate Capacitance = $C_{gg} = C_{gs} + C_{gd}$).

In order to characterize the performance of commercial p-GaN e-mode HEMTs, we changed the geometry of above experimentally calibrated models from $W = 75 \mu\text{m}$ and $L = 75 \mu\text{m}$ to $W = 5.5 \text{ mm}$ and $L = 1 \mu\text{m}$, and simulated ON resistance $R_{DS(\text{on})}$, output and gate-charge Q_g characteristics as a function of doping in p-GaN layer. A decrease in p-GaN doping causes an increase in $R_{DS(\text{on})}$ as shown in Fig. 9.5. Furthermore, it shows the variation of effective gate-source voltage (V_{gseff}) which is responsible for modulating 2-DEG charge in the channel. As doping in p-GaN layer decreases a large voltage is dropped in this layer and V_{gseff} reduces, indicating smaller 2-DEG charge and hence larger $R_{DS(\text{on})}$.

Fig. 9.6 shows simulated output characteristics of the sample A with and without using p-GaN depletion model. The voltage drop in p-GaN layer with the p-GaN depletion model is a function of p-GaN layer doping N_A . This voltage drop in p-GaN layer reduces the 2-DEG charge, thereby decreasing the drain current in Fig. 9.6. In Fig. 9.7 we analyzed

the amount of gate charge required to get 6 V (which is the maximum voltage for given samples) at the gate terminal by using a resistive load at drain connected to a DC supply of 6 V and with a gate voltage sweep from 0 to 6 V. The impact of doping on the gate charge is found to be opposite to that of ON resistance. Indeed, reduction in capacitance seen in Fig. 9.3 and the developed model shows that as p-GaN doping is reduced the amount of gate charge required to reach certain gate voltage reduces. These simulations indicate a very interesting point that a careful optimization of doping in p-GaN layer can be used to improve the $Q_g * R_{DS(on)}$ performance metric of a p-GaN power HEMT.

9.4 Conclusion

We studied the effect of doping of p-GaN layer on the performance parameters, such as $R_{DS(on)}$ and Q_g of enhancement mode power GaN devices. We found that there exists a trade-off between $R_{DS(on)}$ and Q_g depending on the doping level of p-GaN layer. Higher doping, which gives lower $R_{DS(on)}$, could be preferred for an application in which switching losses are critical. On the other hand, lower doping of p-GaN results in lower Q_g , which implies that the device reaches a certain gate voltage faster with lower doping. We present a simple analytical simulation model of the effect of p-GaN layer doping. The model shows excellent agreement with the experimental data. The developed model can be used to simulate a given power switching circuit and predict and optimize its performance w.r.t p-GaN layer doping.

10

Conclusions And Future Work

“Only two kinds of people can attain self-knowledge: those who are not encumbered at all with learning, that is to say, whose minds are not over-crowded with thoughts borrowed from others; and those who, after studying all the scriptures and sciences, have come to realise that they know nothing.”

– Shri RamaKrishna

10.1 Conclusions

In the previous eight chapters, we have covered almost all the aspects of modeling power and low voltage III-V HEMTs with AlGaN/GaN HEMT as an example. Fig. 10.1 is an allegory of our journey so far with an elephant and six blind men from the famous poem of John Godfrey Saxe[160], representing DUT (Device Under Test, which is AlGaN/GaN HEMT in our case) and different kinds of measurements respectively. The choice of one experimental/measurement setup (represented by blind men) over another dictates the structure and functionality of the model derived from the measurement and restricts us from seeing the remaining aspects of the DUT, i.e. each blind man represents a unique



Figure 10.1: An allegory of our journey so far showing that there are multitude of ways of modeling a DUT (AlGaN/GaN HEMT) based on various kinds of experiments/measurements, with each model forming a part of the whole. This is a recurring theme in the current methodology of science and engineering - towards unification of all the different models of nature that the various constituent theories paint in order to gain a complete knowledge of nature.

boundary condition, which as discussed in chapt.1, is the starting point of any modeling exercise. Thus, one argument to make a “complete” model of a DUT will be to go on increasing the number of measurements, which is an impossible task with given time and resources. A more pragmatic approach would be to regard all the different models as complementary - whether they are inter-dependent or mutually exclusive description of the DUT. This explanation is similar to the complementarity principle expounded by the famous Quantum physicist of 20th century - Niels Bohr, who explained the wave-particle duality as mutually exclusive complementary descriptions of the same entity (only valid for entities/objects at quantum scale such as photons and electrons)[161], however with one big difference, whereas our measurements (blind men) are purely classical and the measurements they produce are macroscopic i.e. currents, voltages, capacitances etc which

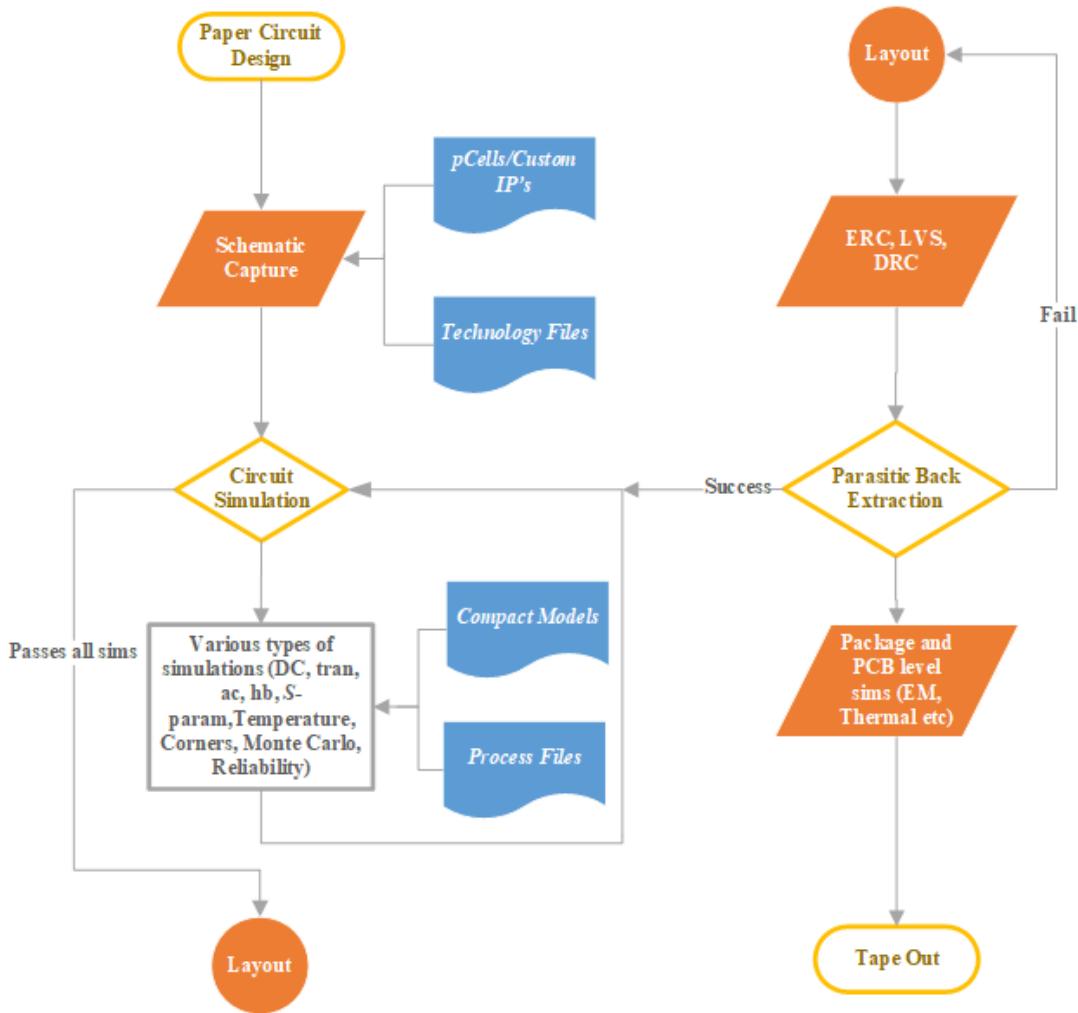


Figure 10.2: A general flow for analog/RF/power electronic custom integrated circuit (IC) and system co-design using a semiconductor process from a chosen foundry PDK, involving tools from companies such as Cadence (ADE), Keysight (ADS), National Instruments/Cadence (AWR) etc.

are *derived* quantities that describe an average behavior of an ensemble of microscopic particles such as electrons, Niels Bohr's principle describes the behavior of purely quantum particles/waves, whose quantized (discrete) description merges into classical (continuous) description at macroscopic scale.

Having given an epistemological explanation (use of blind men/various experiments to answer the question “What is an elephant/HEMT and how can we know about him/her/it?”)

of the modeling process, which eventually leads towards ontological realization of the being (elephant/HEMT in Fig. 10.1 which represents the objective truth in this case), we would like to know the utilitarian value of the resulting knowledge and models created thereon as practicing engineers. This brings us back to the discussion from chapt.1 about any analog/RF/power electronic circuit design using various commercial/non-commercial EDA tools from companies such as Cadence (ADE), Keysight (ADS), National Instruments/Cadence (AWR) etc. A unified, custom flow for such an IC and system co-design driven flow is given in Fig. 10.2. It shows compact models as being an integral part of the design process, with all the different types of simulations such as DC, transient, ac, harmonic balance (hb), temperature, corners, statistical Monte Carlo and reliability, whose veracity is based on the level of accuracy and stability (convergence) of the compact models of a chosen foundry's PDK, that contains the given integrated devices. These simulations can also be coupled with system level (package, PCB etc) EM/thermal simulations at the end as shown in Fig. 10.2, for overall system design. However, for discrete devices, where process specific technology files, pcells and process parameters based process files are unavailable, the process agnostic version of ASM-GaN (described fully in chapters 2, 3 & 4) would be a necessary and useful replacement. Furthermore, it is understood that a circuit design using discrete HV/LV HEMTs would exclude the portion related to an IC's layout, ERC (Electrical Rule Checks), LVS (Layout Vs Schematic), DRC (Design Rule Checks) and parasitic back extraction in Fig. 10.2 and instead will be replaced by various PCB layout design considerations, coupled with system level EM/thermal and circuit co-simulations.

10.2 Future Work

No research work can be complete without pointing towards future improvements, applications or birth of a new topic of research. Following is a compilation of such work based on this thesis:

- In chapt.4, we used OFF-state S -parameter measurements to model the package parasitics of a given power AlGaN/GaN HEMT. Further work on ON-state modeling of power HEMTs from ON-state S -parameter measurements could give more insights into the ON-state operation of power HEMTs. However, getting clean ON-state S -parameter measurements on power devices is a big challenge because of the noisy and non-meaningful amplitude-phase data, which we observed for our ON-state measurements performed on Panasonic's power HEMT PGA26E19BA.
- In chapt.5, we corrected the small-signal OFF-state capacitance component C_{ds} by reformulating its linear character into non-linear, in addition to $NLESR$, in order to derive a non-linear, large-signal model of output OFF-state capacitance C_{oss} . Thus, further work on large-signal equivalents of the remaining small-signal components of the power AlGaN/GaN HEMT's intrinsic model as shown in Fig. 2.3, after verifying if they need updates for large-signal modeling, could be an excellent topic of investigation into the question "What constitutes a complete large-signal model of a HEMT?".
- Improving the non-linear ESR ($NLESR$) & non-linear C_{ds} model of chapt.5 in terms of its physical explanation and perhaps verifying the generality of both linear and non-linear ESR models for other power devices based on different technologies (Si, SiC etc) and architectures (such as lateral and vertical power device structures) could be an excellent topic of research.

- Another impactful topic could be to develop a robust methodology for statistical modeling of power AlGaN/GaN HEMTs, when the data-sheets can't be trusted or have become obsolete and at the same time manufacturing (process) specs are not available; from single point measurements performed on a limited data-set, using BPV technique. For example, a small OEM (Original Equipment Manufacturer) orders some tens of samples and from single point DC measurements creates specs similar to the data-sheet in Table. 6.1 for corner and statistical model generation. The modeling team then creates a custom compact model of the power HEMT for accurate circuit design from DC I-V, C-V and OFF-state *S*-parameter measurements, with corners and statistical Monte Carlo models created from a limited data-set gained from measuring statistically less number of devices.
- Verification and application of the SRH trap model of chapt.7 assuming multiple trap centres, each having different time constants measured from transient drain-source current measurements[118], and studying the impact of such modeling on various kinds of circuit designs (RF, power etc) could be an excellent topic for an advanced research.
- In chapt.8, we modeled degradation in device characteristics of AlGaN/GaN HEMTs due to extreme temperatures and proton radiation exposure, using the trap model implemented in chapt.7. The next logical step would be to compare the circuit simulations using such models at extreme temperatures and radiation environments against data measured at circuit level, so that the impact of such modeling at circuit level can be studied in order to mitigate the ensuing degradation in circuit level performance.
- Chapt.9 gives an analytical model of the charge in p-GaN doped AlGaN/GaN HEMTs based on solution to the basic problem of electrostatics in the vertical

cross-section of a typical HEMT. In a commercial III-V semiconductor foundry, where engineers use calibrated TCAD tools such as Silvaco, Sentaurus etc in order to design the various integrated/packaged devices, this analytical model can be especially useful in verifying and adding corrections to the predictions from TCAD simulations, thus resulting in precise device design from an early design phase of a given III-V process.

Appendix A

Setup For Transient Simulation Of Power Electronic Circuits In Cadence Environment

A.1 The Problem Of Simulating Power Electronic Circuits

The core problem in simulating power electronic circuits that we would discuss in this appendix is about having a correct and convergent steady state solution to a given circuit, preferably in a transient simulation starting from $t = 0$ s, for convenience of a circuit designer. For achieving this, correct initial conditions, which are required for the algorithm for transient simulation in order to evaluate precise time evolution of voltages and currents in a given circuit, are a very important pre-requisite. For $t = 0$ s simulation, the simulator performs simple DC simulation to arrive at a stable solution for various nodal voltages and branch currents. The solution of DC simulation is determined by an iterative process, typically Newton-Raphson (N-R) with various criteria which try to minimize the residues

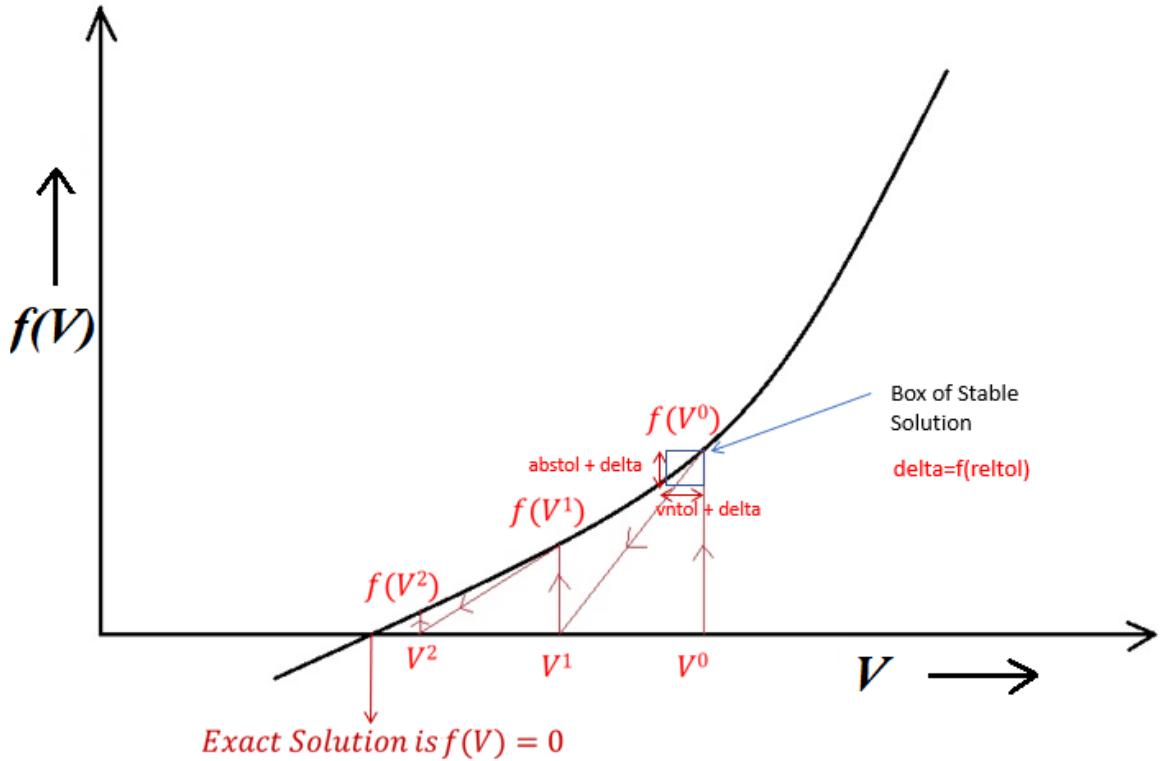


Figure A.1: Use of Newton-Raphson iterative method to solve KCL, in order to get a DC solution for given circuit.

of voltages, currents, power etc. Typical residue functions used for voltages and currents in Spectre simulator are given below:

$$\left| V_n^j - V_n^{j-1} \right| < \text{vntol} + \text{reltol} \times \max \left(V_n^j, V_n^{j-1} \right) \quad (\text{A.1a})$$

$$\left| f_n \left(V^j \right) - f_n \left(V^{j-1} \right) \right| < \text{abstol} + \text{reltol} \times \max \left(f_n \left(V^j \right), f_n \left(V^{j-1} \right) \right) \quad (\text{A.1b})$$

where V_n^j is the voltage at n^{th} node evaluated by the simulator according to the N-R method in the current iteration j , V_n^{j-1} is the voltage that was evaluated or guessed (for 0^{th} iteration) in the previous iteration and which didn't satisfy the residue criteria in (A.1), while $f(V)$'s are the corresponding currents evaluated using compact models. Equations (A.1a) & (A.1b) define a box of stable solution as shown in Fig. A.1. The iteration starts with initial assumption of values for all the nodal voltages V^0 as shown

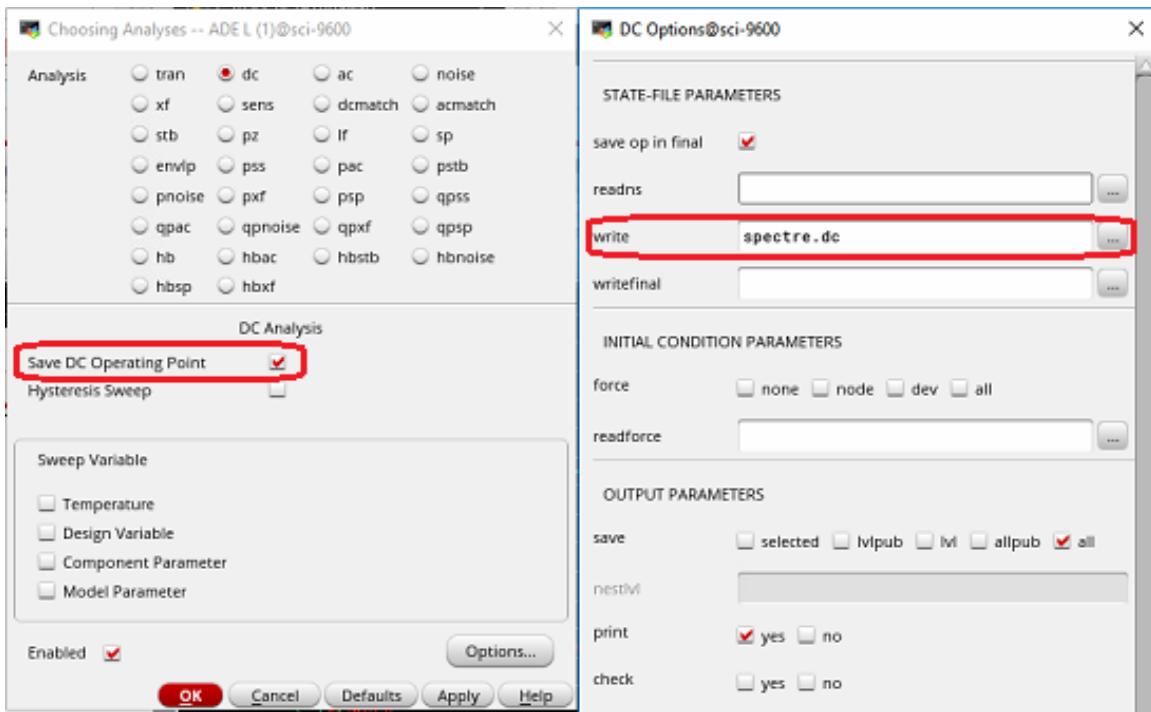


Figure A.2: Options to be entered in DC operating point simulation.

in Fig. A.1. Then, N-R method is used in an iterative manner till you arrive close to the actual solution $f(V) = 0$, i.e. when the solution of e.g. i^{th} iteration falls within the box of stable solution shown in Fig. A.1, the solution is said to be converged in i^{th} iteration and corresponding voltages V_n^i 's and currents $f(V_n^i)$'s are said to be the converged solutions for all n nodes in a given circuit.

The rationale behind using the criteria of residue is because a computer system can only understand numerical techniques to solve a set of algebraic equations, such as those given by KCL. A circuit simulator solves KCL and not KVL because KCL gives you exactly n number of algebraic equations for n nodes in a circuit; and even if we decide to use KVL instead, then identifying the number of non-redundant loops in a complex circuit will be very difficult to implement in a circuit simulation algorithm.

For transient simulation, the converged set of nodal voltages and branch currents arrived in DC solution of a circuit are used as initial conditions for solving a set of difference

```

# CHECKPOINT_VERSION 1
# Generated by spectre (mode: Spectre) from circuit file `input.scs` during analysis dcOp.
# 3:56:34 AM, Fri Aug 30, 2019
# Number of equations = 38
# The default unit is V, otherwise its unit is after #unit
D      400.000000000054
G      0
Lchoke:1      -2.69276631163002e-08  #unit A
MSwitch:1      -2.69276631163003e-08  #unit A
net1    400.000000000054
net03   400.000000000027
net07   400
net08   400.000000000054
Vdd:p   2.69276631163003e-08  #unit A
Vpulse:p   0  #unit A
MSwitch.dint  400.000000000054
MSwitch.gint  0
MSwitch.gmid 0
MSwitch.Ld:1  -2.69276631163003e-08  #unit A
MSwitch.Lg:1  0  #unit A
MSwitch.Ls:1  2.69276631163003e-08  #unit A
MSwitch.mn.di 53611.1032436548
MSwitch.mn.dt -8.60060122070157799  #unit C
MSwitch.mn.fp1 27045.1769742322
MSwitch.mn.fp2 400.000000002774
MSwitch.mn.fp3 400.000000002774
MSwitch.mn.fp4 400.000000002774
MSwitch.mn.gi 0
MSwitch.mn.si -1.38758248038295e-09
MSwitch.mn.trap1 0
MSwitch.mn.trap2 0
MSwitch.mn:d_fp4_flow -2.69280219684576e-08  #unit A
MSwitch.mn:di_si_flow -2.69276631163003e-08  #unit A
MSwitch.mn:di_si_probe 53611.1032436548
MSwitch.mn:fp3_fp2_flow -2.69276631163003e-08  #unit A
MSwitch.mn:fp4_fp3_flow -2.69276631163003e-08  #unit A
MSwitch.mn:g_gi_flow 0  #unit A
MSwitch.mn:si_s_flow -2.69276631163007e-08  #unit A
MSwitch.mn:trap1_flow 0  #unit A
MSwitch.mn:trap2_flow 0  #unit A
MSwitch.sint 0

```

(a)

```

# CHECKPOINT_VERSION 1
# Generated by spectre (mode: Spectre) from circuit file `input.scs` during analysis dcOp.
# 10:11:29 PM, Thur Aug 29, 2019
# Number of equations = 40
# The default unit is V, otherwise its unit is after #unit
D      399.999999999999
G      0
Lchoke:1      4.0003952448198e-10  #unit A
MSwitch:1      4.00039524481982e-10  #unit A
net1    399.999999999999
net03   400
net07   400
net08   399.999999999999
Vdd:p   -4.00039524481982e-10  #unit A
Vpulse:p   0  #unit A
MSwitch.dint  399.999999999999
MSwitch.gint  0
MSwitch.gmid 0
MSwitch.Ld:1  4.00039524481982e-10  #unit A
MSwitch.Lg:1  0  #unit A
MSwitch.Ls:1  -4.00039524481982e-10  #unit A
MSwitch.mn.di 399.999999999959
MSwitch.mn.dt 3.1619585634702e-11  #unit C
MSwitch.mn.fp1 399.999999999959
MSwitch.mn.fp2 399.999999999959
MSwitch.mn.fp3 399.999999999959
MSwitch.mn.fp4 399.999999999959
MSwitch.mn.gi 0
MSwitch.mn.si 2.06140366965565e-11
MSwitch.mn.trap1 0
MSwitch.mn.trap2 0
MSwitch.mn:d_fp4_flow 4.00155156534995e-10  #unit A
MSwitch.mn:di_si_flow 4.00039524481982e-10  #unit A
MSwitch.mn:di_si_probe 399.999999999959
MSwitch.mn:fp1_di_flow 4.00039524481982e-10  #unit A
MSwitch.mn:fp2_fp1_flow 4.00039524481982e-10  #unit A
MSwitch.mn:fp3_fp2_flow 4.00039524481982e-10  #unit A
MSwitch.mn:fp4_fp3_flow 4.00039524481982e-10  #unit A
MSwitch.mn:g_gi_flow 0  #unit A
MSwitch.mn:si_s_flow 4.00039524481982e-10  #unit A
MSwitch.mn:trap1_flow 0  #unit A
MSwitch.mn:trap2_flow 0  #unit A
MSwitch.sint 0

```

(b)

Figure A.3: For a circuit containing a voltage source of maximum 400 V - (a) ‘spectre.dc’ file with wrong prediction of voltage (≈ 27 KV) at ASM-GaN model’s internal node fp1 & (b) ‘spectre.dc’ file with correct prediction of voltage (400 V) at ASM-GaN model’s internal node fp1.

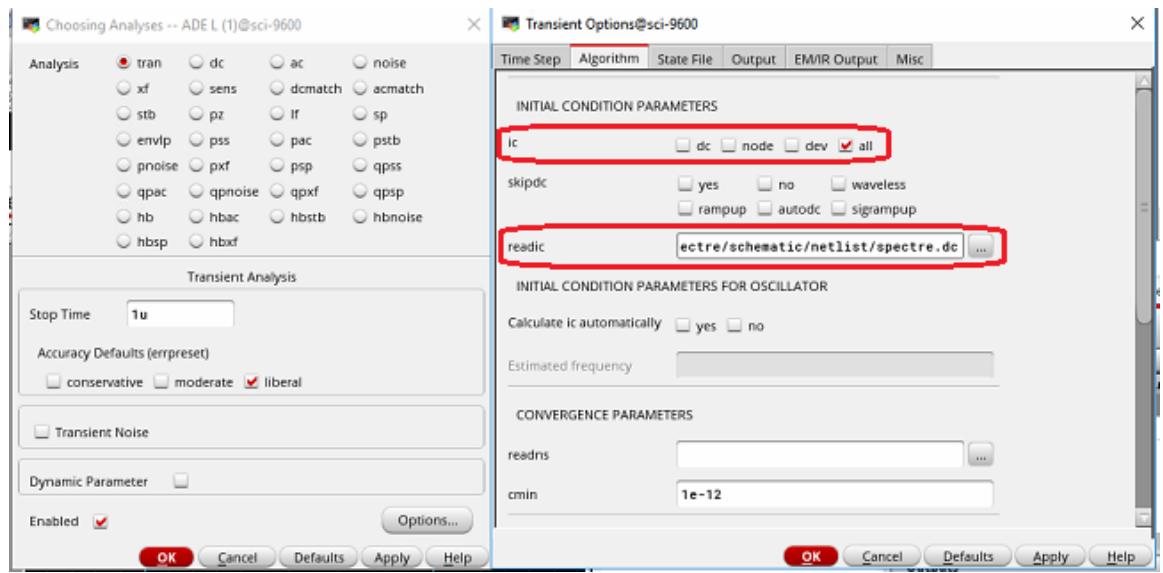


Figure A.4: Options to be entered in transient simulation for specifying initial condition file - ‘spectre.dc’ saved after performing the DC operating point analysis.

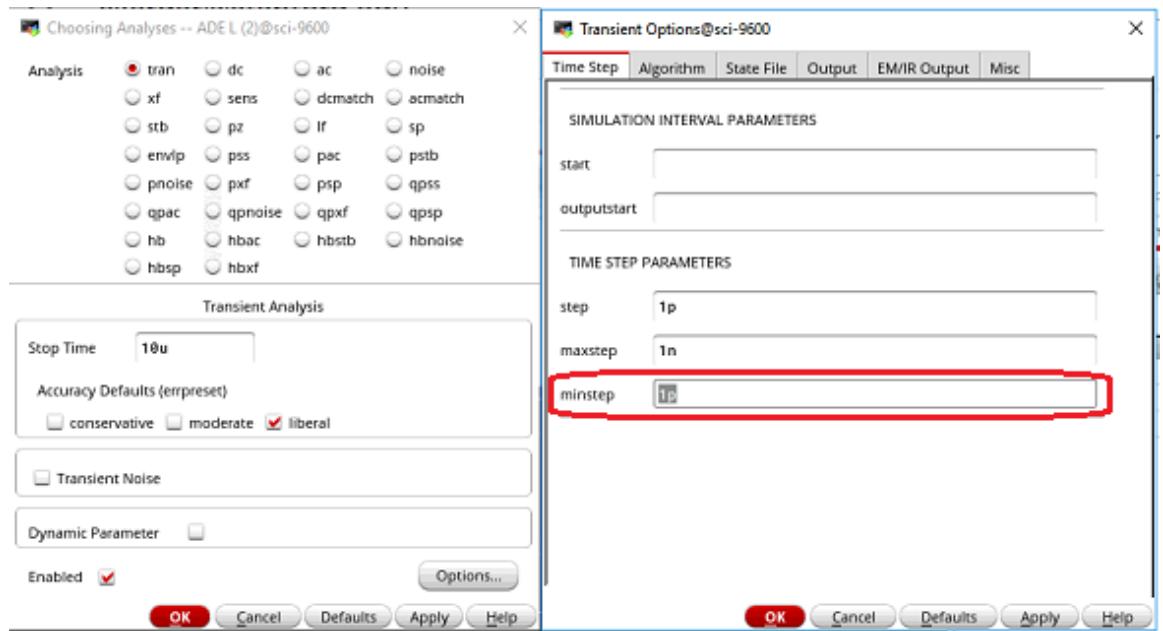


Figure A.5: Options to be entered in transient simulation for setting minimum time step.

equations formed for a given circuit using KCL. Here, it's interesting to note that for DC solution, the equations were simple algebraic equations using KCL at each node. However for transient analysis, difference equations are formed from the governing differential equations. Then, known methods of solving difference equations such as Euler's method are used to solve for the time evolution of voltages, while assuming linear or quadratic shape of solution space of currents i.e $f(V)$ in Fig. A.1, with time replacing the voltages plotted on the horizontal axis (obviously locus of $f(V)$ vs time is different from that vs voltage). Once a set of nodal voltages are evaluated by solving the difference equations, the currents ($f(V)$) are given by the various linear/non-linear compact models present in the circuit. It's here that the main problem in simulating power circuits arises. The problem is that if the supply voltages are very high and voltage signal rise/fall times are small, then the various methods used to arrive at transient solution such as Euler's method, can give very large and unrealistic values of voltages at certain nodes. For example, for a circuit containing supply voltage of hundreds of volts, certain nodal voltages going to a value of tens of KV's at a certain point in time is certainly a failure of the simulation algorithm. So, in nutshell, convergence in transient simulation requires following:

A) DC solution to be convergent. One way to achieve DC convergence is to relax the default values of tolerance parameters used in residue evaluation, such as `reltol` and `abstol` (A.1), which can loosen or tighten the box of stable solution as shown in Fig. A.1. However loosening the tolerances can have an adverse impact on the accuracy of the solution as the box of stable solution becomes bigger. Hence, other methods such as `gmin` and `cmin` stepping in transient and ac simulations are suggested. These methods add a path of very high impedance from a floating or highly non linear node to ground and thus increase the slope locally around the m^{th} solution V^m , so that for $(m + 1)^{th}$ iteration, the solution falls within the box of stable solution.

and

B) Variation in the temporal solution of nodal voltages to be relatively slow w.r.t the minimum time step specified. If this is not the case, we get unusually high voltage and current swings as solutions which are evidently nonphysical.

A.2 Solution

In order to achieve convergence in transient simulations in power circuit simulations using Cadence's Analog Design Environment (ADE) that uses Spectre simulator, we have discovered following steps which have worked for most of the power circuits that we simulated in this work (the steps are valid for any other circuit simulator because the algorithms for DC and transient simulations generally don't change from simulator to simulator):

1. Ensure that DC convergence is achieved in the circuit. For this, perform a DC operating point analysis with the value of supply voltages same as the initial condition ($t = 0$ s) of the circuit. Ensure that the value of nodal voltages and currents make sense. Spectre simulator saves the output of this as 'spectre.dc' file when you specify the options in DC analysis as shown in Fig. A.2. This file must be checked for consistency.

For example, Fig. A.3a shows that for a given 'spectre.dc' file, device instance 'MSwitch' of the AlGaN/GaN HEMT - PGA26E19BA that has been implemented as a sub-circuit model in the file 'nmos4.scs' of appendix. B, has an incorrect DC solution of ≈ 27 KV for internal node fp1 belonging to the sub-circuit component 'mn' of the overall sub-circuit model - 'nmos4'. This is because the maximum voltage being applied to the circuit is 400 V. Fig. A.3b shows the correct solution achieved using tolerance parameters or gmin/cmin stepping as explained earlier.

2. Include the correct 'spectre.dc' file created in step 1 as the initial condition file in the transient simulation options as shown in Fig. A.4. This will give correct set of initial conditions for the transient algorithm and will avoid transient convergence errors

for most of the circuits. In case you want to simulate steady-state simulation right from $t = 0$ s, which is how we have performed simulations in chapt.5, you will need the correct steady-state initial conditions for all the nodal voltages and/or branch currents in a given circuit, and then manually enter them in the ‘spectre.dc’ file or use the initial condition or node-set statements to initialize the known steady-state initial conditions.

3. If step 2 still gives convergence errors, then set the minimum time step parameter ‘minstep’ in the transient simulation setup to be as minimum as possible (preferably less than one tenth of the rise or fall times of voltages/currents in the circuit) as shown in Fig. A.5. Specifying the minimum time step explicitly ensures that the evaluated solution space for nodal voltages in transient algorithm doesn’t explode beyond the value of maximum voltages defined in a given circuit.

Appendix B

Model Cards For Simulation With Calibrated Model Of Panasonic's Power HEMT: PGA26E19BA

Since most of the simulations in this work were performed in Cadence's Spectre simulator, in addition to Keysight's ADS in ICCAP environment, we are giving the final model card of Panasonic's power AlGaN/GaN HEMT device PGA26E19BA in Spectre format. The same model card can be converted into ADS format for simulation in ICCAP environment. Please note that the following file is saved by the name "nmos4.scs".

```
1 // The model card file starts with all the include statements for
  Verilog-A model source code "asmhemt_power.va" and Spectre include
  file "stats_include.scs", as defined in listing B.2, for corner and
  statistical simulations.

2 ahdl_include "asmhemt_power.va"
3 include "stats_include.scs" section=typical // Mandatory include for
  corner and Monte Carlo simulations. Other corner options are "
```

```

    as_measured", "fast", "slow" and "coss_loss". Please use typical
    corner only for Monte Carlo simulations, as by definition, Monte
    Carlo simulation is not defined for other corners.

4 include "stats_include.scs" section=monte_carlo // Optional. Include for
    Monte-Carlo simulations only.

5 // Start of the sub-circuit model definition of Fig. 4.1.

6 inline subckt nmos4 (d g s b)

7 // Define the key model parameters that determine the observed
    electrical measurements such as Ron, Vth etc for statistical
    simulations in chapt.6. The sub-circuit model parameters res_fac,
    vth_fac etc from "stats_include.scs" (see listing B.2) are used for
    tuning source/drain contact resistances, threshold voltage etc to the
    data-sheet values in order to center the as measured model
    parameters to either the corner specs (min/typ/max) given in the data
    -sheet (corner values possible = as_measured, typical, fast, slow) in
    chapt.6 or for calibrating the as measured model to the different
    specimen of the same device for simulating the Coss losses in chapt
    .5.

8 parameters voff_dev=vth_fac*1.8
9 parameters rdc_dev=res_fac*61e-3
10 parameters rsc_dev=res_fac*31e-3
11 parameters rss0_dev=res_fac*20.53e-3
12 parameters rdd0_dev=res_fac*40e-3
13 parameters rgc_dev=798.8e-3
14 parameters cgdo_dev=cgdo_fac*20e-12
15 parameters cgso_dev=cgso_fac*201.1e-12
16 parameters cdso_dev=cdso_fac*39.53e-12
17 parameters cgdl_dev=cgdl_fac*146.9e-15
18 // Following are instances of three inductances belonging to the
    extrinsic model of Fig. 4.1 with values taken from table 4.1 and
    intrinsic device "mn".

```

```

19 Lg (gext g) inductor l=632.7e-12
20 Ld (dext d) inductor l=616.4e-12
21 Ls (sext s) inductor l=328.4e-12
22 mn (d g s b) nmod
23 // Definition of the model "nmod" that has been instantiated in previous
   statement with instance name "mn", with all the model parameters
   taken from tables 3.1, 3.2, 4.1. Please note that the linear and non-
   linear ESR models formulated in chapt.5 for modeling the OFF-state
   Coss losses have not been parameterized in the ASM-GaN model and
   hence not given below.
24 model nmod asmhemt_power
25 + voff = voff_dev
26 + rdc = rdc_dev
27 + rsc = rsc_dev
28 + rss0 = rss0_dev
29 + rdd0 = rdd0_dev
30 + rgc = rgc_dev
31 + cgdo = cgdo_dev
32 + cgso = cgso_dev
33 + cdso = cdso_dev
34 + cgdl = cgdl_dev
35 + cgg0 = 2.264e-3
36 + beta0 = 400e+3
37 + areafac = 160e+3
38 + imin0 = 700e-9
39 + vdsat0 = 0.9
40 + rdsmodpa = 1
41 + mexpacc = 2
42 + idmax = 28
43 + eta0 = 12e-3
44 + at = -2

```

```
45 + ute = -2
46 + nfactor = 0.5
47 + vdsscale = 5
48 + shmod = 1
49 + rth0 = 2
50 + vdssatcv = 121
51 + qm0i = 9.918e-12
52 + fp1mod = 1
53 + fp2mod = 2
54 + cgg0fp1 = 1.01e-3
55 + cgg0fp2 = 0.2132e-4
56 + areafacfp1 = 97.09e+3
57 + areafacfp2 = 1
58 + vofffp1 = -22
59 + vofffp2 = -76
60 + vdsscalefp1 = 4
61 + vdsscalefp2 = 4
62 + nfactorfp1 = 0.1
63 + nfactorfp2 = 0.1
64 + qm0fp1 = 4.177
65 + qm0fp2 = 41.83
66 + adosfp1 = 110.2e+12
67 + adosfp2 = 1.794e+19
68 + bdosfp1 = 1.258
69 + bdosfp2 = 1.588
70 + csubscalei = 1e-3
71 + csubscale1 = 19.87e-3
72 + csubscale2 = 283.1e-3
73 + cfp1scale = 18.19e-12
74 + cfp2scale = 350e-3
75 + vdssat0fp1 = 1
```

```

76 + vdsat0fp2 = 1
77 + cfgd = 95e-15
78 + cfgd0 = 16e-12
79 + cds1 = 30e-15
80 ends nmos4

```

Listing B.1: Model card file for Panasonic’s power HEMT device PGA26E19BA, named “nmos4.scs” in Spectre format to be used with 4 terminal nmosfet symbol “nmos4” in Cadence ADE environment.

The following listing gives the model card file used for specifying corner or statistical simulations of chapt.6 or C_{oss} loss model of chapt.5. If you don’t want to use the statistical simulation or the ‘typical’ corner or the ‘fast’, ‘slow’ or ‘coss_loss’ corners, use the corner ‘as_measured’ from the file “stats_include.scs” as defined in listing B.2 below:

```

1 // Following file contains various sections, which represent either Coss
   loss model, a statistical model or a corner model based on the data-
   sheet of the power HEMT device PGA26E19BA.
2 section monte_carlo
3 // Statistics block specifies information to Spectre simulator about the
   type of distribution in the model parameter, such as Gaussian,
   uniform etc, along-with all the sigma values to be used in the Monte
   Carlo simulation. The sigma values can be given as absolute or
   relative (in percent) w.r.t the mean/average value. The statement "
   truncate tr=nsig" is used to specify the coverage of the distribution
   to '+/-' nsig*sigma' values, e.g. +/- 3*sigma for nsig=3 as in the
   code below, which simulates the six sigma variation in the model
   parameters about their mean.
4 statistics {
5     process {
6         vary voff_dev dist=gauss std=0.4/3
7         vary rdc_dev   dist=gauss std=40.2032e-3/3
8         vary rsc_dev   dist=gauss std=10.2672e-3/3

```

```
9      vary rss0_dev dist=gauss std=6.8e-3/3
10     vary rdd0_dev dist=gauss std=13.248e-3/3
11     vary rgc_dev    dist=gauss std=25 percent=yes
12     vary cgdo_dev  dist=gauss std=25 percent=yes
13     vary cgso_dev  dist=gauss std=25 percent=yes
14     vary cdso_dev  dist=gauss std=25 percent=yes
15   }
16
17   truncate tr=3.0
18 }
19 endsection monte_carlo
20
21 section as_measured
22 parameters res_fac=1
23 parameters vth_fac=1
24 parameters cgdo_fac=1
25 parameters cgso_fac=1
26 parameters cdso_fac=1
27 parameters cgdl_fac=1
28 endsection as_measured
29
30 section typical
31 parameters res_fac=0.906
32 parameters vth_fac=0.944
33 parameters cgdo_fac=0.85
34 parameters cgso_fac=0.7877
35 parameters cdso_fac=0.7033
36 parameters cgdl_fac=0.911
37 endsection typical
38
39 section fast
```

```
40 parameters res_fac=0.5748
41 parameters vth_fac=0.777
42 parameters cgdo_fac=0.85
43 parameters cgso_fac=0.7877
44 parameters cdso_fac=0.7033
45 parameters cgdl_fac=0.911
46 endsection fast
47
48 section slow
49 parameters res_fac=1.233
50 parameters vth_fac=1.167
51 parameters cgdo_fac=0.85
52 parameters cgso_fac=0.7877
53 parameters cdso_fac=0.7033
54 parameters cgdl_fac=0.911
55 endsection slow
56
57 section coss_loss
58 parameters res_fac=1
59 parameters vth_fac=1
60 parameters cgdo_fac=0.89
61 parameters cgso_fac=1
62 parameters cdso_fac=0.89
63 parameters cgdl_fac=1
64 endsection coss_loss
```

Listing B.2: Spectre include library file for corner, statistical and C_{oss} loss simulations - “stats_include.scs”.

Appendix C

Curriculum Vitae

C.1 Personal Details

- Name: **Dhawal Dilip Mahajan**
- DOB: 26/09/1982
- Nationality: **Indian**
- Sex: Male
- Languages: Marathi, Hindi, English
- email: dhawal.mahajan@gmail.com
- Permanent Address: 368, Vijay Raj Apts, Rangole Marg, Khare Town, Dharampeth, Nagpur, Maharashtra, India - 440010
- Phone No: +91 9591378508

C.2 Education

- **M.Tech**, Microelectronics, **IIT Mumbai** (2005 - 2007)
- **B.E**, Electronics, **Nagpur University** (2000 - 2004)

C.3 Skills

1. *Device Simulation/Modeling*: ICCAP, Verilog A, Silvaco
2. *Circuit Design*: Cadence ADE, AWR, SPICE, LTSpice, HSPICE, Spectre, Spec-tremdl
3. *Computational/Statistical/Scripting*: Python, C, ACE, Excel
4. *Characterization Lab Skills*: Various Cascade probe stations, Keysight's parameter analyzers and C-V meters

C.4 Professional Associations And Responsibilities

- Student Member, **IEEE**, USA
- Active reviewer of IEEE's *Transactions on Electron Devices* (TED)
- Active reviewer of IEEE's *Transactions on Microwave Theory and Techniques* (TMTT)
- Active reviewer of IEEE's *Journal of Electron Device Society* (JEDS)
- Active reviewer of **ECS**'s *Journal of Solid State Science and Technology* (JSS)

C.5 Work Experience

1. MTS, Device Modeling, PDK Enablement, **Globalfoundries** (Dec'2015 - Oct'2017)
 - *Compact Modeling*: Complete DC, CV and RF modeling of Silicon On Insulator(SOI) MOSFET's for 180 nm, 130 nm processes
 - *Reliability*: Generation and verification of Reliability models of 45 nm SOI process for HCI and NBTI
 - *Layout Design*: Designing and taping out of DC and RF test structures for compact modeling
2. MTS, Device Modeling, TR&D Dept, **Maxim Integrated** (Sept'2007 - Nov'2015)
 - *Compact Modeling*: Measurement and complete DC, CV, process and mismatch (Monte-Carlo) modeling of LV CMOS and HV Power MOSFET's using BPV/FPV method. Measurement and modeling of LDMOS, BJT's, Diodes, ESD's and passives for 180 nm, 130 nm and 90 nm BCD(Bipolar, CMOS, DMOS) process
 - *Reliability*: Measurement, generation and verification of Reliability models for HCI and mismatch due to HCI and NBTI
 - *Foundry PDK Validation*: Feedback to foundry based on Model Validation with the measured inline data from foundry
 - *Statistical split lot analysis*: Analysis of process robustness, based on deep understanding of device physics and comprehensive analysis after data mining the split lot data generated based on DOE's
 - *Latch-up prevention*: Providing solution to mitigate substrate injection and eventual latch-up due to conducting parasitic bipolar of a HV n-Epi process

- *Model QA*: Coding QA programs based on Python script that takes in any model library file and QA's the functionality and IOS specs of all the types of devices - MOSFETs, Diodes, BJTs and passives(R/L/C)

Appendix D

List Of Publications

D.1 Journal Publications

1. **D. D. Mahajan**, S. A. Albahrani, R. Sodhi, T. Eguchi and S. Khandelwal, “Physics-Oriented Device Model for Packaged GaN Devices,” in *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 6332-6339, June 2020, doi: 10.1109/TPEL.2019.2953060.
2. **D. Mahajan** and S. Khandelwal, “Analysis and modeling of OFF-state hysteretic losses in GaN power HEMTs,” submitted to *Solid State Electronics* Journal.
3. S. A. Albahrani, **D. Mahajan*** et al., “Extreme Temperature Modeling of Al-GaN/GaN HEMTs,” in *IEEE Transactions on Electron Devices*, vol. 67, no. 2, pp. 430-437, Feb. 2020. doi: 10.1109/TED.2019.2960573.
4. S. A. Albahrani, **D. Mahajan***, J. Hodges, Y. S. Chauhan and S. Khandelwal, “ASM GaN: Industry Standard Model for GaN RF and Power Devices—Part-II: Modeling of Charge Trapping,” in *IEEE Transactions on Electron Devices*, vol. 66, no. 1, pp. 87-94, Jan. 2019, doi: 10.1109/TED.2018.2868261.

*Equal contribution authors.

5. S. A. Albahrani , **D. Mahajan** et al., “Modeling of the Impact of the Substrate Voltage on the Capacitances of GaN-on-Si HEMTs,” in *IEEE Transactions on Electron Devices*, vol. 66, no. 12, pp. 5103-5110, Dec. 2019, doi: 10.1109/TED.2019.2948828.
6. S. Khandelwal, Yogesh Singh Chauhan, Tor A. Fjeldly, Sudip Ghosh, Ahtisham Pampori, **Dhawal Mahajan**, Raghvendra Dangi, Sheikh Aamir Ahsan, “ASM GaN: Industry Standard Model for GaN RF and Power Devices—Part 1: DC, CV, and RF Model,” in *IEEE Transactions on Electron Devices*, vol. 66, no. 1, pp. 80-86, Jan. 2019, doi: 10.1109/TED.2018.2867874.
7. Hossein Eslahi, **Dhawal Mahajan**, Sayed Ali Albahrani, Sourabh Khandelwal, “Design methodology considering evolution of statistical corners under long term degradation”, in *Microelectronics Journal*, Volume 91, 2019, Pages 36-41, <https://doi.org/10.1016/j.mejo.2019.07.006>.
8. H. Eslahi, S. A. Albahrani, **D. Mahajan** and S. Khandelwal, “An Analytical Model for Hot Carrier Induced Long-Term Degradation in Power Amplifiers,” in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, doi: 10.1109/TCAD.2019.2952554.

D.2 Conference Publications

1. **D. Mahajan** and S. Khandelwal, “Impact of p-GaN layer Doping on Switching Performance of Enhancement Mode GaN Devices,” 2018 *IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Padua, 2018, pp. 1-4, doi: 10.1109/COMPEL.2018.8460098.
2. **D. Mahajan**, S. A. Albahrani, H. Eslahi and S. Khandelwal, “A Study of Hard Switching Characteristics of GaN-based DC-DC Boost Power Converter using ASM-

GaN Compact Model,” *2018 Australasian Universities Power Engineering Conference (AUPEC)*, Auckland, New Zealand, 2018, pp. 1-4, doi: 10.1109/AUPEC.2018.8757974.

3. **D. Mahajan**, S. A. Albahrani, J. Hodges and S. Khandelwal, “Robust Circuit Model for GaN-Based Radiation-Hard Electronics,” *2018 IEEE Nuclear Science Symposium and Medical Imaging Conference Proceedings (NSS/MIC)*, Sydney, Australia, 2018, pp. 1-2, doi: 10.1109/NSSMIC.2018.8824520.
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6. H. Eslahi, S. A. Albahrani, **D. Mahajan** and S. Khandelwal, “A Tunable Input-Impedance Matching Approach for Long-term Degradation effects of Power Amplifier,” *2018 IEEE International RF and Microwave Conference (RFM)*, Penang, Malaysia, 2018, pp. 151-154, doi: 10.1109/RFM.2018.8846551.

D.3 Invited Talks And Tutorials

1. 25th May’2020 & 26th May’2020 – Delivered an online tutorial series on “Advanced Concepts in Circuit Simulation and Compact Modeling” in collaboration with local chapter of IEEE.
2. 4th March’2020 to 18th March’2020 – Delivered a tutorial series on “DFT and

Test Application Requirements for Functional Safety” at Center For VLSI AND Nanotechnology, VNIT, Nagpur.

3. 29th May'2019 – Delivered a talk on “Advanced concepts in simulation” for PhD students of Prof. Karmarkar at IIT Madras.

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