CS311-COMPUTER ARCHITECTURE

ASSIGNMENT-3 REPORT

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ABSTRACT:

A BASIC PIPELINED PROCESSOR HAS BEEN IMPLEMENTED.

IMPLEMENTATION:

THE PROCESSOR IS SIMULATED BY FOLLOWING THE ISA SPECIFICATIONS OF THE TOYRISC AND THE CODE FOR EACH UNIT WAS CLOSELY BASED ON THE W ORKING ON OF THE SIMPLERISC TAUGHT IN THE CLASS.

SUBMISSION:

THE SUBMITTED ZIP FILE CONSISTS OF THE STATS FOLDER WHICH CONSISTS OF OBSERVED STATS FILES AND THE SRC FOLDER.

OBSERVATION:

THE NUMBER OF INSTRUCTIONS AND THE NUMBER OF CYCLES FOR THE ASSEMBLY PROGRAMS DONE AS A PART OF ASSIGNMENT-1 HAS BEEN TABULATED HERE.

ASSEMBLY FILE NAME	NUMBER OF CYCLES	NUMBER OF INSTRUCTIONS
DESCENDING.ASM	277	277
FIBONACCI.ASM	90	90
PALINDROME.ASM	108	108
PRIME.ASM	7	7
EVEN-ODD.ASM	5	5

TABLE: STATISTICS TABLE