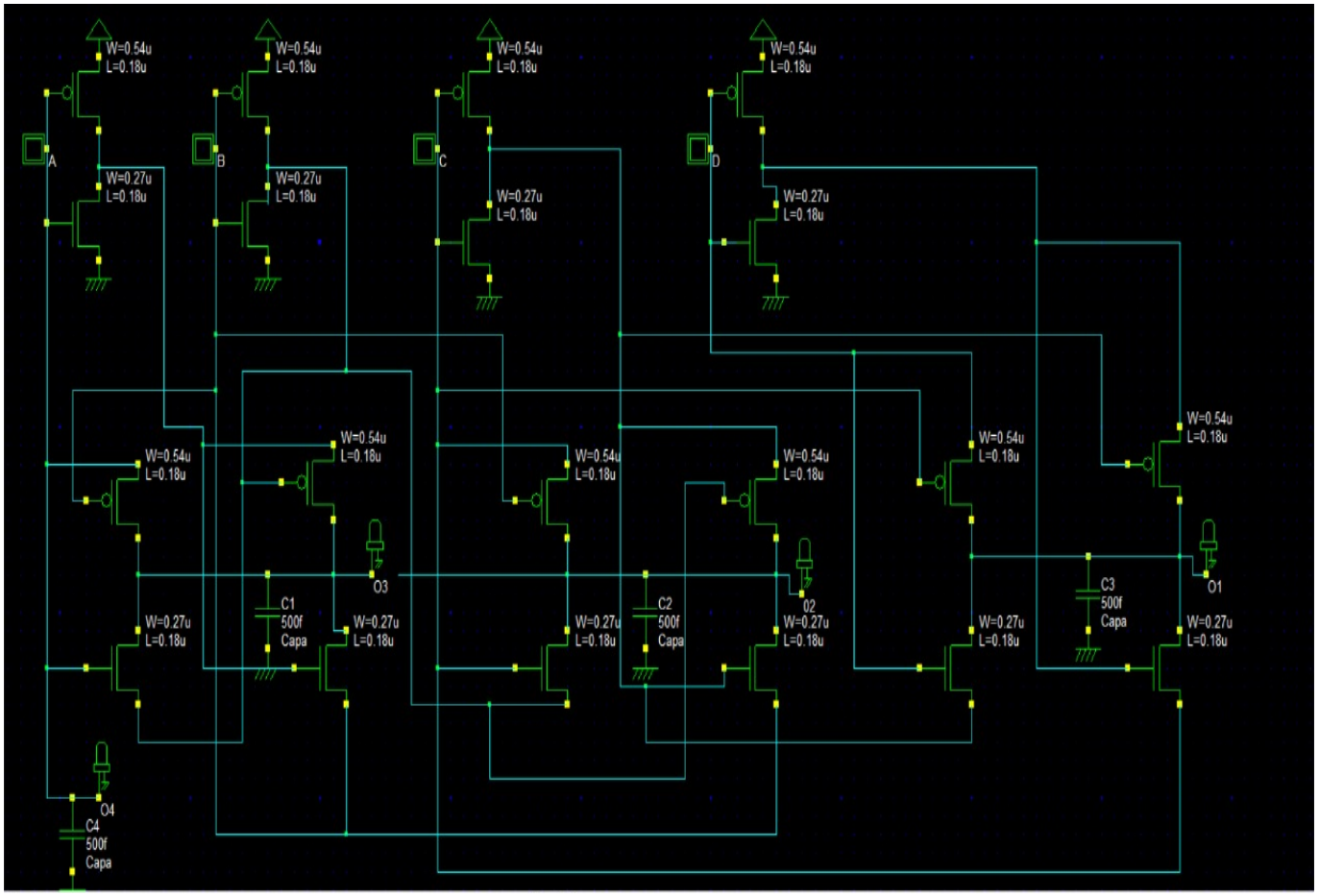
Q.1. Design a Binary-to-Gray code Converter at 1GHz with load capacitance of 500fF.

Logic Used- Double Pass Transistor Logic. This logic was used to design this circuit on account of least power consumption and time delay amongst all topologies listed, as per various research papers published.

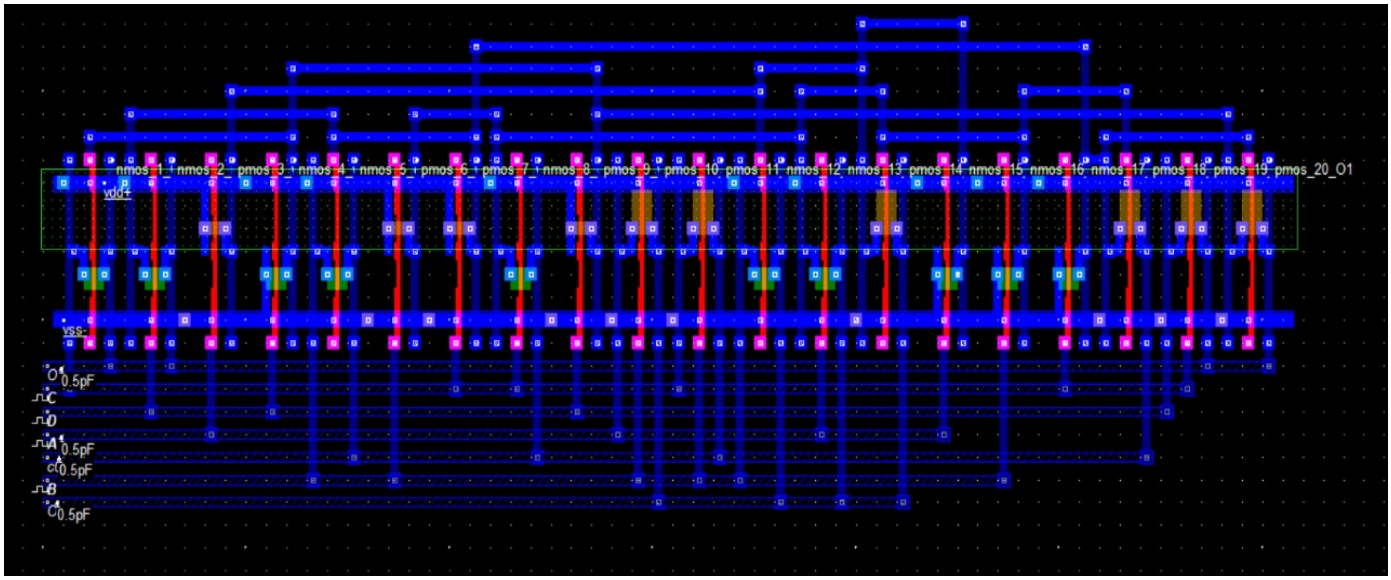
A	B	C	D	O4	O3	O2	O1
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

O1=C’D + CD’
O2=B’C + BC’
O3=A’B + AB’
O4=A

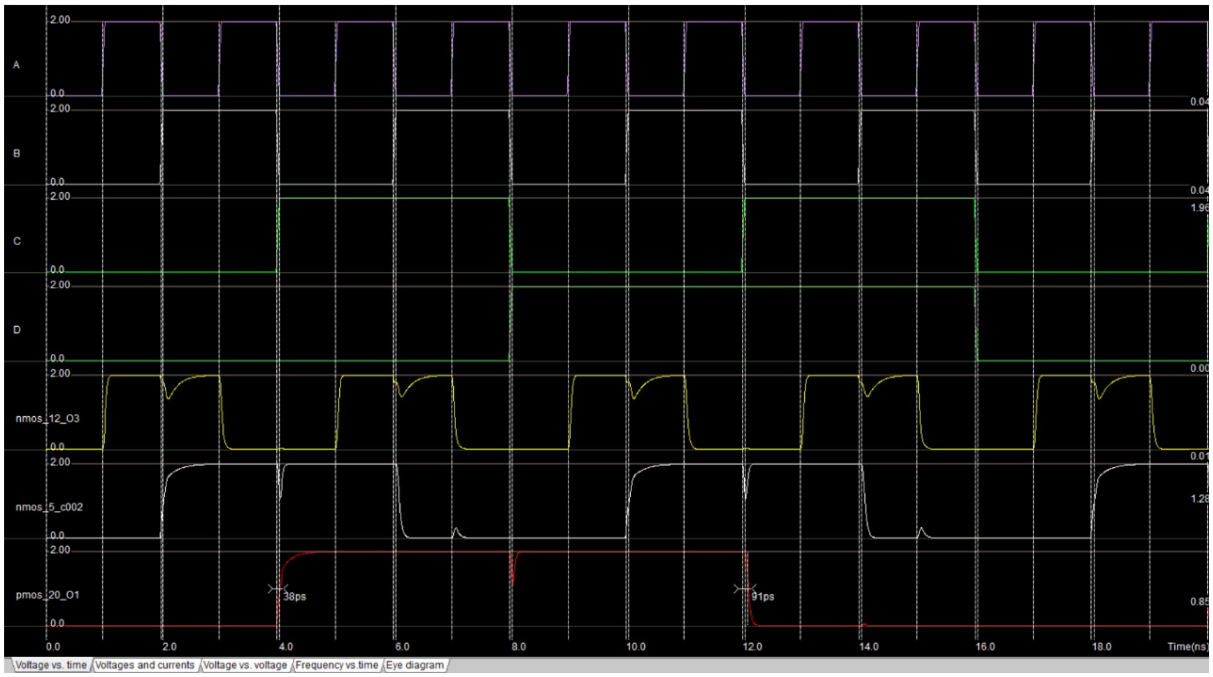
Schematic



Layout



Outputs



Parameters	Values
$(W/L)_n$	1.5
$(W/L)_p$	3
Time-Delay(O3)	604ps
Time-Delay(O2)	721.5ps
Time-Delay(O1)	1743.5ps
Power consumed	244 micro Watt