COMPUTER ARCHITECTURE
CS2010

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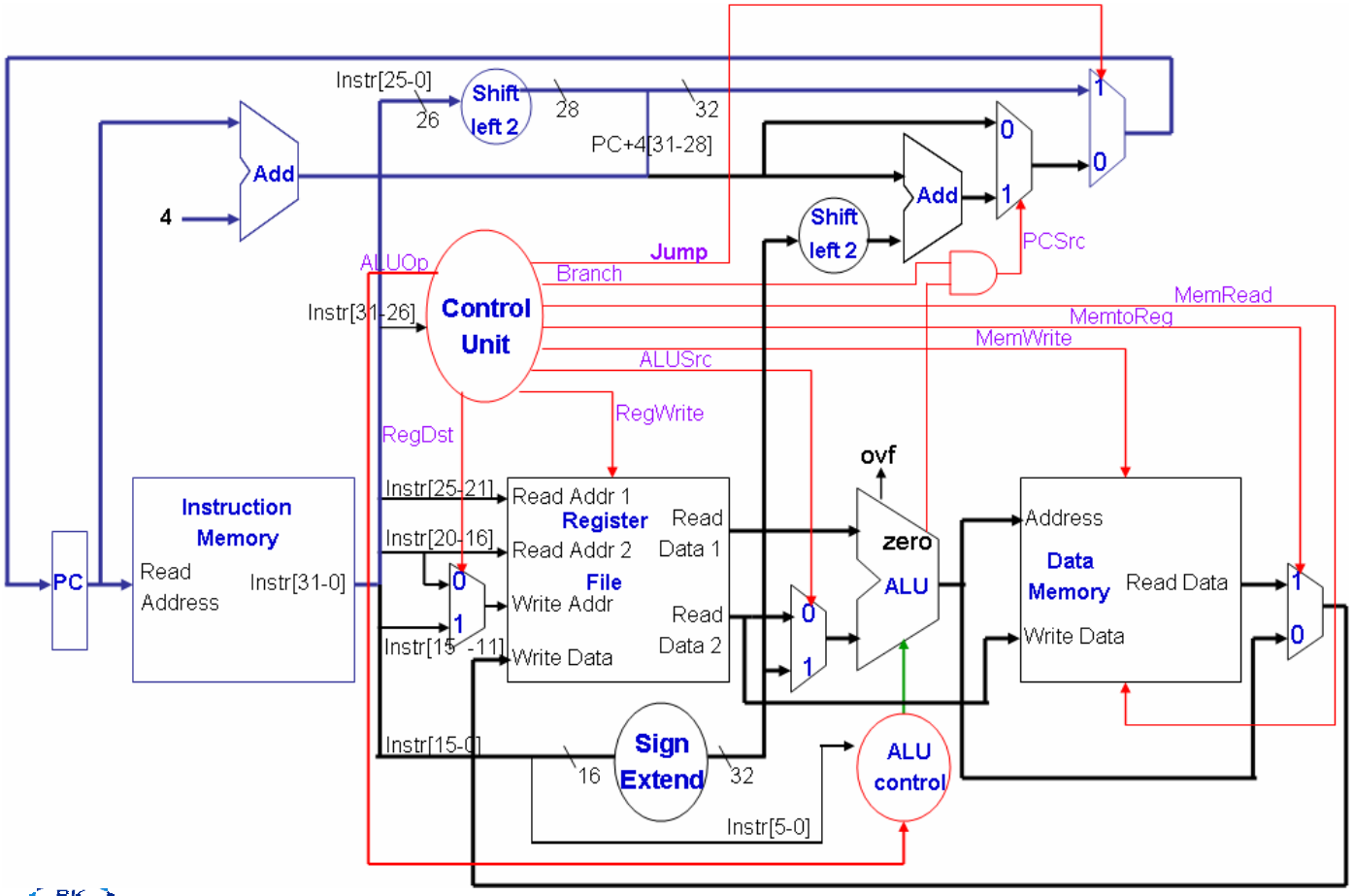
Chapter 4

THE PROCESSOR

Exercise 1

- Assuming we have a hardware with single clock implementation and latencies of blocks showed on the table below.
- What is the critical path (longest-latency) for a MIPS AND instruction ?
- What is the clock cycle time ?



I-Mem	400ps
Add	100ps
Mux	30ps
ALU	120ps
Regs	200ps
D-Mem	350ps
Control	100ps

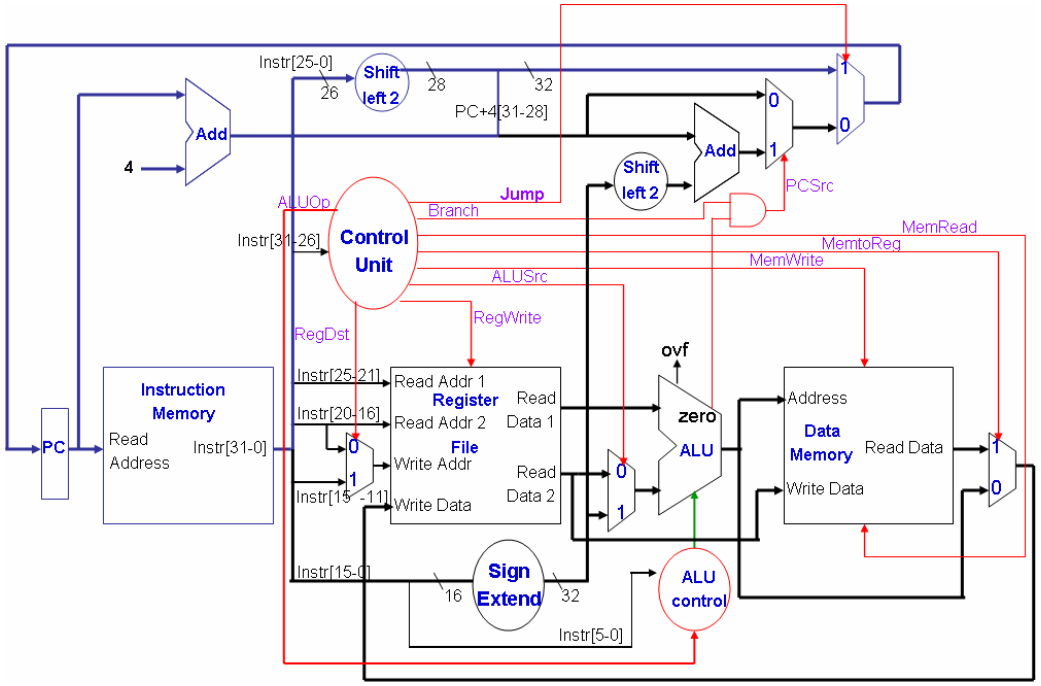
Exercise 1

- The the critical path (longest-latency) for a MIPS AND instruction
  - I-Mem ->Regs -> Mux -> ALU -> Mux
- The critical path for LOAD instruction
  - I-Mem ->Regs -> Mux -> ALU -> D-Mem->Mux
  - CC = 400 + 200 + 30 + 120 + 350 + 30 = 1130ps

Exercise 2

- How long should the control unit generate the MemWrite signal ?
  - Maximum time is CC – I-Mem = 1130ps – 400ps
- How about RegWrite?

I-Mem	400ps
Add	100ps
Mux	30ps
ALU	120ps
Regs	200ps
D-Mem	350ps
Control	100ps



Exercise 3

- Assume that the instructions executed by a processors are broken down as follows.

ALU	Beq	lw	sw
50%	25%	15%	10%

- Assuming there are no stalls or hazards, calculate speedup with pipelined organization and multi-cycle.
  - (0.15 x 5 + (0.5 + 0.25 + 0.1) x 4) * IC * CC
  - 1 * IC * CC

Exercise 4

- Indicate dependences and their type for the following sequence of instruction

  I1: lw $1,40($6)

  I2: add $6,$2,$2

  I3: sw $6,50($1)

- Assume there is no forwarding in this pipelined processor. Indicate hazards and add **nop** instruction to eliminate them
- Assume there is full forwarding. Indicate hazards and add **nop** instruction to eliminate them

Exercise 4

I1: lw $1,40($6)

I2: add $6,$2,$2

I3: sw $6,50($1)

lw $1,40($6)

add $6,$2,$2

nop

sw $6,50($1)