COMPUTER ARCHITECTURE
CS2010

Faculty of Computer Science and Engineering
Department of Computer Engineering

Nam Ho
namh@cse.hcmut.edu.vn

Chapter 5

MEMORY SYSTEMS

Exercise 1

- Design memory system with a cache L1 having size 4KB. Assuming that memory access uses SRAM chip 16M x 8 and each cache line has 1 word. CPU reads/writes 1 byte for each access.
- a). Using direct-mapped cache
- b). Using 4-way set associative cache
- c). Using fully associative cache

Exercise 1

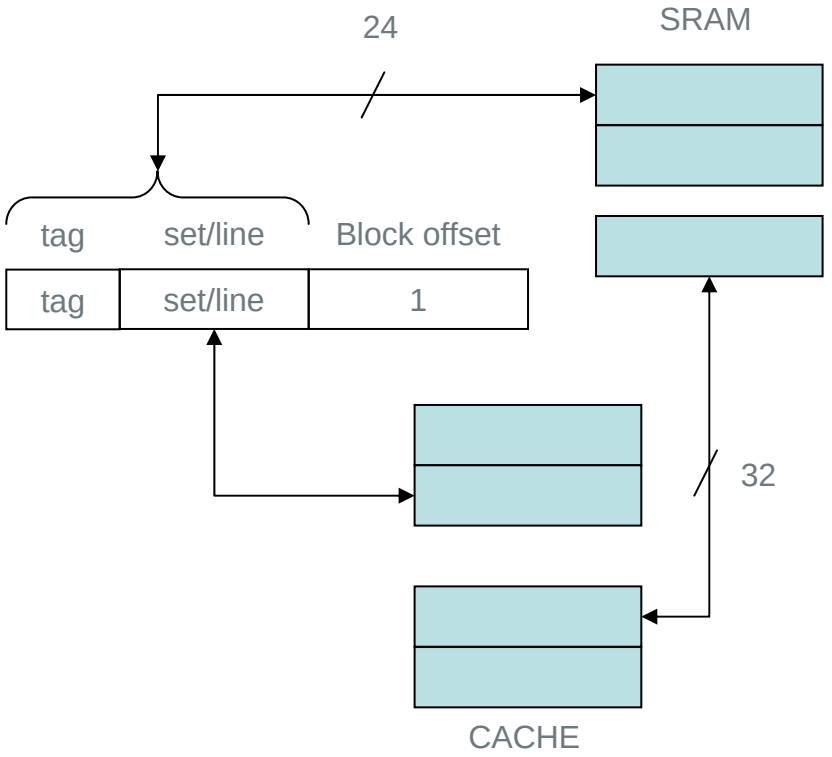
- a
  - 4KB cache = 2^12, line = 2^2 , 16MB = 2^24
  - => r =10
  - => w = 2
  - Tag = 24 – 10 – 2 = 12
- b
  - k = 4 => v = 2^10/2^2 = 2^8 => d = 8
  - Tag = 24 – 8 – 2 = 14
- c
  - Tag = 24 – 2 = 22

Exercise 2

- Design memory system with a cache L1 having size 8KB. Assuming that memory access uses SRAM chip 16M x 32 and each cache line has 1 word. CPU reads/writes 2 bytes for each access.
- a). Using direct-mapped cache
- b). Using 4-way set associative cache
- c). Using fully associative cache

Exercise 2

- a
  - 8KB cache = 2^13 bytes, block size= 2^1 half-words , 16MB x 32 = 2^24 words
  - => w = 1
  - => number of line = 2^13/2^2 =>r =11
  - Tag = 25 – 11 – 1 = 13
- b
  - k = 4 => v = 2^11/2^2 = 2^9 => d = 9
  - Tag = 25 – 9 – 1 = 15
- c
  - Tag = 25 – 1 = 24



Exercise 3

- Assuming the design by using direct-mapped cache is above. Initially, the cache is empty and the write scheme is write-through. Show what happens if CPU accesses data as following addresses
- a). (read) 0x0000A1A, (read) 0x0001A1A
- b). (write) 0x0101B1B, (write) 0x0001A1A
- c). (read) 0x0101B1B, (read) 0x0102B1B

Exercise 3

- 0x0000A1A = 00000 0000 0000 101 0000 1101 0
- a
  - …
- b
  - …
- c
  - …

Exercise 4

- For a direct-mapped cache design with 32-bit address, the following bits of address are used to access the cache
- 32-10(tag)| 9-4 (index) | 3-0 (offset)
- Starting from power on, the following byte-addressed cache references are recorded
- 0 4 16 132 232 160 1024 30 140 3100 180 2180
- How many blocks are replaced ?
- What is the hit ratio ?

Exercise 5

- Assume that main memory accesses take 70ns and that memory accesses are 36% of all instructions. The system memory uses an L1 data cache with miss rate 11.4%. CPU's clock rate is 1.61GHz
- Assuming a base CPI of 1.0. Calculate the total CPI?
- If we add an L2 cache with local miss rate 98%, hit time 3.22ns, what is the total CPI in this case?

Exercise 5

- 1.61GHz ~ 0.62ns
- Memory access cycles = 70/0.62 = 113
- CPI = 1 + 0.36*0.114 *113

- CPI = 1 + 0.36*(0.114*3.22/0.63+0.114*0.98*113)