System_Design

Created	@November 14, 2024 8:55 PM
Tags	VLSI

WDT

What is a watchdog timer (WDT)? – ABLIC Inc.

看門狗計時器 - 維基百科，自由的百科全書

CDC

1. Master slave Latch (the theory how to reserve the data)

2. **Clock domain crossing (Figure 1)**
   * A clk signal(A data) transfer to B clk signal(A data)
   * Need to check (A data) in B clk is "stable"
   *"Unstable" is a *probability of events*

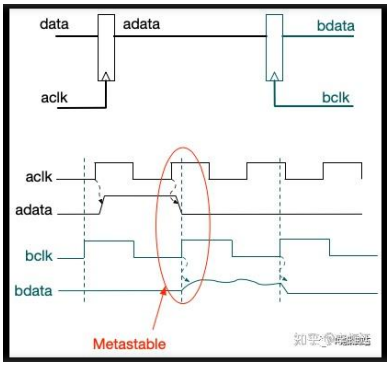


Figure 1

3. **Single bit level (add a flop) (Figure 2)**
   ***have some constraint**

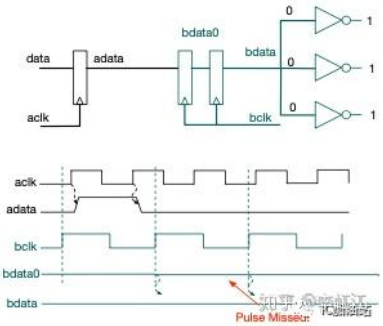
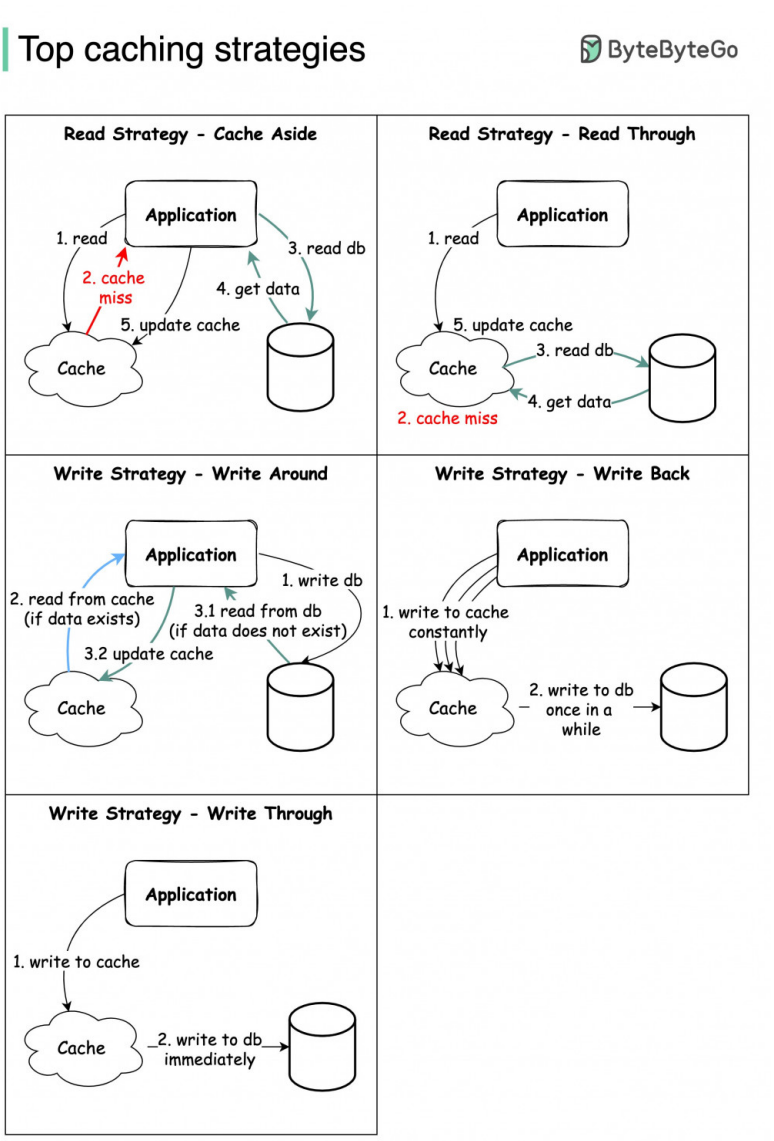


Figure 2

Multiple bit

Cache



https://hackmd.io/@derek8955/H1jlRjbZi

跟老李一起学习芯片设计-- CDC的那些事（1） - 知乎

《補充》 — 5 Classic Caching Strategies - iT 邦幫忙::一起幫忙解決難題，拯救 IT 人的一天

什麼是快取 (Cache)？快取 (Cache) 的機制為何？｜ExplainThis

IO Pad的選擇 | 皓宇的筆記

https://zhuanlan.zhihu.com/p/22681019

https://ithelp.ithome.com.tw/m/articles/10308633

Systemverilog interface/modport 簡介＆使用方法 | Hayashi's Blog