Feasibility Tests

Summary of Results

Test	Rate Monotonic		Dynamic Priority
	Completion Test Feasibility	Scheduling Point Feasibility	EDF Feasibility
0			
1			
2			
3			
4			
5			
6			
6 - DM			
7			
8			
9			

Code Output

```
zturner@jetson-nano:~/projects/rtes/e2$ ./feasibility_tests
Ex-0 U=0.733333 ({S0: C0=1, T0=2, D0=2};   {S1: C1=1, T1=10, D1=10};   {S2: C2=2, T2=15, D2=15})
Completion Test Feasibility: FEASIBLE
Scheduling Point Feasibility: FEASIBLE
EDF Feasibility: FEASIBLE

Ex-1 U=0.985714 ({S0: C0=1, T0=2, D0=2};   {S1: C1=1, T1=5, D1=5};   {S2: C2=2, T2=7, D2=7})
Completion Test Feasibility: INFEASIBLE
Scheduling Point Feasibility: INFEASIBLE
EDF Feasibility: FEASIBLE

Ex-2 U=0.996703 ({S0: C0=1, T0=2, D0=2};   {S1: C1=1, T1=5, D1=5};   {S2: C2=1, T2=7, D2=7};   {S3: C3=2, T3=13, D3=13})
Completion Test Feasibility: INFEASIBLE
Scheduling Point Feasibility: INFEASIBLE
EDF Feasibility: FEASIBLE

Ex-3 U=0.933333 ({S0: C0=1, T0=3, D0=3};   {S1: C1=2, T1=5, D1=5};   {S2: C2=3, T2=15, D2=15})
Completion Test Feasibility: FEASIBLE
Scheduling Point Feasibility: FEASIBLE
EDF Feasibility: FEASIBLE

Ex-4 U=1.000000 ({S0: C0=1, T0=2, D0=2};   {S1: C1=1, T1=4, D1=4};   {S2: C2=4, T2=16, D2=16})
Completion Test Feasibility: FEASIBLE
Scheduling Point Feasibility: FEASIBLE
EDF Feasibility: FEASIBLE

Ex-5 U=1.000000 ({S0: C0=1, T0=2, D0=2};   {S1: C1=2, T1=5, D1=5};   {S2: C2=1, T2=10, D2=10})
Completion Test Feasibility: FEASIBLE
Scheduling Point Feasibility: FEASIBLE
EDF Feasibility: FEASIBLE

Ex-6 U=0.996703 ({S0: C0=1, T0=2, D0=2};   {S1: C1=1, T1=5, D1=5};   {S2: C2=1, T2=7, D2=7};   {S3: C3=2, T3=13, D3=13})
Completion Test Feasibility: INFEASIBLE
Scheduling Point Feasibility: INFEASIBLE
EDF Feasibility: FEASIBLE

Ex-7 U=1.000000 ({S0: C0=1, T0=3, D0=3};   {S1: C1=2, T1=5, D1=5};   {S2: C2=4, T2=15, D2=15})
Completion Test Feasibility: FEASIBLE
Scheduling Point Feasibility: FEASIBLE
EDF Feasibility: FEASIBLE

Ex-8 U=0.996703 ({S0: C0=1, T0=2, D0=2};   {S1: C1=1, T1=5, D1=5};   {S2: C2=1, T2=7, D2=7};   {S3: C3=2, T3=13, D3=13})
Completion Test Feasibility: INFEASIBLE
Scheduling Point Feasibility: INFEASIBLE
EDF Feasibility: FEASIBLE

Ex-9 U=1.000000 ({S0: C0=1, T0=6, D0=6};   {S1: C1=2, T1=8, D1=8};   {S2: C2=4, T2=12, D2=12};   {S3: C3=6, T3=24, D3=24})
Completion Test Feasibility: FEASIBLE
Scheduling Point Feasibility: FEASIBLE
EDF Feasibility: FEASIBLE

Ex-6 DM U=0.992857 ({S0: C0=1, T0=2, D0=2};   {S1: C1=1, T1=5, D1=4};   {S2: C2=1, T2=7, D2=7};   {S3: C3=2, T3=13, D3=20})
Completion Test Feasibility: FEASIBLE
Scheduling Point Feasibility: INFEASIBLE
Dynamic Priority Feasibility: INFEASIBLE
```

```
Ex-0 U=0.733333 ({S0: C0=1, T0=2, D0=2};   {S1: C1=1, T1=10, D1=10};   {S2: C2=2, T2=15, D2=15})
RM LUB = 0.779763
RM LUB Test Feasibility: FEASIBLE
Completion Test Feasibility: FEASIBLE
Scheduling Point Feasibility: FEASIBLE
EDF Feasibility: FEASIBLE

Ex-1 U=0.985714 ({S0: C0=1, T0=2, D0=2};   {S1: C1=1, T1=5, D1=5};   {S2: C2=2, T2=7, D2=7})
RM LUB = 0.779763
RM LUB Test Feasibility: INFEASIBLE
Completion Test Feasibility: INFEASIBLE
Scheduling Point Feasibility: INFEASIBLE
EDF Feasibility: FEASIBLE

Ex-2 U=0.996703 ({S0: C0=1, T0=2, D0=2};   {S1: C1=1, T1=5, D1=5};   {S2: C2=1, T2=7, D2=7};   {S3: C3=2, T3=13, D3=13})
RM LUB = 0.756828
RM LUB Test Feasibility: INFEASIBLE
Completion Test Feasibility: INFEASIBLE
Scheduling Point Feasibility: INFEASIBLE
EDF Feasibility: FEASIBLE

Ex-3 U=0.933333 ({S0: C0=1, T0=3, D0=3};   {S1: C1=2, T1=5, D1=5};   {S2: C2=3, T2=15, D2=15})
RM LUB = 0.779763
RM LUB Test Feasibility: INFEASIBLE
Completion Test Feasibility: FEASIBLE
Scheduling Point Feasibility: FEASIBLE
EDF Feasibility: FEASIBLE

Ex-4 U=1.000000 ({S0: C0=1, T0=2, D0=2};   {S1: C1=1, T1=4, D1=4};   {S2: C2=4, T2=16, D2=16})
RM LUB = 0.779763
RM LUB Test Feasibility: INFEASIBLE
Completion Test Feasibility: FEASIBLE
Scheduling Point Feasibility: FEASIBLE
EDF Feasibility: FEASIBLE

Ex-5 U=1.000000 ({S0: C0=1, T0=2, D0=2};   {S1: C1=2, T1=5, D1=5};   {S2: C2=1, T2=10, D2=10})
RM LUB = 0.779763
RM LUB Test Feasibility: INFEASIBLE
Completion Test Feasibility: FEASIBLE
Scheduling Point Feasibility: FEASIBLE
EDF Feasibility: FEASIBLE
```

```
Ex-6 U=0.996703 ({S0: C0=1, T0=2, D0=2};   {S1: C1=1, T1=5, D1=5};   {S2: C2=1, T2=7, D2=7};   {S3: C3=2, T3=13, D3=13})
RM LUB = 0.756828
RM LUB Test Feasibility: INFEASIBLE
Completion Test Feasibility: INFEASIBLE
Scheduling Point Feasibility: INFEASIBLE
EDF Feasibility: FEASIBLE

Ex-7 U=1.000000 ({S0: C0=1, T0=3, D0=3};   {S1: C1=2, T1=5, D1=5};   {S2: C2=4, T2=15, D2=15})
RM LUB = 0.779763
RM LUB Test Feasibility: INFEASIBLE
Completion Test Feasibility: FEASIBLE
Scheduling Point Feasibility: FEASIBLE
EDF Feasibility: FEASIBLE

Ex-8 U=0.996703 ({S0: C0=1, T0=2, D0=2};   {S1: C1=1, T1=5, D1=5};   {S2: C2=1, T2=7, D2=7};   {S3: C3=2, T3=13, D3=13})
RM LUB = 0.756828
RM LUB Test Feasibility: INFEASIBLE
Completion Test Feasibility: INFEASIBLE
Scheduling Point Feasibility: INFEASIBLE
EDF Feasibility: FEASIBLE

Ex-9 U=1.000000 ({S0: C0=1, T0=6, D0=6};   {S1: C1=2, T1=8, D1=8};   {S2: C2=4, T2=12, D2=12};   {S3: C3=6, T3=24, D3=24})
RM LUB = 0.756828
RM LUB Test Feasibility: INFEASIBLE
Completion Test Feasibility: FEASIBLE
Scheduling Point Feasibility: FEASIBLE
EDF Feasibility: FEASIBLE

Ex-6 DM U=0.992857 ({S0: C0=1, T0=2, D0=2};   {S1: C1=1, T1=5, D1=4};   {S2: C2=1, T2=7, D2=7};   {S3: C3=2, T3=13, D3=20})
Completion Test Feasibility: FEASIBLE
Scheduling Point Feasibility: INFEASIBLE
Dynamic Priority Feasibility: INFEASIBLE
```

Earliest Deadline First Feasibility Test

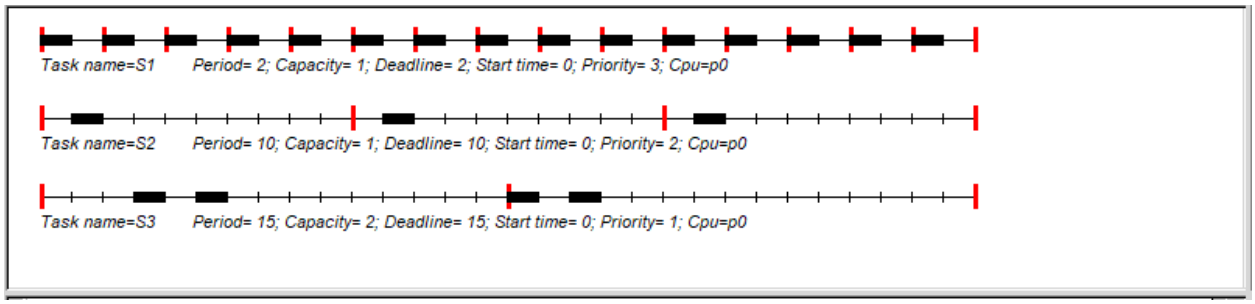
The feasibility test that was used for Earliest Deadline First scheduling was taken from the paper *Preemptive and Non-Preemptive Real-Time UniProcessor Scheduling* [1].

[1] Laurent George, Nicolas Rivierre, Marco Spuri. Preemptive and Non-Preemptive Real-Time UniProcessor Scheduling. [Research Report] RR-2966, INRIA. 1996. ffinria-00073732

Example-0

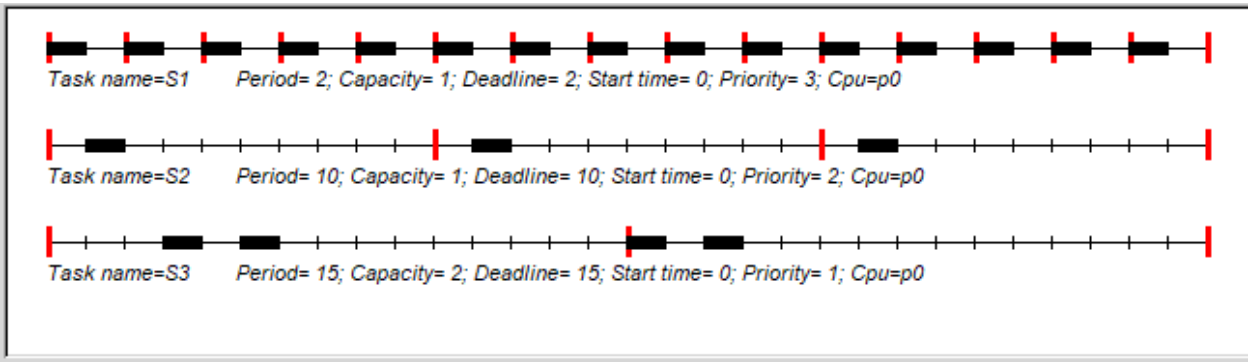
Rate Monotonic

```
Scheduling feasibility, Processor p0 :
1) Feasibility test based on the processor utilization factor :

- The base period is 30 (see [18], page 5).
- 8 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.73333 (see [1], page 6).
- Processor utilization factor with period is 0.73333 (see [1], page 6).
- In the preemptive case, with RM, the task set is schedulable because the processor
utilization factor 0.73333 is equal or less than 0.77976 (see [1], page 16, theorem 8).


2) Feasibility  test based on worst case task response time :

- Bound on task response time :  (see [2], page 3, equation 4).
    S3 => 6
    S2 => 2
    S1 => 1
- All task deadlines will be met : the task set is schedulable.
```



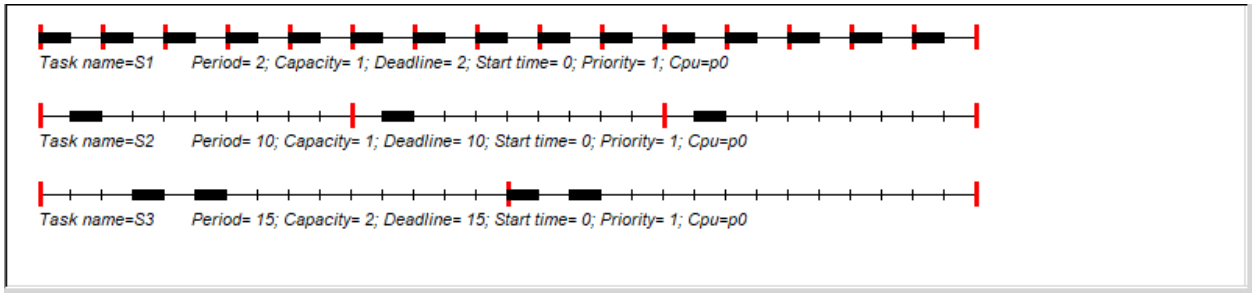
Earliest Deadline First

```
Scheduling feasibility, Processor p0 :
1) Feasibility test based on the processor utilization factor :

- The base period is 30 (see [18], page 5).
- 8 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.73333 (see [1], page 6).
- Processor utilization factor with period is 0.73333 (see [1], page 6).
- In the preemptive case, with EDF, the task set is schedulable because the processor
utilization factor 0.73333 is equal or less than 1.00000 (see [1], page 8, theorem 2).


2) Feasibility  test based on worst case task response time :

- Bound on task response time :
    S1 => 1
    S2 => 8
    S3 => 13
- All task deadlines will be met : the task set is schedulable.
```



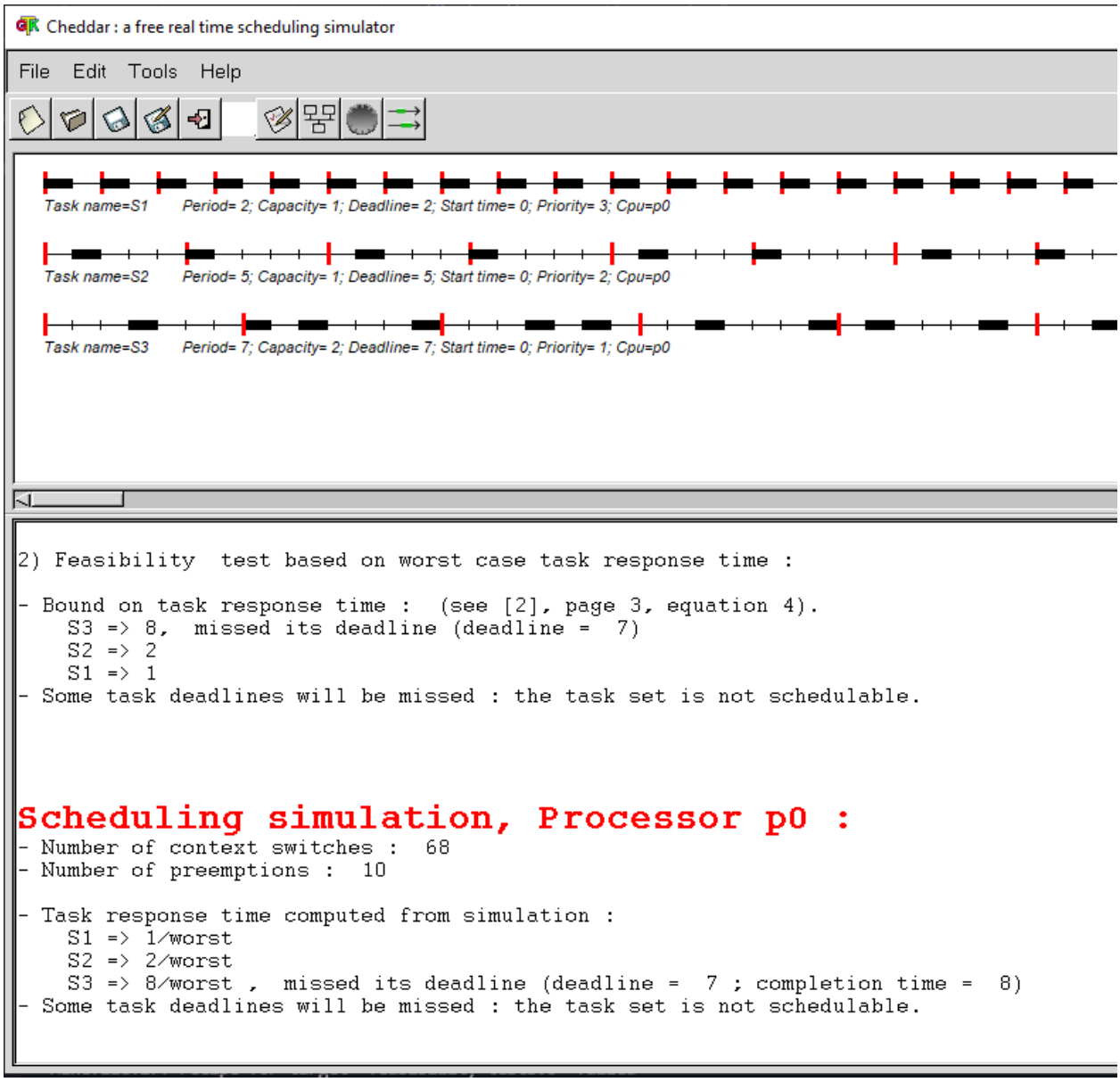
Least Laxity First

```
Scheduling feasibility, Processor p0 :
1) Feasibility test based on the processor utilization factor :

- The base period is 30 (see [18], page 5).
- 8 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.73333 (see [1], page 6).
- Processor utilization factor with period is 0.73333 (see [1], page 6).
- In the preemptive case, with LLF, the task set is schedulable because the processor
utilization factor 0.73333 is equal or less than 1.00000 (see [7]).

2) Feasibility  test based on worst case task response time :

- Bound on task response time :
    S3 => 13
    S1 => 1
    S2 => 8
- All task deadlines will be met : the task set is schedulable.
```


Task name=S1 Period= 2; Capacity= 1; Deadline= 2; Start time= 0; Priority= 1; Cpu=p0
Task name=S2 Period= 10; Capacity= 1; Deadline= 10; Start time= 0; Priority= 1; Cpu=p0
Task name=S3 Period= 15; Capacity= 2; Deadline= 15; Start time= 0; Priority= 1; Cpu=p0

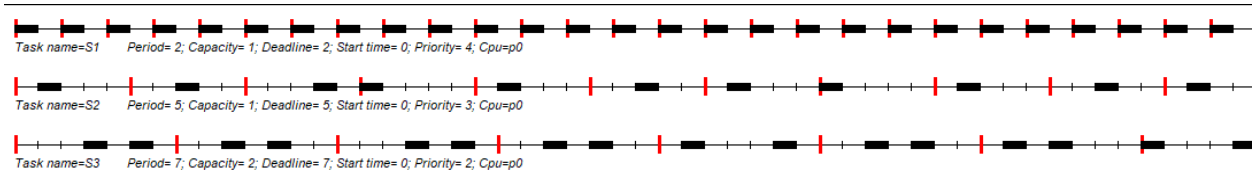
Example 1

Rate Monotonic



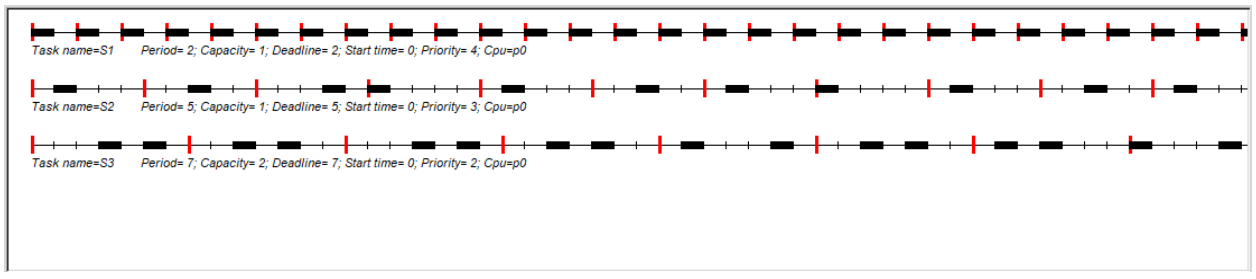
Earliest Deadline First

```
Scheduling feasibility, Processor p0 :
1) Feasibility test based on the processor utilization factor :

- The base period is 70 (see [18], page 5).
- 1 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.98571 (see [1], page 6).
- Processor utilization factor with period is 0.98571 (see [1], page 6).
- In the preemptive case, with EDF, the task set is schedulable because the processor utilization factor 0.98571 is equal
or less than 1.00000 (see [1], page 8, theorem 2).


2) Feasibility  test based on worst case task response time :

- Bound on task response time :
    S1 => 1
    S2 => 4
    S3 => 6
- All task deadlines will be met : the task set is schedulable.
```



Least Laxity First

```
Scheduling feasibility, Processor p0 :
1) Feasibility test based on the processor utilization factor :

- The base period is 70 (see [18], page 5).
- 1 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.98571 (see [1], page 6).
- Processor utilization factor with period is 0.98571 (see [1], page 6).
- In the preemptive case, with LLF, the task set is schedulable because the processor utilization factor 0.98571 is equal
or less than 1.00000 (see [7]).

2) Feasibility  test based on worst case task response time :

- Bound on task response time :
    S1 => 1
    S2 => 4
    S3 => 6
- All task deadlines will be met : the task set is schedulable.
```

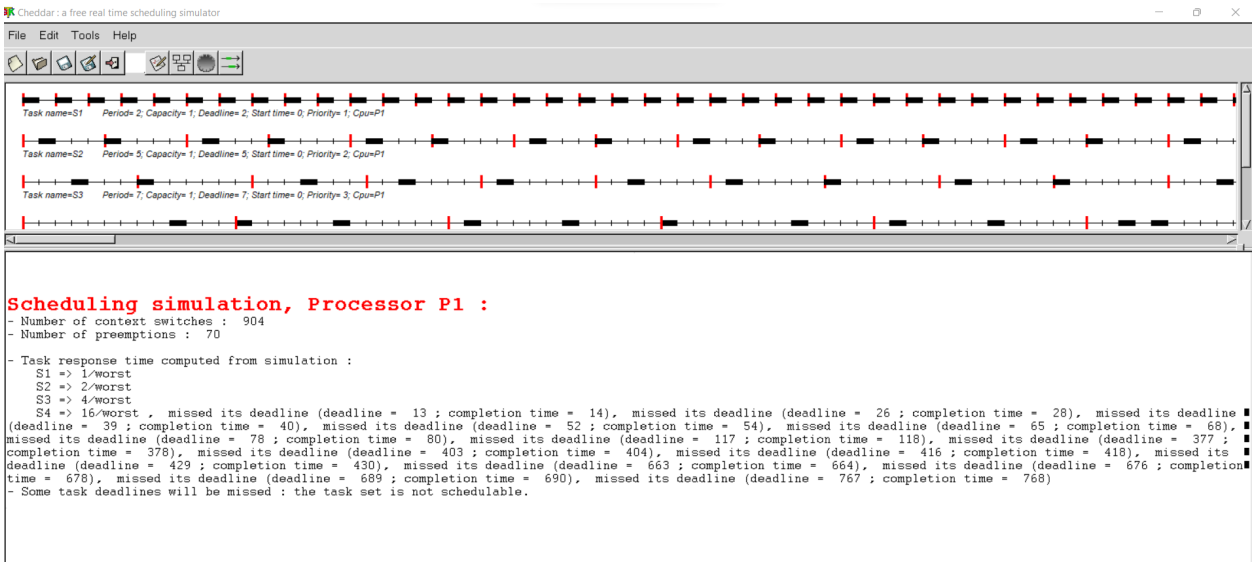


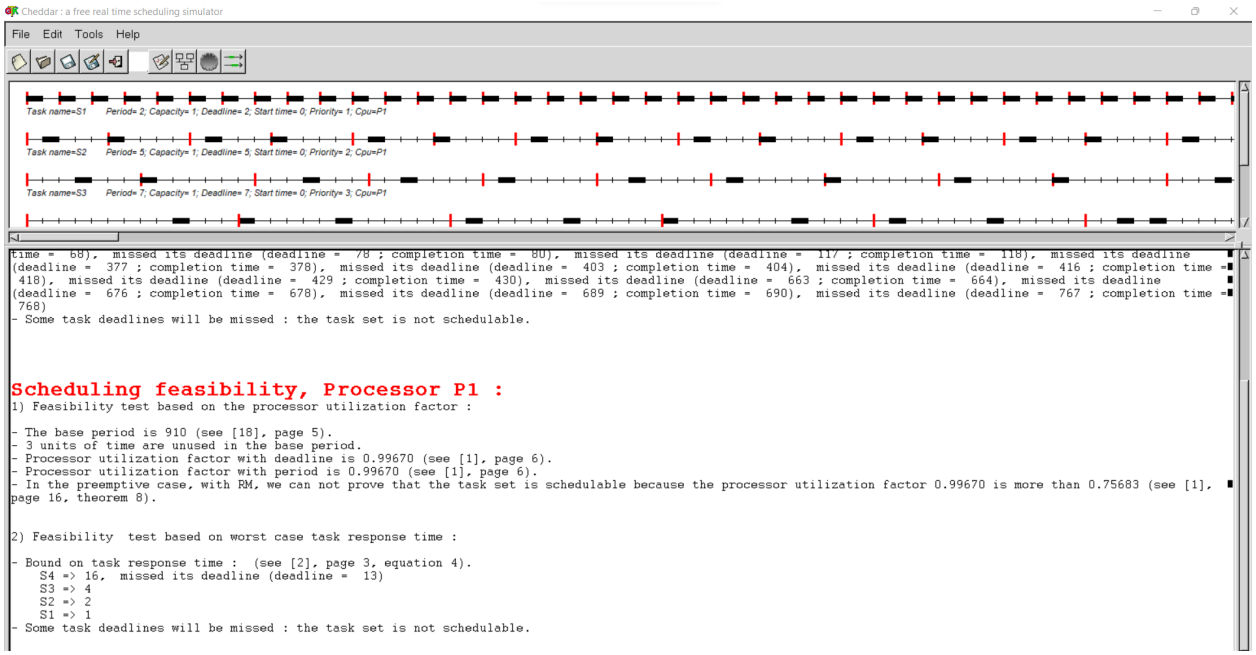
Why RM Fails, but EDF/LLF Passed

- Fixed priority of tasks causes S3 to be starved 6 of its 7 time cycles before the deadline.

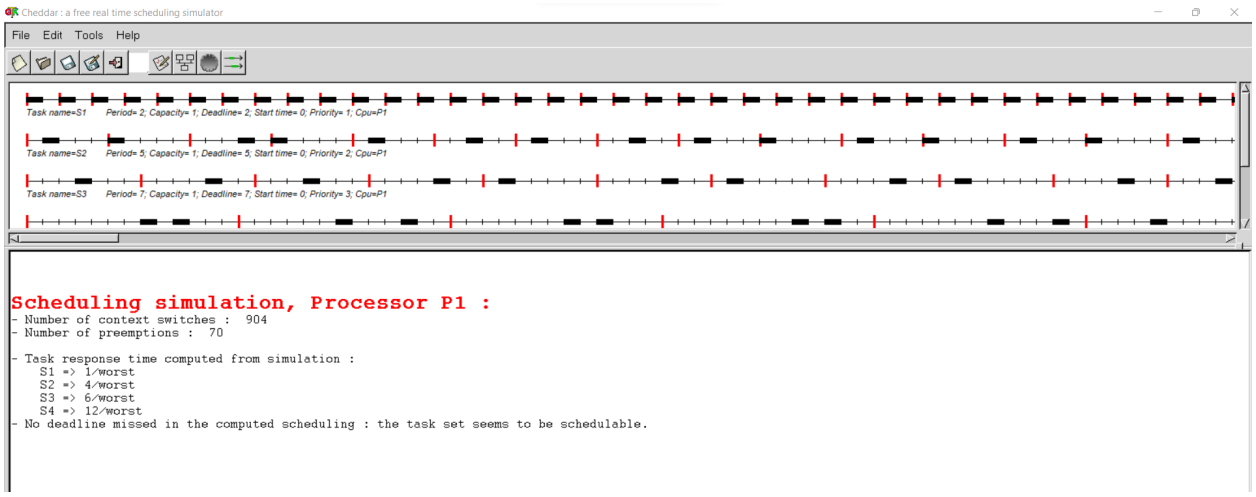
Example 2

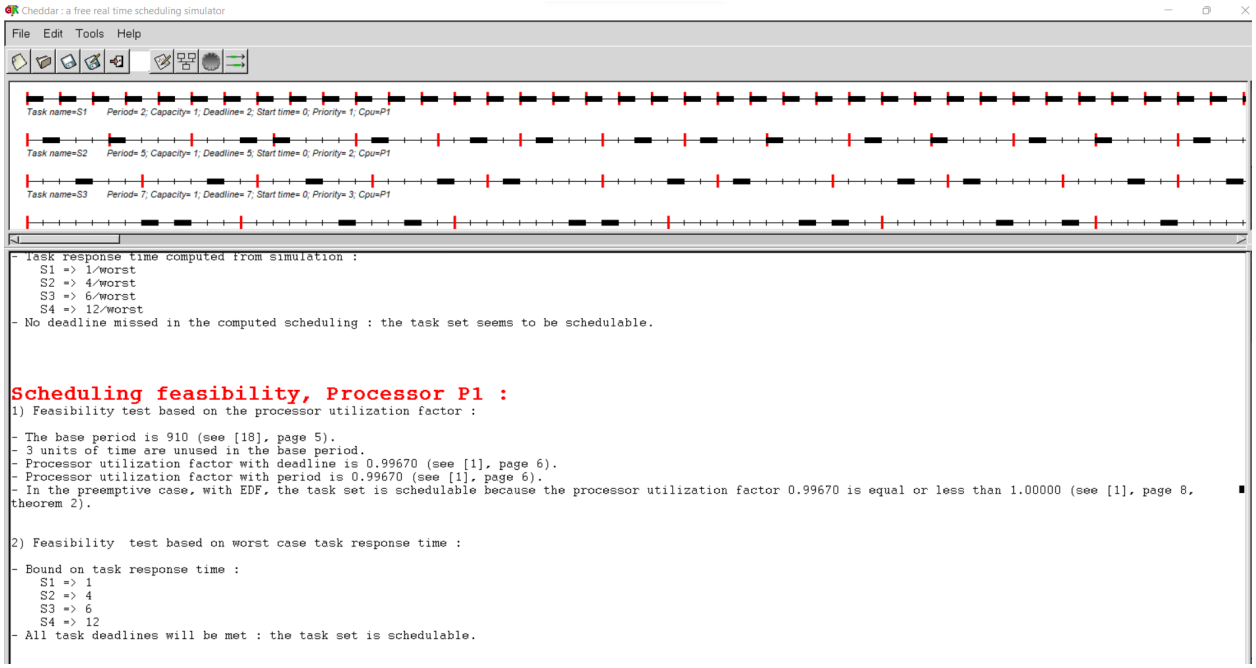
Rate Monotonic



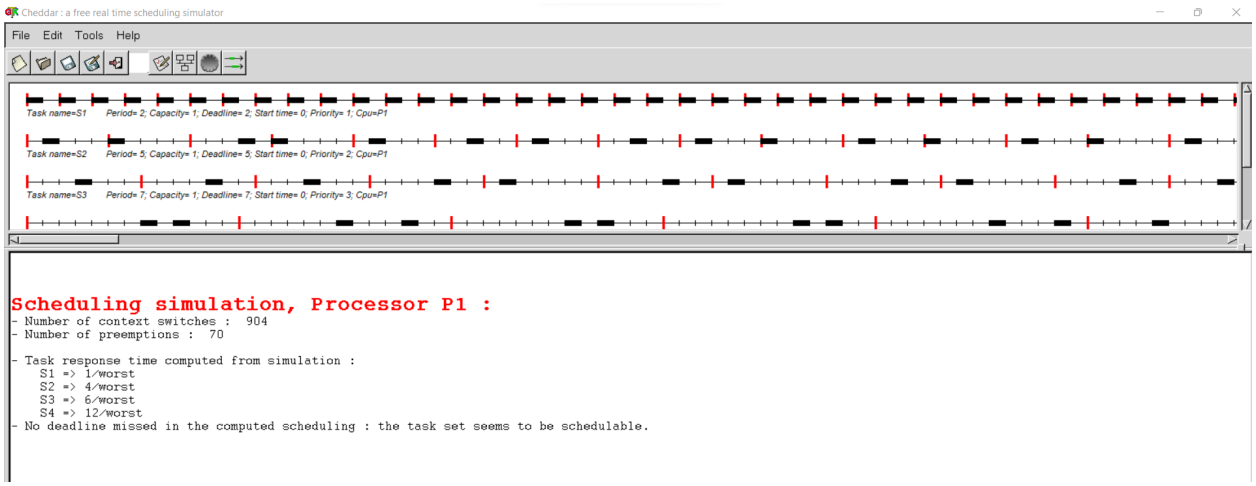


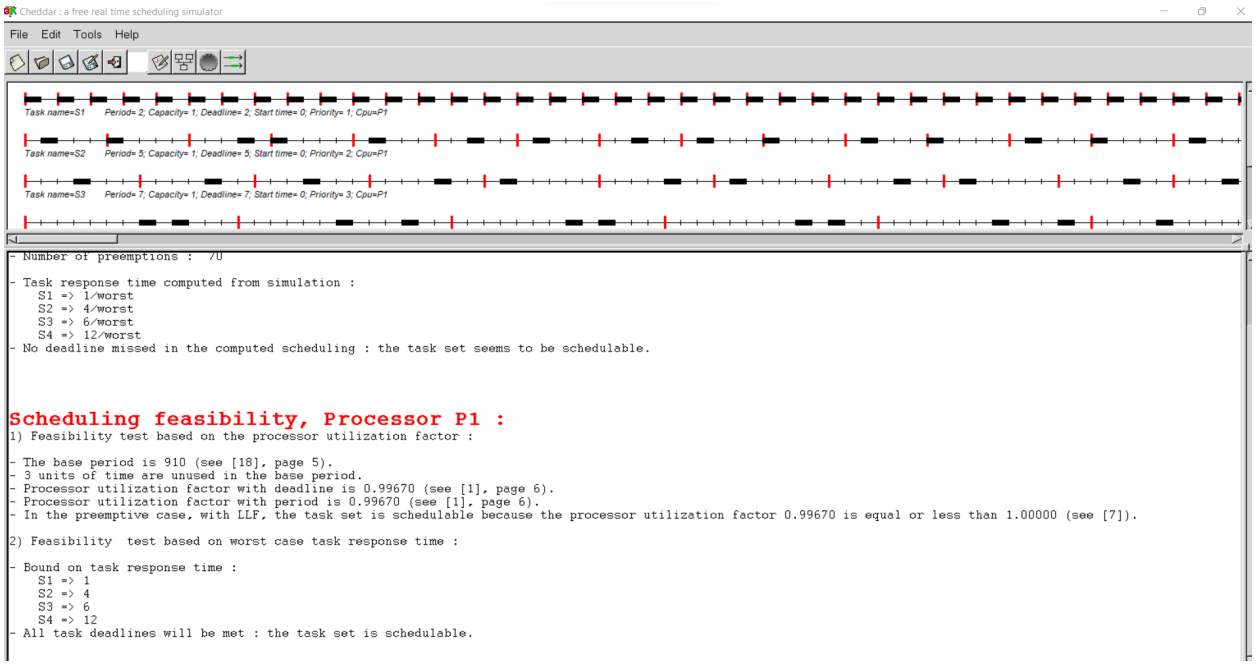
Earliest Deadline First





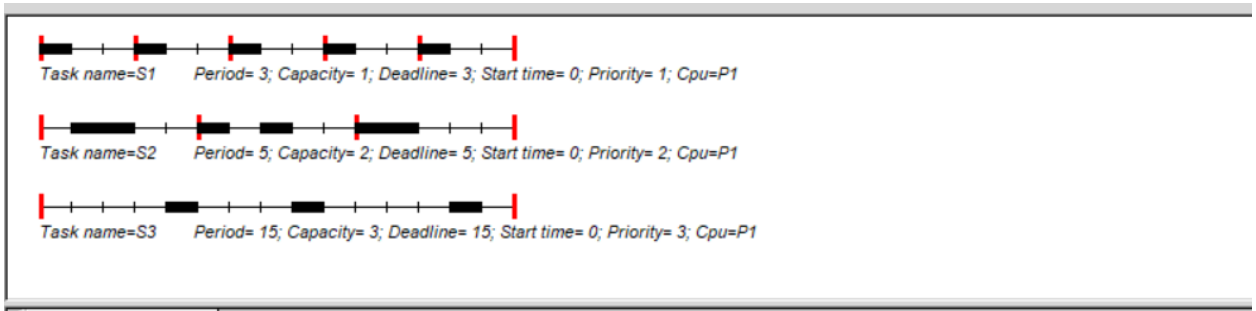
Least Laxity First





Example 3

Rate Monotonic



Scheduling simulation, Processor P1 :

- Number of context switches : 11
- Number of preemptions : 3

- Task response time computed from simulation :
  S1 => 1/worst
  S2 => 3/worst
  S3 => 14/worst
- No deadline missed in the computed scheduling : the task set seems to be schedulable.

Scheduling feasibility, Processor P1 :

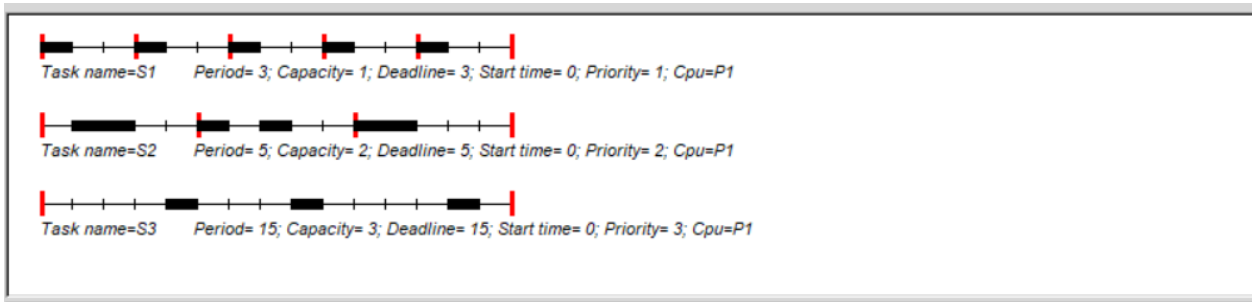
1) Feasibility test based on the processor utilization factor :

- The base period is 15 (see [18], page 5).
- 1 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.93333 (see [1], page 6).
- Processor utilization factor with period is 0.93333 (see [1], page 6).
- In the preemptive case, with RM, we can not prove that the task set is schedulable because the processor utilization factor 0.93333 is more than 0.77976 (see [1], page 16, theorem 8).

2) Feasibility test based on worst case task response time :

- Bound on task response time : (see [2], page 3, equation 4).
  S3 => 14
  S2 => 3
  S1 => 1
- All task deadlines will be met : the task set is schedulable.

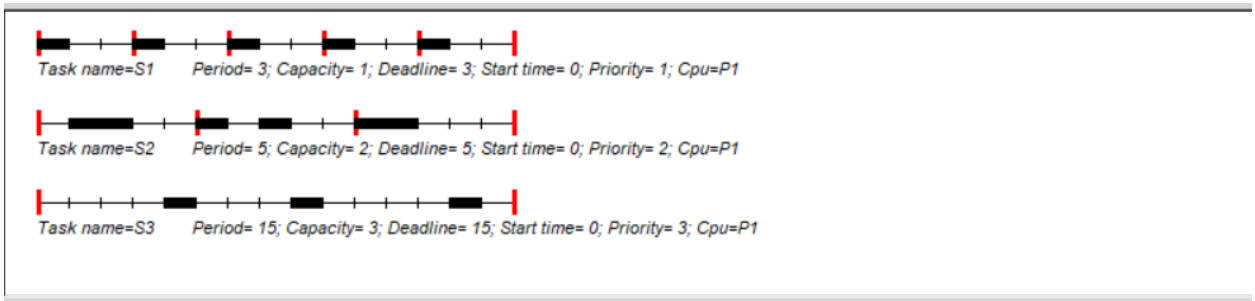
Earliest Deadline First




```
Scheduling simulation, Processor P1 :
- Number of context switches :  11
- Number of preemptions :  3

- Task response time computed from simulation :
    S1 => 1/worst
    S2 => 3/worst
    S3 => 14/worst
- No deadline missed in the computed scheduling : the task set seems to be schedulable.
```


```
- Number of preemptions :  3

- Task response time computed from simulation :
    S1 => 1/worst
    S2 => 3/worst
    S3 => 14/worst
- No deadline missed in the computed scheduling : the task set seems to be schedulable.


Scheduling feasibility, Processor P1 :
1) Feasibility test based on the processor utilization factor :

- The base period is 15 (see [18], page 5).
- 1 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.93333 (see [1], page 6).
- Processor utilization factor with period is 0.93333 (see [1], page 6).
- In the preemptive case, with EDF, the task set is schedulable because the processor utilization factor 0.93333 is equal or less than 1.00000 (see [1], page 8,
theorem 2).


2) Feasibility  test based on worst case task response time :

- Bound on task response time :
    S1 => 2
    S2 => 4
    S3 => 14
- All task deadlines will be met : the task set is schedulable.
```

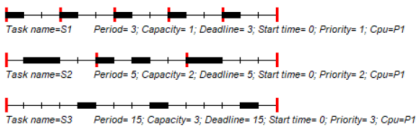
Least Laxity First



Scheduling simulation, Processor P1 :

- Number of context switches : 11
- Number of preemptions : 3

- Task response time computed from simulation :
  S1 => 1/worst
  S2 => 3/worst
  S3 => 14/worst
- No deadline missed in the computed scheduling : the task set seems to be schedulable.



- Number of context switches : 11
- Number of preemptions : 3

- Task response time computed from simulation :
  S1 => 1/worst
  S2 => 3/worst
  S3 => 14/worst
- No deadline missed in the computed scheduling : the task set seems to be schedulable.

Scheduling feasibility, Processor P1 :

1) Feasibility test based on the processor utilization factor :

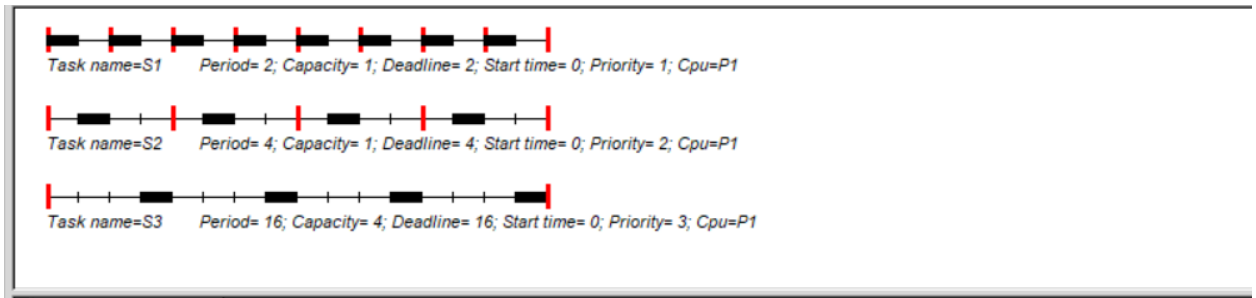
- The base period is 15 (see [18], page 5).
- 1 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.93333 (see [1], page 6).
- Processor utilization factor with period is 0.93333 (see [1], page 6).
- In the preemptive case, with LLF, the task set is schedulable because the processor utilization factor 0.93333 is equal or less than 1.00000 (see [7]).

2) Feasibility test based on worst case task response time :

- Bound on task response time :
  S1 => 2
  S2 => 4
  S3 => 14
- All task deadlines will be met : the task set is schedulable.

Example 4

Rate Monotonic



Scheduling simulation, Processor P1 :

- Number of context switches : 15
- Number of preemptions : 3

- Task response time computed from simulation :
  S1 => 1/worst
  S2 => 2/worst
  S3 => 16/worst
- No deadline missed in the computed scheduling : the task set seems to be schedulable.

- Number of context switches : 15
- Number of preemptions : 3

- Task response time computed from simulation :
  S1 => 1/worst
  S2 => 2/worst
  S3 => 16/worst
- No deadline missed in the computed scheduling : the task set seems to be schedulable.

Scheduling feasibility, Processor P1 :

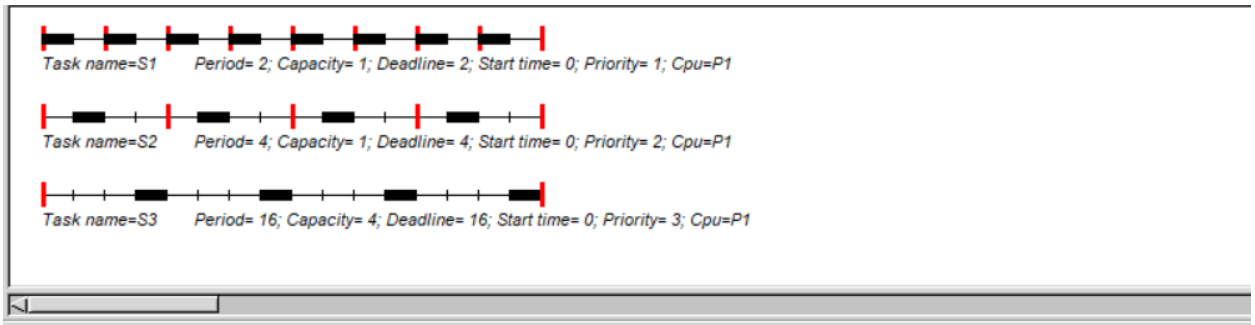
1) Feasibility test based on the processor utilization factor :

- The base period is 16 (see [18], page 5).
- 0 units of time are unused in the base period.
- Processor utilization factor with deadline is 1.00000 (see [1], page 6).
- Processor utilization factor with period is 1.00000 (see [1], page 6).
- In the preemptive case, with RM, the task set is schedulable because the processor utilization factor 1.00000 is equal or less than 1.00000 (see [19], page 13).

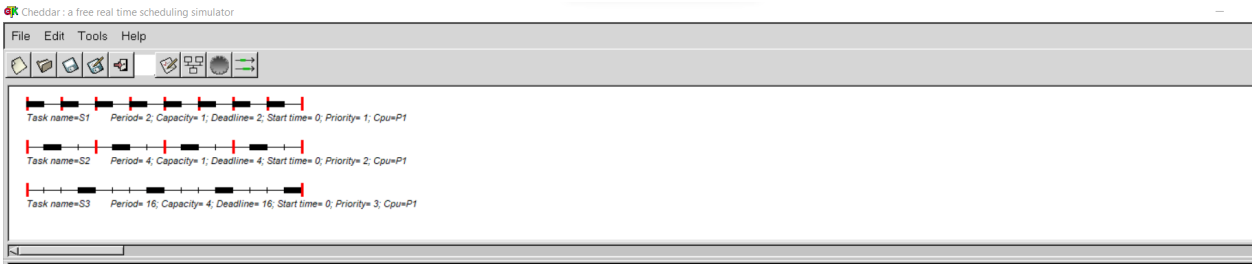
2) Feasibility test based on worst case task response time :

- Bound on task response time : (see [2], page 3, equation 4).
  S3 => 16
  S2 => 2
  S1 => 1
- All task deadlines will be met : the task set is schedulable.

Earliest Deadline First

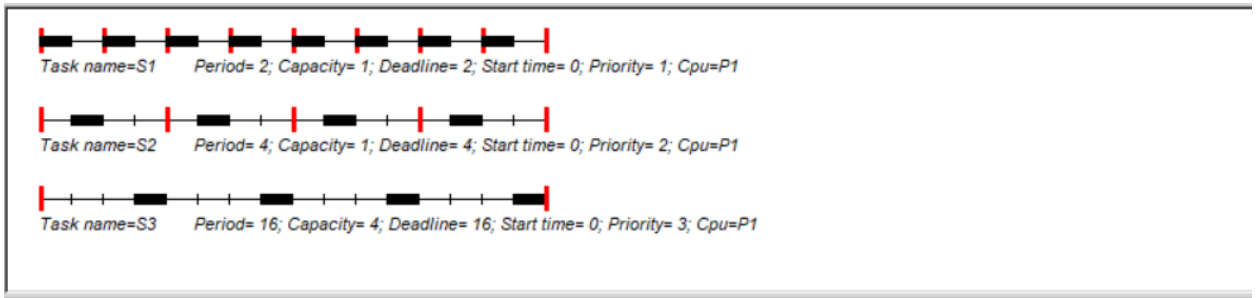



```
Scheduling simulation, Processor P1 :
- Number of context switches :  15
- Number of preemptions :  3

- Task response time computed from simulation :
    S1 => 1/worst
    S2 => 2/worst
    S3 => 16/worst
- No deadline missed in the computed scheduling : the task set seems to be schedulable.
```




```
- Number of preemptions :  3

- Task response time computed from simulation :
    S1 => 1/worst
    S2 => 2/worst
    S3 => 16/worst
- No deadline missed in the computed scheduling : the task set seems to be schedulable.



Scheduling feasibility, Processor P1 :
1) Feasibility test based on the processor utilization factor :

- The base period is 16 (see [18], page 5).
- 0 units of time are unused in the base period.
- Processor utilization factor with deadline is 1.00000 (see [1], page 6).
- Processor utilization factor with period is 1.00000 (see [1], page 6).
- In the preemptive case, with EDF, the task set is schedulable because the processor utilization factor 1.00000 is equal or less than 1.00000 (see [1], page 8,
theorem 2).


2) Feasibility  test based on worst case task response time :

- Bound on task response time :
    S1 => 2
    S2 => 4
    S3 => 16
- All task deadlines will be met : the task set is schedulable.
```

Least Laxity First



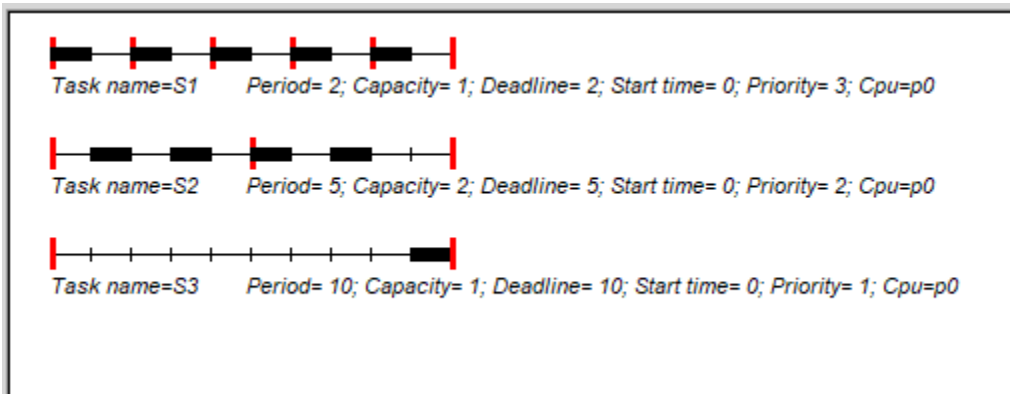

```
Scheduling simulation, Processor P1 :
- Number of context switches :  15
- Number of preemptions :  3

- Task response time computed from simulation :
    S1 => 1/worst
    S2 => 2/worst
    S3 => 16/worst
- No deadline missed in the computed scheduling : the task set seems to be schedulable.
```


```
- Number of context switches :  15
- Number of preemptions :  3

- Task response time computed from simulation :
    S1 => 1/worst
    S2 => 2/worst
    S3 => 16/worst
- No deadline missed in the computed scheduling : the task set seems to be schedulable.


Scheduling feasibility, Processor P1 :
1) Feasibility test based on the processor utilization factor :

- The base period is 16 (see [18], page 5).
- 0 units of time are unused in the base period.
- Processor utilization factor with deadline is 1.00000 (see [1], page 6).
- Processor utilization factor with period is 1.00000 (see [1], page 6).
- In the preemptive case, with LLF, the task set is schedulable because the processor utilization factor 1.00000 is equal or less than 1.00000 (see [7]).

2) Feasibility  test based on worst case task response time :

- Bound on task response time :
    S1 => 2
    S2 => 4
    S3 => 16
- All task deadlines will be met : the task set is schedulable.
```

Example 5

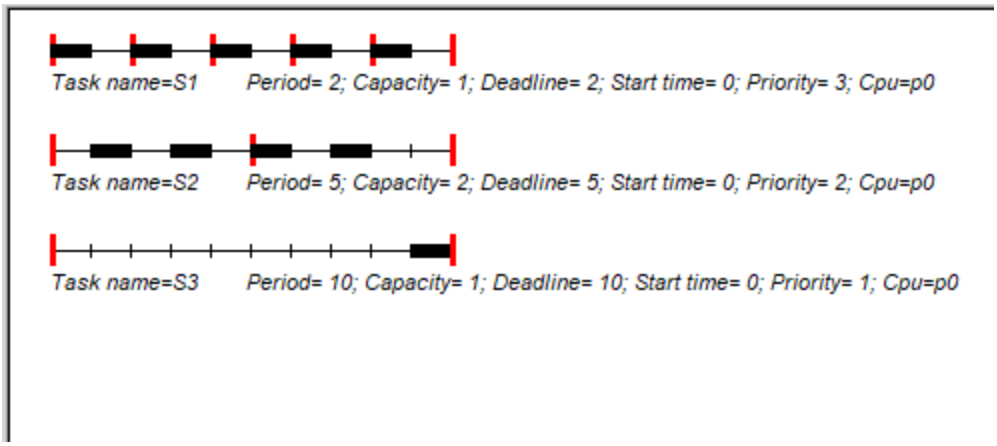
Rate Monotonic

```
Scheduling feasibility, Processor p0 :
1) Feasibility test based on the processor utilization factor :

- The base period is 10 (see [18], page 5).
- 0 units of time are unused in the base period.
- Processor utilization factor with deadline is 1.00000 (see [1], page 6).
- Processor utilization factor with period is 1.00000 (see [1], page 6).
- In the preemptive case, with RM, we can not prove that the task set is schedulable because the processor utilization
factor 1.00000 is more than 0.77976 (see [1], page 16, theorem 8).


2) Feasibility  test based on worst case task response time :

- Bound on task response time :  (see [2], page 3, equation 4).
    S3 => 10
    S2 => 4
    S1 => 1
- All task deadlines will be met : the task set is schedulable.
```

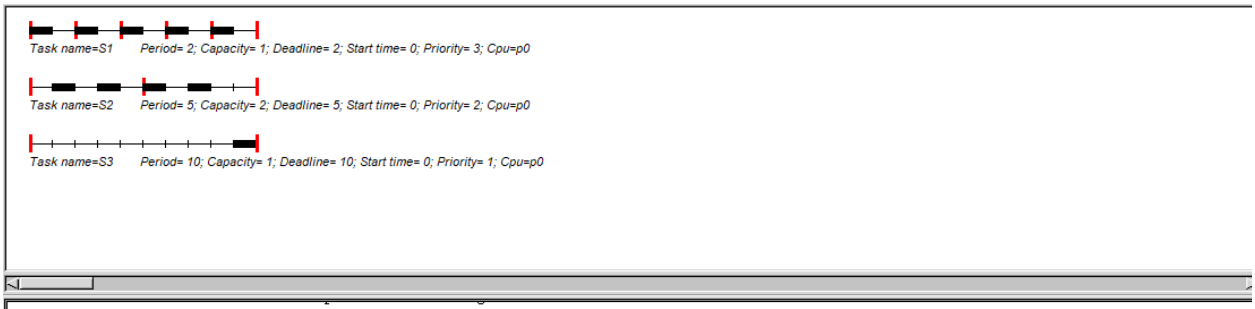


Earliest Deadline First

```
Scheduling feasibility, Processor p0 :
1) Feasibility test based on the processor utilization factor :

- The base period is 10 (see [18], page 5).
- 0 units of time are unused in the base period.
- Processor utilization factor with deadline is 1.00000 (see [1], page 6).
- Processor utilization factor with period is 1.00000 (see [1], page 6).
- In the preemptive case, with EDF, the task set is schedulable because the processor utilization factor 1.00000 is equal
or less than 1.00000 (see [1], page 8, theorem 2).


2) Feasibility  test based on worst case task response time :

- Bound on task response time :
    S1 => 2
    S2 => 5
    S3 => 10
- All task deadlines will be met : the task set is schedulable.
```



Least Laxity First



Scheduling feasibility, Processor p0 :

```
1) Feasibility test based on the processor utilization factor :

- The base period is 10 (see [18], page 5).
- 0 units of time are unused in the base period.
- Processor utilization factor with deadline is 1.00000 (see [1], page 6).
- Processor utilization factor with period is 1.00000 (see [1], page 6).
- In the preemptive case, with LLF, the task set is schedulable because the processor utilization factor 1.00000 is equal
or less than 1.00000 (see [7]).

2) Feasibility  test based on worst case task response time :

- Bound on task response time :
    S1 => 2
    S2 => 5
    S3 => 10
- All task deadlines will be met : the task set is schedulable.
```

Example 6

Rate Monotonic

```
Scheduling feasibility, Processor p0 :
1) Feasibility test based on the processor utilization factor :

- The base period is 910 (see [18], page 5).
- 3 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.99670 (see [1], page 6).
- Processor utilization factor with period is 0.99670 (see [1], page 6).
- In the preemptive case, with RM, we can not prove that the task set is schedulable
because the processor utilization factor 0.99670 is more than 0.75683 (see [1], page
16, theorem 8).


2) Feasibility  test based on worst case task response time :

- Bound on task response time :  (see [2], page 3, equation 4).
    S4 => 16,  missed its deadline (deadline =  13)
    S3 => 4
    S2 => 2
    S1 => 1
- Some task deadlines will be missed : the task set is not schedulable.
```

Earliest Deadline First

```
Scheduling feasibility, Processor p0 :
1) Feasibility test based on the processor utilization factor :

- The base period is 910 (see [18], page 5).
- 3 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.99670 (see [1], page 6).
- Processor utilization factor with period is 0.99670 (see [1], page 6).
- In the preemptive case, with EDF, the task set is schedulable because the processor utilization factor 0.99670 is equal
or less than 1.00000 (see [1], page 8, theorem 2).


2) Feasibility  test based on worst case task response time :

- Bound on task response time :
    S1 => 1
    S2 => 4
    S3 => 6
    S4 => 12
- All task deadlines will be met : the task set is schedulable.
```

Least Laxity First

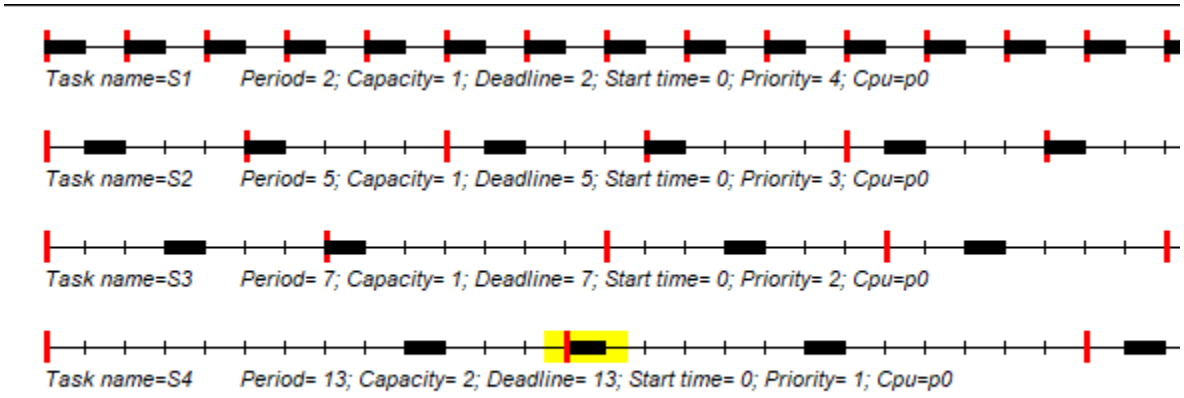
```
Scheduling feasibility, Processor p0 :
1) Feasibility test based on the processor utilization factor :

- The base period is 910 (see [18], page 5).
- 3 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.99670 (see [1], page 6).
- Processor utilization factor with period is 0.99670 (see [1], page 6).
- In the preemptive case, with LLF, the task set is schedulable because the processor utilization factor 0.99670 is equal
or less than 1.00000 (see [7]).

2) Feasibility  test based on worst case task response time :

- Bound on task response time :
    S1 => 1
    S2 => 4
    S3 => 6
    S4 => 12
- All task deadlines will be met : the task set is schedulable.
```

Deadline Monotonic

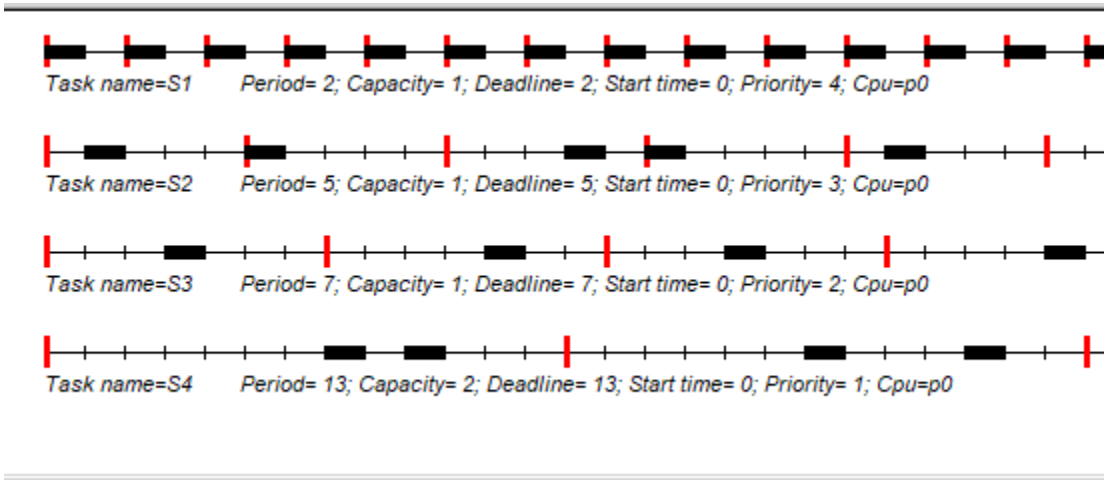
```
Scheduling feasibility, Processor p0 :
1) Feasibility test based on the processor utilization factor :

- The base period is 910 (see [18], page 5).
- 3 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.99286 (see [1], page 6).
- Processor utilization factor with period is 0.99670 (see [1], page 6).
- In the preemptive case, with DM, the task set is not schedulable because the processor utilization factor 0.99286 is more
than 0.75683 (see [7]).

2) Feasibility  test based on worst case task response time :

- Bound on task response time :  (see [2], page 3, equation 4).
    S4 => 16
    S3 => 4
    S2 => 2
    S1 => 1
- All task deadlines will be met : the task set is schedulable.
```

Reason why RM failed, but LLF/EDF Passed

Rate Monotonic:



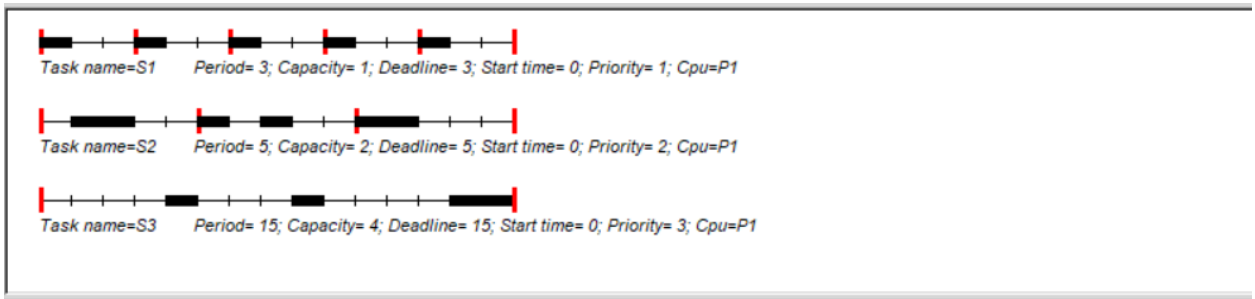
Earliest Deadline First:



- In Rate Monotonic, higher frequency tasks take priority. With S1 having a period of 2 time units, that leaves every other time unit for the remaining three tasks
- For S4, a period of 13 time units but only 6 available to it because of the priority of S1
- Before S4's deadline, there are 5 new periods of execution between S2 and S3, leaving only 1 available for S4. However, since S4 has a capacity of 2, it will fail to schedule this.
- EDF solves this by prioritizing the deadline of the first period of S4 over the new periods of S2 and S3

Example 7

Rate Monotonic



Scheduling simulation, Processor P1 :

- Number of context switches : 11
- Number of preemptions : 3

- Task response time computed from simulation :
  - S1 => 1/worst
  - S2 => 3/worst
  - S3 => 15/worst
- No deadline missed in the computed scheduling : the task set seems to be schedulable.

Scheduling feasibility, Processor P1 :

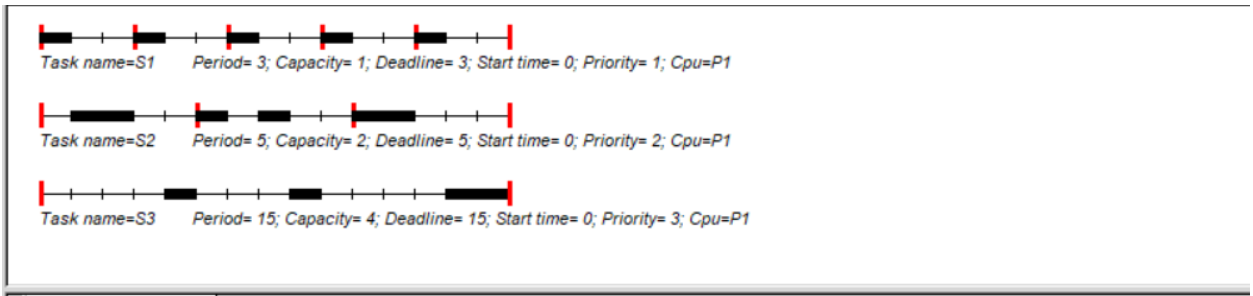
1) Feasibility test based on the processor utilization factor :

- The base period is 15 (see [18], page 5).
- 0 units of time are unused in the base period.
- Processor utilization factor with deadline is 1.00000 (see [1], page 6).
- Processor utilization factor with period is 1.00000 (see [1], page 6).
- In the preemptive case, with RM, we can not prove that the task set is schedulable because the processor utilization factor 1.00000 is more than 0.77976 (see [1], page 16, theorem 8).

2) Feasibility test based on worst case task response time :

- Bound on task response time : (see [2], page 3, equation 4).
  - S3 => 15
  - S2 => 3
  - S1 => 1
- All task deadlines will be met : the task set is schedulable.

Earliest Deadline First



Scheduling simulation, Processor P1 :

- Number of context switches : 11
- Number of preemptions : 3

- Task response time computed from simulation :
  - S1 => 1/worst
  - S2 => 3/worst
  - S3 => 15/worst
- No deadline missed in the computed scheduling : the task set seems to be schedulable.

Scheduling feasibility, Processor P1 :

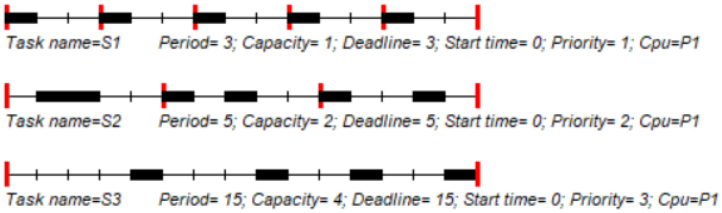
1) Feasibility test based on the processor utilization factor :

- The base period is 15 (see [18], page 5).
- 0 units of time are unused in the base period.
- Processor utilization factor with deadline is 1.00000 (see [1], page 6).
- Processor utilization factor with period is 1.00000 (see [1], page 6).
- In the preemptive case, with EDF, the task set is schedulable because the processor utilization factor 1.00000 is equal or less than 1.00000 (see [1], page 8, theorem 2).

2) Feasibility test based on worst case task response time :

- Bound on task response time :
  - S1 => 3
  - S2 => 5
  - S3 => 15
- All task deadlines will be met : the task set is schedulable.

Least Laxity First



Scheduling simulation, Processor P1 :

- Number of context switches : 13
- Number of preemptions : 5

- Task response time computed from simulation :
  - S1 => 1/worst
  - S2 => 4/worst
  - S3 => 15/worst
- No deadline missed in the computed scheduling : the task set seems to be schedulable.

Scheduling feasibility, Processor P1 :

1) Feasibility test based on the processor utilization factor :

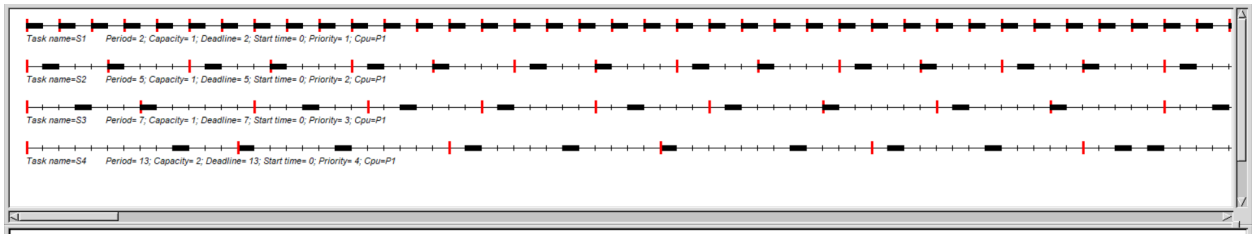
- The base period is 15 (see [18], page 5).
- 0 units of time are unused in the base period.
- Processor utilization factor with deadline is 1.00000 (see [1], page 6).
- Processor utilization factor with period is 1.00000 (see [1], page 6).
- In the preemptive case, with LLF, the task set is schedulable because the processor utilization factor 1.00000 is equal or less than 1.00000 (see [7]).

2) Feasibility test based on worst case task response time :

- Bound on task response time :
  - S1 => 3
  - S2 => 5
  - S3 => 15
- All task deadlines will be met : the task set is schedulable.

Example 8

Rate Monotonic



Scheduling simulation, Processor P1 :

- Number of context switches : 904
- Number of preemptions : 70

- Task response time computed from simulation :
  S1 => 1/worst
  S2 => 2/worst
  S3 => 4/worst
  S4 => 16/worst , missed its deadline (deadline = 13 ; completion time = 14), missed its deadline (deadline = 26 ; completion time = 28), missed its deadline (deadline = 39 ; completion time = 40), missed its deadline (deadline = 52 ; completion time = 54), missed its deadline (deadline = 65 ; completion time = 68), missed its deadline (deadline = 78 ; completion time = 80), missed its deadline (deadline = 117 ; completion time = 118), missed its deadline (deadline = 377 ; completion time = 378), missed its deadline (deadline = 403 ; completion time = 404), missed its deadline (deadline = 416 ; completion time = 418), missed its deadline (deadline = 429 ; completion time = 430), missed its deadline (deadline = 663 ; completion time = 664), missed its deadline (deadline = 676 ; completion time = 678), missed its deadline (deadline = 689 ; completion time = 690), missed its deadline (deadline = 767 ; completion time = 768)
- Some task deadlines will be missed : the task set is not schedulable.

Scheduling feasibility, Processor P1 :

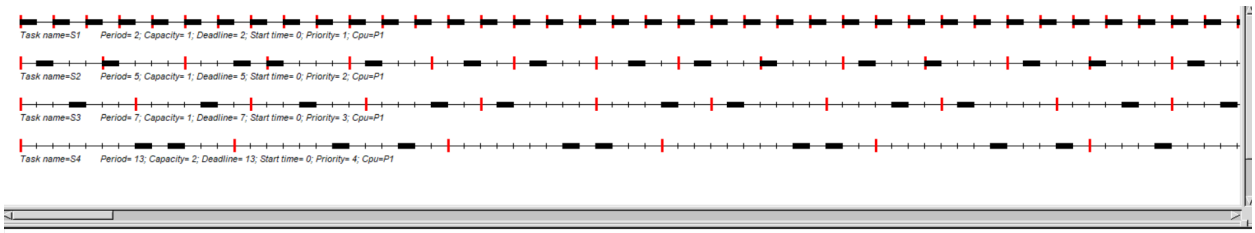
1) Feasibility test based on the processor utilization factor :

- The base period is 910 (see [18], page 5).
- 3 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.99670 (see [1], page 6).
- Processor utilization factor with period is 0.99670 (see [1], page 6).
- In the preemptive case, with RM, we can not prove that the task set is schedulable because the processor utilization factor 0.99670 is more than 0.75683 (see [1], page 16, theorem 8).

2) Feasibility test based on worst case task response time :

- Bound on task response time : (see [2], page 3, equation 4).
  S4 => 16, missed its deadline (deadline = 13)
  S3 => 4
  S2 => 2
  S1 => 1
- Some task deadlines will be missed : the task set is not schedulable.

Earliest Deadline First



Scheduling simulation, Processor P1 :

- Number of context switches : 904
- Number of preemptions : 70

- Task response time computed from simulation :
  S1 => 1/worst
  S2 => 4/worst
  S3 => 6/worst
  S4 => 12/worst
- No deadline missed in the computed scheduling : the task set seems to be schedulable.

Scheduling feasibility, Processor P1 :

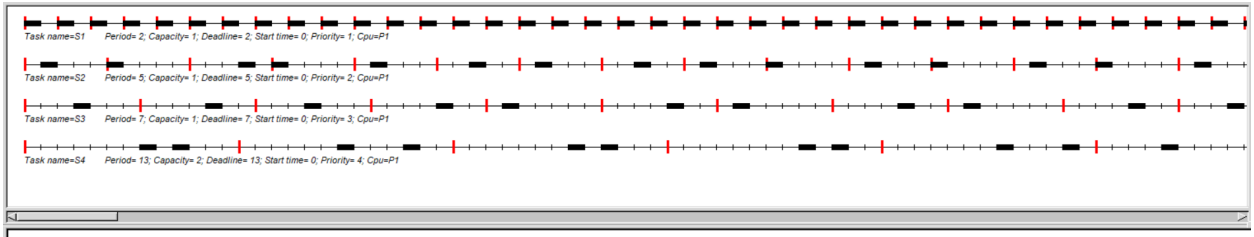
1) Feasibility test based on the processor utilization factor :

- The base period is 910 (see [18], page 5).
- 3 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.99670 (see [1], page 6).
- Processor utilization factor with period is 0.99670 (see [1], page 6).
- In the preemptive case, with EDF, the task set is schedulable because the processor utilization factor 0.99670 is equal or less than 1.00000 (see [1], page 8, theorem 2).

2) Feasibility test based on worst case task response time :

- Bound on task response time :
  - S1 => 1
  - S2 => 4
  - S3 => 6
  - S4 => 12
- All task deadlines will be met : the task set is schedulable.

Least Laxity First



Scheduling simulation, Processor P1 :

- Number of context switches : 904
- Number of preemptions : 70

- Task response time computed from simulation :
  - S1 => 1/worst
  - S2 => 4/worst
  - S3 => 6/worst
  - S4 => 12/worst
- No deadline missed in the computed scheduling : the task set seems to be schedulable.

Scheduling feasibility, Processor P1 :

1) Feasibility test based on the processor utilization factor :

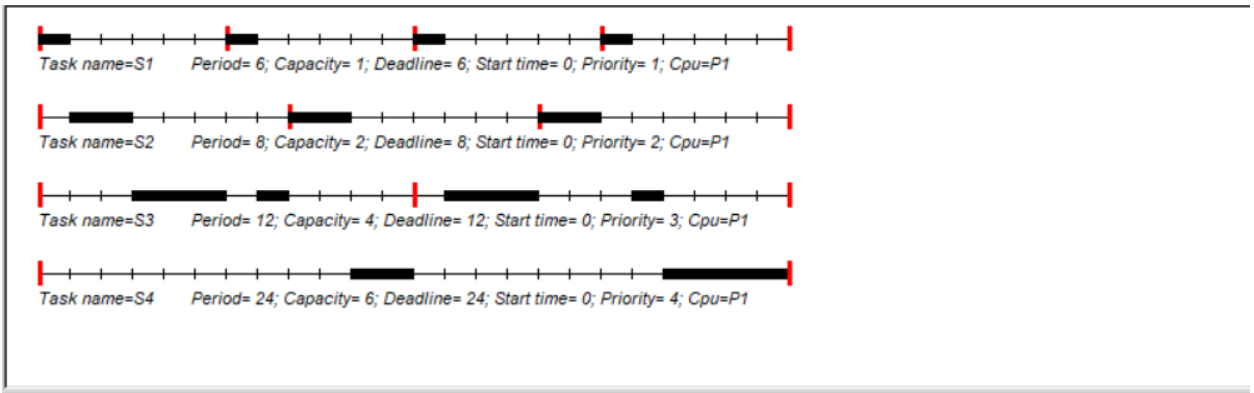
- The base period is 910 (see [18], page 5).
- 3 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.99670 (see [1], page 6).
- Processor utilization factor with period is 0.99670 (see [1], page 6).
- In the preemptive case, with LLF, the task set is schedulable because the processor utilization factor 0.99670 is equal or less than 1.00000 (see [7]).

2) Feasibility test based on worst case task response time :

- Bound on task response time :
  - S1 => 1
  - S2 => 4
  - S3 => 6
  - S4 => 12
- All task deadlines will be met : the task set is schedulable.

Example 9

Rate Monotonic



Scheduling simulation, Processor P1 :

- Number of context switches : 12
- Number of preemptions : 3

- Task response time computed from simulation :
  - S1 => 1/worst
  - S2 => 3/worst
  - S3 => 8/worst
  - S4 => 24/worst
- No deadline missed in the computed scheduling : the task set seems to be schedulable.

Scheduling feasibility, Processor P1 :

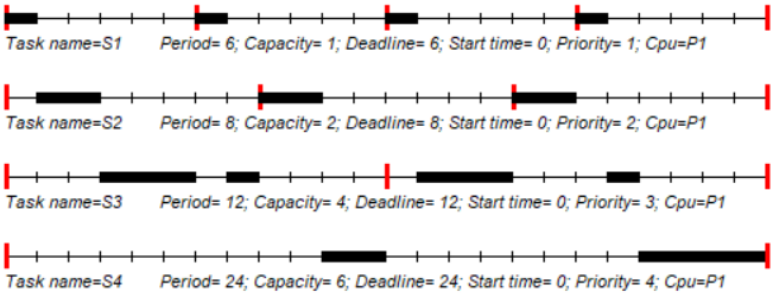
1) Feasibility test based on the processor utilization factor :

- The base period is 24 (see [18], page 5).
- 0 units of time are unused in the base period.
- Processor utilization factor with deadline is 1.00000 (see [1], page 6).
- Processor utilization factor with period is 1.00000 (see [1], page 6).
- In the preemptive case, with RM, we can not prove that the task set is schedulable because the processor utilization factor 1.00000 is more than 0.75683 (see [1], page 16, theorem 8).

2) Feasibility test based on worst case task response time :

- Bound on task response time : (see [2], page 3, equation 4).
  - S4 => 24
  - S3 => 8
  - S2 => 3
  - S1 => 1
- All task deadlines will be met : the task set is schedulable.

Earliest Deadline First



Scheduling simulation, Processor P1 :

- Number of context switches : 12
- Number of preemptions : 3

- Task response time computed from simulation :
  S1 => 1/worst
  S2 => 3/worst
  S3 => 8/worst
  S4 => 24/worst
- No deadline missed in the computed scheduling : the task set seems to be schedulable.

Scheduling feasibility, Processor P1 :

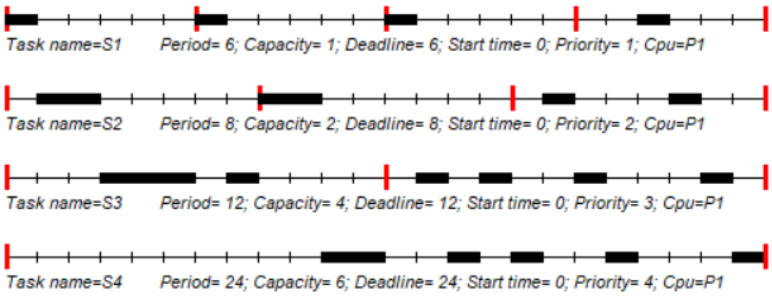
1) Feasibility test based on the processor utilization factor :

- The base period is 24 (see [18], page 5).
- 0 units of time are unused in the base period.
- Processor utilization factor with deadline is 1.00000 (see [1], page 6).
- Processor utilization factor with period is 1.00000 (see [1], page 6).
- In the preemptive case, with EDF, the task set is schedulable because the processor utilization factor 1.00000 is equal or less than 1.00000 (see [1], page 8, theorem 2).

2) Feasibility test based on worst case task response time :

- Bound on task response time :
  S1 => 6
  S2 => 8
  S3 => 12
  S4 => 24
- All task deadlines will be met : the task set is schedulable.

Least Laxity First



Scheduling simulation, Processor P1 :

- Number of context switches : 18
- Number of preemptions : 9

- Task response time computed from simulation :
  - S1 => 3/worst
  - S2 => 6/worst
  - S3 => 11/worst
  - S4 => 24/worst
- No deadline missed in the computed scheduling : the task set seems to be schedulable.

Scheduling feasibility, Processor P1 :

1) Feasibility test based on the processor utilization factor :

- The base period is 24 (see [18], page 5).
- 0 units of time are unused in the base period.
- Processor utilization factor with deadline is 1.00000 (see [1], page 6).
- Processor utilization factor with period is 1.00000 (see [1], page 6).
- In the preemptive case, with LLF, the task set is schedulable because the processor utilization factor 1.00000 is equal or less than 1.00000 (see [7]).

2) Feasibility test based on worst case task response time :

- Bound on task response time :
  - S1 => 6
  - S2 => 8
  - S3 => 12
  - S4 => 24
- All task deadlines will be met : the task set is schedulable.