RTES Exercise 2

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Question 1

```
dhiraj@nano:/root$ su dhiraj
Password:
dhiraj@nano:/root$ sudo whoami
root
dhiraj@nano:/root$ su zach
Password:
zach@nano:/root$ sudo whoami
root
zach@nano:/root$
```

An account has been created in the names of both the user Dhiraj and Zach and root privileges are given to both the users

Question 2

Frequency Executive Advantages

- 1. Can maintain 40 millisecond periods through the cyclic executive for the high frequency tasks with higher priority
- 2. Can reliably handle a variety of frequency services by setting appropriate priorities and allowing the scheduler to preempt low-frequency tasks with high-frequency ones.

3. Frequency executive scheduling can provide more deterministic run time which is easier to test and validate with extremely low or no MTBF (mean time between failures). Real-time scheduling is much harder to have the same test coverage and confidence.

Frequency Executive Disadvantages

- Requires well understood, deterministic service release times and core affinity to be able to schedule tasks with varying priorities based on frequency.
- 2. Not a flexible solution if last minute principal functions need to be added or adjusted
- Real-time threading can better handle asynchronous tasks. Frequency
 executives require either a central timekeeper or a polling of asynchronous
 tasks.

Question 3

Cyclic Executive Architecture has the following properties

- 1. The Architecture has predictable outputs and can easily be tested as there is no interleaving of operations
- 2. Code can have smaller footprint
- 3. Code is difficult to maintain through developmental stages
- 4. The architecture will have low abstraction level

The above mentioned points can be overcome by using reusable software components such as abstract data types and generic packages or templates

Key points in the Paper

- (a) Cyclic Schedule is a table which contains a full execution pattern for a major cycle.
- (b) A dynamic recovery policy will be adopted for failure recovery.
- (c) Cyclic Scheduler is iterative procedure that allows the explicit multiplexing of periodic processes set in one processor.

The following parameters should be configurable in the cyclic architecture

- i. Duration of minor and major cycle periods
- ii. Number of minor cycles per major cycle

- iii. Maximum number of frames per minor cycle
- iv. Process (reference to procedure) that has to be executed in each frame $\,$

Differences in Cyclic Executive and Linux Posix threads

Cyclic Executive	Linux RT Threads		
Low Abstraction Level	High Abstraction Level		
Difficult to maintain as	Addition of functionality is		
changes/addition creates	easier		
ripple throughout			
No concept of priority	Priority levels exits		
Pre-Analysis for developing	Can dynamically adapt new		
Architecture is huge	features with less complexity		
Predictable Response	Mostly predictable		
Low footprint and overhead	Footprint is large		
No context switch except for	Context switch for switching		
interrupts	between different priority		
	threads		

Question 4

Summary of Results

Test	Rate Monotonic		Dynamic Priority
	Completion Test Feasibility	Scheduling Point Feasibility	EDF Feasibility
0			
1			
2			
3			
4			
5			
6			
6 - DM			
7			
8			
9			

Code Output

```
turner@jetson-nano:~/projects/rtes/e2$ ./feasibility_tests
x-0 U=0.733333 ({$0: C0=1, T0=2, D0=2}; {$1: C1=1, T1=10, D1=10}; {$2: C2=2, T2=15, D2=15})
ompletion Test Feasibility: FEASIBLE
cheduling Point Feasibility: FEASIBLE
DF Feasibility: FEASIBLE
   x-1 U=0.985714 ({$0: C0=1, T0=2, D0=2}; {$1: C1=1, T1=5, D1=5}; {$2: C2=2, T2=7, D2=7}) cmpletion Test Feasibility: INFEASIBLE Cheduling Point Feasibility: INFEASIBLE DF Feasibility: FEASIBLE
   x-2 U=0.996703 {{$0: C0=1, T0=2, D0=2}; {$1: C1=1, T1=5, D1=5}; {$2: C2=1, T2=7, D2=7}; {$3: C3=2, T3=13, D3=13})
ompletion Test Feasibility: INFEASIBLE
cheduling Point Feasibility: INFEASIBLE
DF Feasibility: FEASIBLE
   x-3 U=0.933333 ({$0: C0=1, T0=3, D0=3}; {$1: C1=2, T1=5, D1=5}; {$2: C2=3, T2=15, D2=15}) ompletion Test Feasibility: FEASIBLE cheduling Point Feasibility: FEASIBLE DF Feasibility: FEASIBLE
  :x-4 U=1.000000 ({S0: C0=1, T0=2, D0=2}; {S1: C1=1, T1=4, D1=4}; {S2: C2=4, T2=16, D2=16})
completion Test Feasibility: FEASIBLE
icheduling Point Feasibility: FEASIBLE
DF Feasibility: FEASIBLE
   x-5 U=1.000000 ({$0: C0=1, T0=2, D0=2}; {$1: C1=2, T1=5, D1=5}; {$2: C2=1, T2=10, D2=10}) ompletion Test Feasibility: FEASIBLE Cheduling Point Feasibility: FEASIBLE DF Feasibility: FEASIBLE
   x-6 U=0.996703 ({$0: C0=1, T0=2, D0=2}; {$1: C1=1, T1=5, D1=5}; {$2: C2=1, T2=7, D2=7}; {$3: C3=2, T3=13, D3=13})
ompletion Test Feasibility: INFEASIBLE
beduing Point Feasibility: INFEASIBLE
DF Feasibility: FEASIBLE
   x-7 U=1.000000 ({$0: C0=1, T0=3, D0=3}; {$1: C1=2, T1=5, D1=5}; {$2: C2=4, T2=15, D2=15}) ompletion Test Feasibility: FEASIBLE cheduling Point Feasibility: FEASIBLE DF Feasibility: FEASIBLE
   x-8 U=0.996703 ({$0: C0=1, T0=2, D0=2}; {$1: C1=1, T1=5, D1=5}; {$2: C2=1, T2=7, D2=7}; {$3: C3=2, T3=13, D3=13}) ompletion Test Feasibility: INFEASIBLE cheduling Point Feasibility: INFEASIBLE DF Feasibility: FEASIBLE
  x-9 U=1.000000 ({$0: C0=1, T0=6, D0=6}; {$1: C1=2, T1=8, D1=8}; {$2: C2=4, T2=12, D2=12}; {$3: C3=6, T3=24, D3=24})
completion Test Feasibility: FEASIBLE
icheduling Point Feasibility: FEASIBLE
DF Feasibility: FEASIBLE
  ex-6 DM U=0.992857 ({$0: C0=1, T0=2, D0=2}; {$1: C1=1, T1=5, D1=4}; {$2: C2=1, T2=7, D2=7}; {$3: C3=2, T3=13, D3=20})
Completion Test Feasibility: FEASTBLE
Scheduling Point Feasibility: INFEASTBLE
Dynamic Priority Feasibility: INFEASTBLE
 Ex-0 U=0.733333 ({S0: C0=1, T0=2, D0=2}; {S1: C1=1, T1=10, D1=10}; {S2: C2=2, T2=15, D2=15})
RM LUB = 0.779763
RM LUB Test Feastbility: FEASIBLE
Completion Test Feastbility: FEASIBLE
Scheduling Point Feastbility: FEASIBLE
EDF Feastbility: FEASIBLE
 Ex-1 U=0.985714 ({SO: C0=1, T0=2, D0=2}; {S1: C1=1, T1=5, D1=5}; {S2: C2=2, T2=7, D2=7})
RM LUB = 0.779763
RM LUB Test Feasibility: INFEASIBLE
Completion Test Feasibility: INFEASIBLE
Scheduling Point Feasibility: INFEASIBLE
EDF Feasibility: FASIBLE
Ex-2 U=0.996703 ({S0: C0=1, T0=2, D0=2}; {S1: C1=1, T1=5, D1=5}; {S2: C2=1, T2=7, D2=7}; {S3: C3=2, T3=13, D3=13})
RM LUB = 0.756820
RM LUB TS1 Feasibility: INFEASIBLE
Completion Test Feasibility: INFEASIBLE
Scheduling Point Feasibility: INFEASIBLE
EDF Feasibility: FEASIBLE
Ex-3 U=0.933333 ({S0: C0=1, T0=3, D0=3}; {S1: C1=2, T1=5, D1=5}; {S2: C2=3, T2=15, D2=15}) RM LUB = 0.779763 RM LUB Test Feasibility: INFEASIBLE Completion Test Feasibility: FEASIBLE Scheduling Point Feasibility: FEASIBLE EDF Feasibility: FEASIBLE
Ex-4 U=1.000000 ({S0: C0=1, T0=2, D0=2}; {S1: C1=1, T1=4, D1=4}; {S2: C2=4, T2=16, D2=16})
RM LUB = 0.779763
RM LUB Test Feasibility: INFEASIBLE
Completion Test Feasibility: FEASIBLE
Scheduling Point Feasibility: FEASIBLE
EDF Feasibility: FEASIBLE
 Ex-5 U=1.000000 ({S0: C0=1, T0=2, D0=2}; {S1: C1=2, T1=5, D1=5}; {S2: C2=1, T2=10, D2=10})
EX-5 U=1.000000 (\S0: C0=1, 10=2, D0=2
RM LUB = 0.779763
RM LUB Test Feasibility: INFEASIBLE
Completion Test Feasibility: FEASIBLE
Scheduling Point Feasibility: FEASIBLE
EDF Feasibility: FEASIBLE
```

```
Ex-6 U=0.996703 ({50: C0=1, T0=2, D0=2}; {51: C1=1, T1=5, D1=5}; {52: C2=1, T2=7, D2=7}; {53: C3=2, T3=13, D3=13})

RM LUB = 0.756828

RM LUB Test Feasibility: INFEASIBLE

EX-7 U=1.000000 ({50: C0=1, T0=3, D0=3}); {51: C1=2, T1=5, D1=5}; {52: C2=4, T2=15, D2=15})

RM LUB Test Feasibility: INFEASIBLE

Completion Test Feasibility: INFEASIBLE

Completion Test Feasibility: INFEASIBLE

EX-8 U=0.996703 ({50: C0=1, T0=2, D0=2}); {51: C1=1, T1=5, D1=5}; {52: C2=4, T2=15, D2=15})

RM LUB Test Feasibility: INFEASIBLE

EX-8 U=0.996703 ({50: C0=1, T0=2, D0=2}); {51: C1=1, T1=5, D1=5}; {52: C2=1, T2=7, D2=7}; {53: C3=2, T3=13, D3=13})

RM LUB Test Feasibility: INFEASIBLE

EX-8 U=0.996703 ({50: C0=1, T0=6, D0=6}); {51: C1=2, T1=8, D1=8}; {52: C2=4, T2=12, D2=12}; {53: C3=6, T3=24, D3=24})

RM LUB Test Feasibility: INFEASIBLE

EX-9 U=1.000000 ({50: C0=1, T0=6, D0=6}); {51: C1=2, T1=8, D1=8}; {52: C2=4, T2=12, D2=12}; {53: C3=6, T3=24, D3=24})

RM LUB Test Feasibility: FASIBLE

EX-9 U=1.000000 ({50: C0=1, T0=6, D0=6}); {51: C1=2, T1=8, D1=8}; {52: C2=4, T2=12, D2=12}; {53: C3=6, T3=24, D3=24})

RM LUB Test Feasibility: FASIBLE

EX-9 U=1.000000 ({50: C0=1, T0=6, D0=6}); {51: C1=2, T1=8, D1=8}; {52: C2=4, T2=12, D2=12}; {53: C3=6, T3=24, D3=24})

RM LUB Test Feasibility: FASIBLE

EX-9 U=1.000000 ({50: C0=1, T0=6, D0=6}); {51: C1=2, T1=8, D1=8}; {52: C2=4, T2=12, D2=12}; {53: C3=6, T3=24, D3=24})

RM LUB Test Feasibility: FASIBLE

Completion Test Feasibility: FASIBLE

EX-6 DM U=0.992857 ({50: C0=1, T0=2, D0=2}); {51: C1=1, T1=5, D1=4}; {52: C2=1, T2=7, D2=7}; {53: C3=2, T3=13, D3=20})

Completion Test Feasibility: FASIBLE

EX-6 DM U=0.992857 ({50: C0=1, T0=2, D0=2}); {51: C1=1, T1=5, D1=4}; {52: C2=1, T2=7, D2=7}; {53: C3=2, T3=13, D3=20})

COMPLETION TEST FEASIBILE

EX-6 DM U=0.992857 ({50: C0=1, T0=2, D0=2}); {51: C1=1, T1=5, D1=4}; {52: C2=1, T2=7, D2=7}; {53: C3=2, T3=13, D3=20})

COMPLETION TEST FEASIBLE
```

Earliest Deadline First Feasibility Test

The feasibility test that was used for Earliest Deadline First scheduling was taken from the paper Preemptive and Non-Preemptive Real-Time UniProcessor Scheduling [1].

The images for each of the tests are arranged in the pdf file available at below location

Question 4 Results

Question 5

Assumptions made in the Paper

- (a) All services are requested on periodic basis, the period is constant
- (b) The completion time of a service is less than its period
- (c) Service Requests are independent (No Known Phasing)
- (d) Runtime is known and deterministic
- (e) Critical Instant Longest service time for a response occurs when all the system services are requested simultaneously (maximum interference case for lowest priority service)

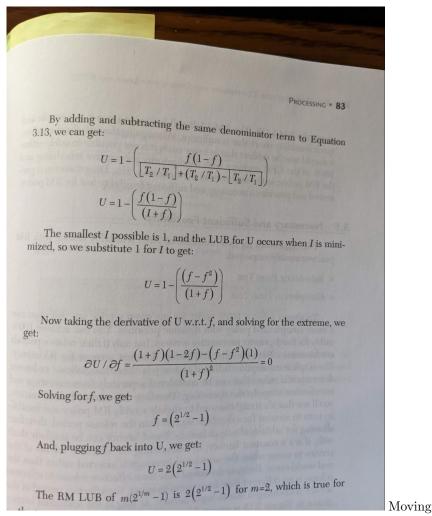
Constraints

- (a) Deadline of a service is equal to the period
- (b) Fixed Priority, Preemptive, Run to Completion Scheduling

- (c) Does not include Secondary, Tertiary Resource Issue
- (d) Fails in cases where Dynamic Priorities succeed

The RM LUB is a pessimistic feasibility test that will fail some proposed service sets that actually work, but it will never pass a set that doesn't work. RM LUB is a sufficient feasibility test but not necessary.

Parts of the paper that contains complicated Math



from 3.12 to 3.13

Rationale: We never would have thought to separate integer interference from fractional interference, but it creates a convenient utility function

$$U = \frac{T_2 - T_1 \left| T_2 / T_1 \right|}{T_1} + \frac{T_2 - C_1 \left| T_2 / T_1 \right|}{T_2}$$

$$U = \frac{T_2 - T_1 \left| T_2 / T_1 \right|}{T_1} + \frac{T_2 - (T_2 - T_1 \left| T_2 / T_1 \right|) \left| T_2 / T_1 \right|}{T_2}$$

$$U = \frac{T_2 - T_1 \left| T_2 / T_1 \right|}{T_1} + \frac{T_2 - T_2 \left| T_2 / T_1 \right| + T_1 \left| T_2 / T_1 \right| \left| T_2 / T_1 \right|}{T_2}$$

$$U = \left(T_2 / T_1 \right) - \left[T_2 / T_1 \right] + \left(T_1 / T_2 \right) \left| T_2 / T_1 \right| + \left(T_1 / T_2 \right) \left| T_2 / T_1 \right| \right|$$

$$U = 1 - \left(T_2 / T_1 \right) + \left(T_1 / T_2 \right) \left| T_2 / T_1 \right| + \left(T_2 / T_1 \right) - \left(T_2 / T_1 \right) \right|$$

$$U = 1 - \left(T_1 / T_2 \right) \left(\left(T_2 / T_1 \right) \right) \left| T_2 / T_1 \right| - \left(T_2 / T_1 \right) \right| - \left(T_2 / T_1 \right) \right|$$

$$U = 1 - \left(T_1 / T_2 \right) \left[\left(T_2 / T_1 \right) - \left(T_2 / T_1 \right) \right] \left[\left(T_2 / T_1 \right) - \left(T_2 / T_1 \right) \right]$$

$$Now, \text{ let whole integer number of interferences of S1 to S2 over T2 be $I = \left[T_2 / T_1 \right] \text{ and the fractional interference of } for utility:$

$$U = 1 - \left(\frac{f(1 - f)}{(T_2 / T_1)} \right) \qquad (3.13)$$
The derivation for Equation 3.11 is based upon substitution of I and f
$$U = 1 - \left(T_1 / T_2 \right) \left[T_2 / T_1 \right] - \left(T_2 / T_1 \right) \left[\left(T_2 / T_1 \right) - \left[T_2 / T_1 \right] \right]$$

$$U = 1 - \left(T_1 / T_2 \right) \left[T_2 / T_1 \right] - \left(T_2 / T_1 \right) \left[\left(T_2 / T_1 \right) - \left[T_2 / T_1 \right] \right]$$

$$U = 1 - \left(T_1 / T_2 \right) \left[T_2 / T_1 \right] - \left(T_2 / T_1 \right) \left[\left(T_2 / T_1 \right) - \left[T_2 / T_1 \right] \right]$$

$$U = 1 - \left(T_1 / T_2 \right) \left[T_2 / T_1 \right] - \left(T_2 / T_1 \right) \right] \left[\left(T_2 / T_1 \right) - \left[T_2 / T_1 \right] \right]$$

$$U = 1 - \left(T_1 / T_2 \right) \left[T_2 / T_1 \right] - \left(T_2 / T_1 \right) \right] \left[\left(T_2 / T_1 \right) - \left[T_2 / T_1 \right] \right]$$

$$U = 1 - \left(T_1 / T_2 \right) \left[T_2 / T_1 \right] - \left(T_2 / T_1 \right) \right] \left[\left(T_2 / T_1 \right) - \left[T_2 / T_1 \right] \right]$$

$$U = 1 - \left(T_1 / T_2 \right) \left[T_2 / T_1 \right] - \left(T_2 / T_1 \right) \right] \left[\left(T_2 / T_1 \right) - \left[T_2 / T_1 \right] \right]$$

$$U = 1 - \left(T_1 / T_2 \right) \left[T_2 / T_1 \right] - \left(T_2 / T_1 \right) \right] \left[\left(T_2 / T_1 \right) - \left[T_2 / T_1 \right] \right]$$

$$U = 1 - \left(T_1 / T_2 \right) \left[T_2 / T_1 \right] - \left(T_2 / T_1 \right) \right] \left[\left(T_2 / T_1 \right) - \left[T_2 / T_1 \right] \right]$$

$$U = 1 - \left(T_1 / T_2 \right) \left[T_1 / T_1 \right] \left[T_2 / T_1 \right] \right] \left[T_2 / T_1 \right] \left[T_2 / T_1 \right] \left[T_2 / T_1 \right] \right]$$

$$U = 1 - \left(T_1 / T_2 \right) \left[$$$$

Adding

and subtracting same value to denominator

Rationale: It's interesting to add more expressions into the derivation so that we can represent the integer interference

Taking the derivative of U w.r.t f and solving for the extreme Rationale: Taking the derivative of U w.r.t f and solving for the extreme

References

- [1] Laurent George, Nicolas Rivierre, Marco Spuri. Preemptive and Non-Preemptive Real-Time UniProcessor Scheduling. [Research Report] RR-2966, INRIA. 1996. ffinria-00073732
- [2] Code Source: http://mercury.pr.erau.edu/ siewerts/cec450/code/ Courtesy: Dr Sam Siewert Professor Tim Scherr