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Class CSE-2

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~~**Exam No.**~~ Sub — DE

Institution CPC

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2.	Realization of logic functions with the help of universal gates - NAND Gate.	9 to 15.	20-8-2020	5-9-2020	

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AIM :-

Realization of logic functions with the help of universal gates – NAND Gate.

Apparatus :- Logic trainer Kit, NAND gates (IC 7400), wires.

THEORY :

NAND gate is actually a combination of two logic gates : AND gate followed by NOT gate. So its output is complement of the output of an AND gate.

This gate can have minimum two input, output is always one. By using only NAND gates, we can realize all logic functions : AND, OR, NOT, X-OR, X-NOR, NOR. So this gate is also called universal gate

NAND gates as NOT gate

A NOT produces complement of the input. It can have only input, tie the inputs of a NAND gate together. Now it will work as a NOT gate. Its output is

$$Y = (A.A)'$$

$$Y = (A)'$$

NAND gates as AND gate

A NAND produces complement of AND gate. So, if the output of a NAND gate is inverted

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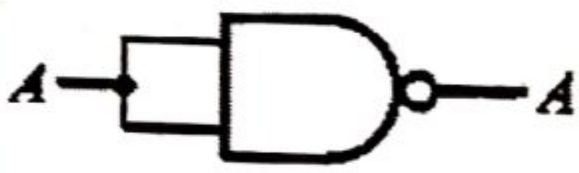
AIM:- Realization of logic functions with the help of universal gates - NAND gates.

NAND gates as NOT gate

2 Input NAND gate		
A	B	$\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0



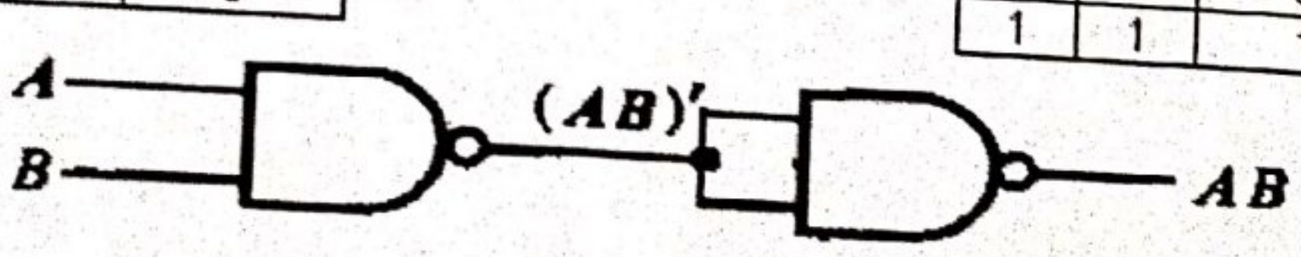
NOT (inverter)

NOT gate	
A	$\overline{A}$
0	1
1	0

NAND gates as AND gate

2 Input NAND gate		
A	B	$\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

2 Input AND gate		
A	B	AB
0	0	0
0	1	0
1	0	0
1	1	1



AND

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overall output will be that of an AND gate.

$$Y = ((A.B)')'$$
$$Y = (A.B)$$

NAND gates as OR gate

From DeMorgan's theorems : $(A.B)' = A' + B'$

$$\Rightarrow (A'.B')' = A'' + B'' = A + B$$

So, give the inverted inputs to a NAND gate, obtain OR operation at output.

NAND gates as X-OR gate

The output of a input X-OR gate is shown by $Y = A'+B + AB'$. This can be achieved with the logic diagram shown in. the left side.

Gate No.	Inputs	output
1	A, B	(AB)'
2	A, (AB)'	(A(AB)')'
3	(AB)', B	(B(AB)')'
4	(A(AB)')', (B(AB)')	A'B + AB'

Now the output from gate no. 4 is the overall output of the configuration.

$$Y = ((A.(AB)')' \ (B(AB)')')'$$
$$= (A(AB)')'' + (B(AB)')''$$

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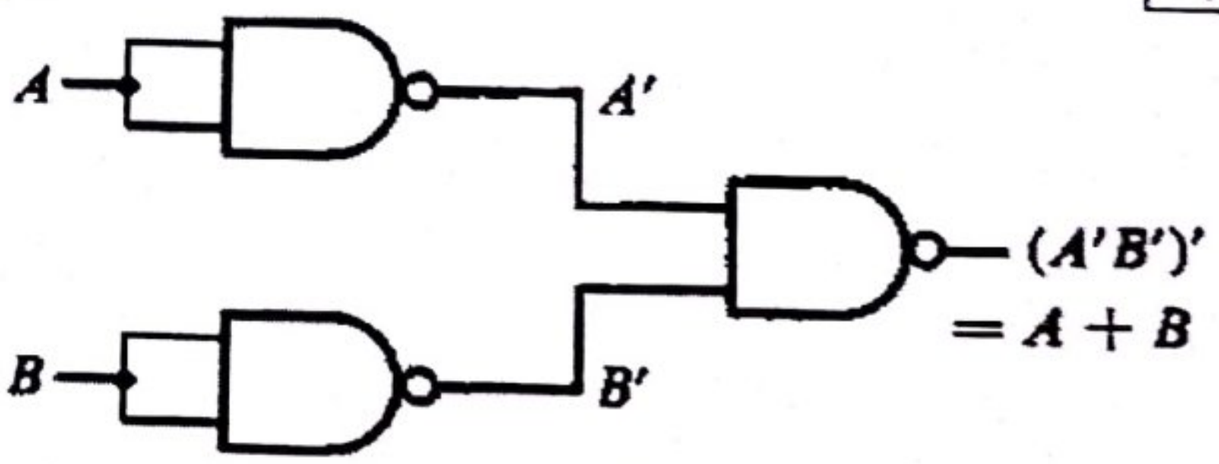
NAND gates as OR gate

2 Input NAND gate		
A	B	$\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

2 Input OR gate		
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

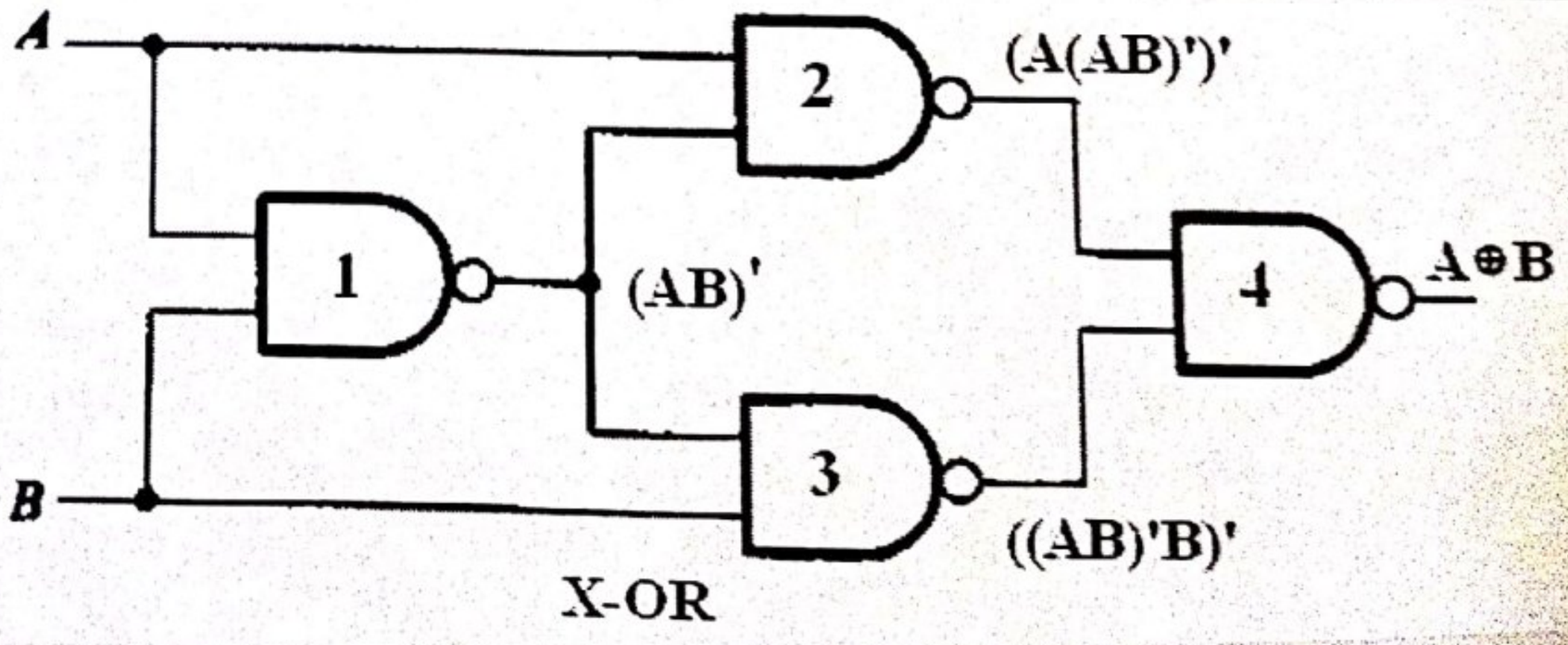


OR

NAND gates as X-OR gate

2 Input NAND gate		
A	B	$\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

2 Input EXOR gate		
A	B	A⊕B
0	0	0
0	1	1
1	0	1
1	1	0



X-OR

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$= (A(AB)') + (B(AB)')$

$= (A(A'+B)') + (B(A'+B'))$

$= (AA'+AB') + (BA'+BB')$

$= (0+AB') + BA'+0)$

$= AB^2 + BA'$

$y = AB^2 + A'B$

NAND gates as X-NOR gate

X-NOR gate is actually X-OR gate followed by NOT gate. So give the output of X-OR gate to a NOT gate, overall output is that of an X-NOR gate.

$$y = AB + A'B'$$

NAND gates as NOR gate

A NOR gate is an OR gate followed by NOT gate. So connect the output of OR gate to a NOT gate, overall output is that of a NOR gate.

$$y = (A+B'$$

PROCEDURE:-

(i) Connect the trainer kit to ac power supply.

(ii) Connect the NAND gate for any of the logic

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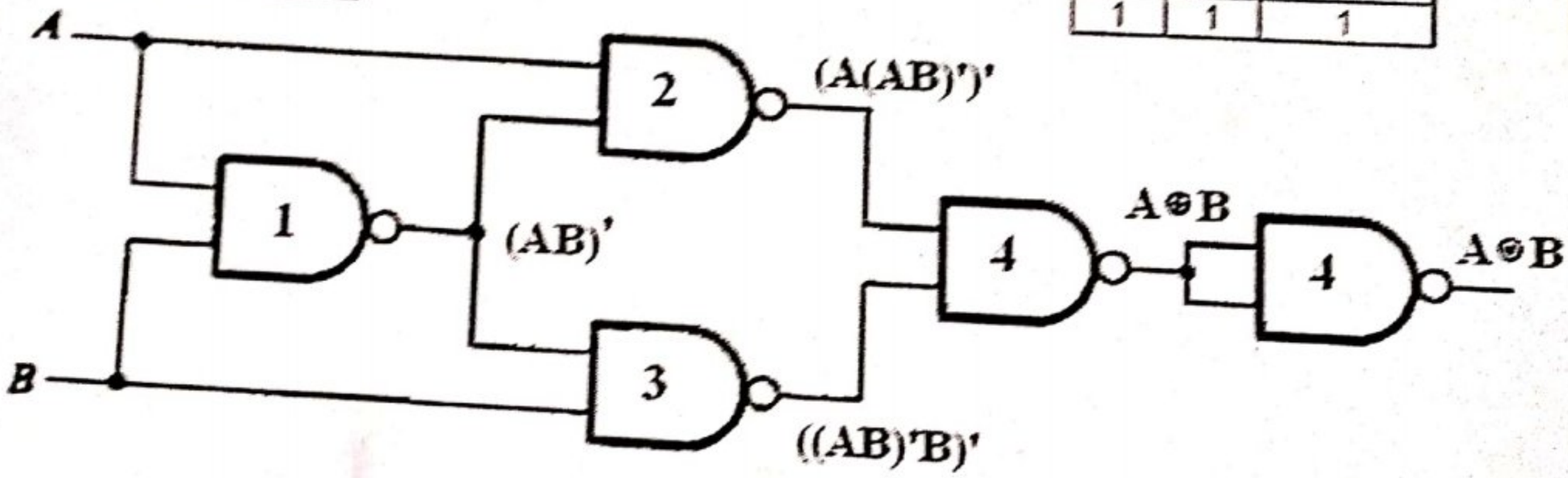
NAND gates as X-NOR gate

2 Input NAND gate		
A	B	$\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

2 Input EXNOR gate		
A	B	$\overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

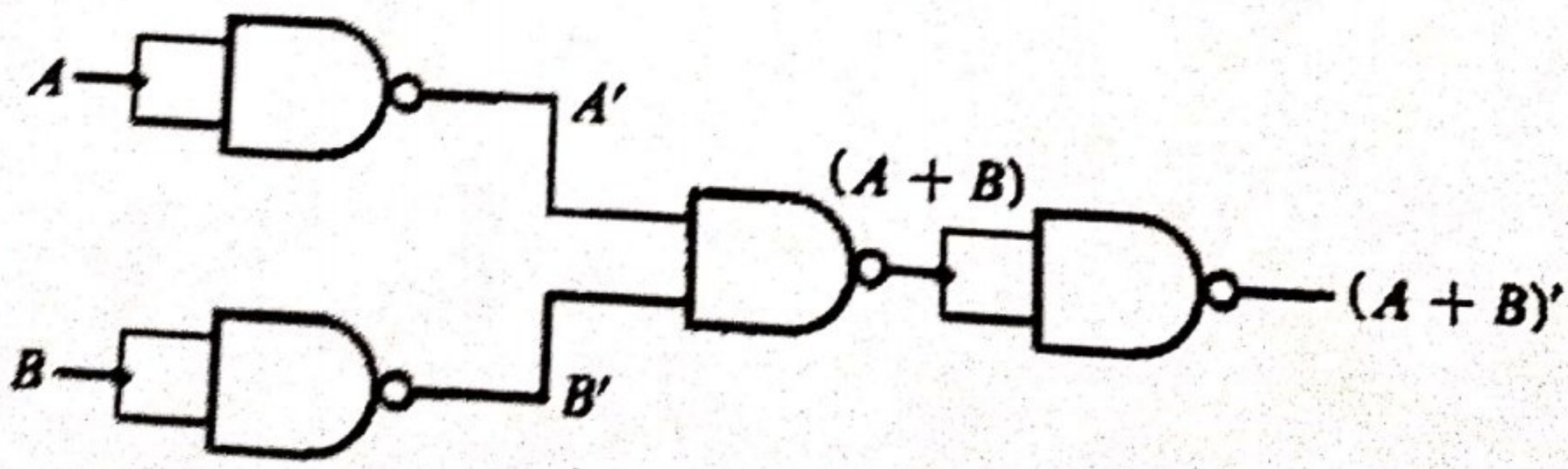


X-NOR

NAND gates as NOR gate"

2 Input NAND gate		
A	B	$\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

2 Input NOR gate		
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0



NOR

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functions to be realised.

(iii) Connect the input of first stage to logic sources and output of the last gate to logic indicator.

(iv) Apply various input combinations and observe output for each one.

(v) verify the truth table for each input / output combination.

(vi) Repeat the process for all logic functions.

(vii) Switch off the ac power supply.

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