
Section 41. Prefetch Module for Devices with L1 CPU Cache

HIGHLIGHTS

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Note: This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all PIC32 devices.

Please consult the note at the beginning of the “**Prefetch Module**” chapter in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: <http://www.microchip.com>

41.1 INTRODUCTION

This section describes the features and operation of the Prefetch module for PIC32 devices with L1 CPU Cache. Prefetch module features increase system performance for most applications.

41.1.1 Prefetch Module Features

The Prefetch module includes the following features:

- 4 x 16 byte fully associative lines
- One line for CPU instructions
- One line for CPU data
- Two lines for peripheral data
- 16 byte parallel memory fetch
- Configurable predictive prefetch
- Error detection and correction

41.2 PREFETCH MODULE OVERVIEW

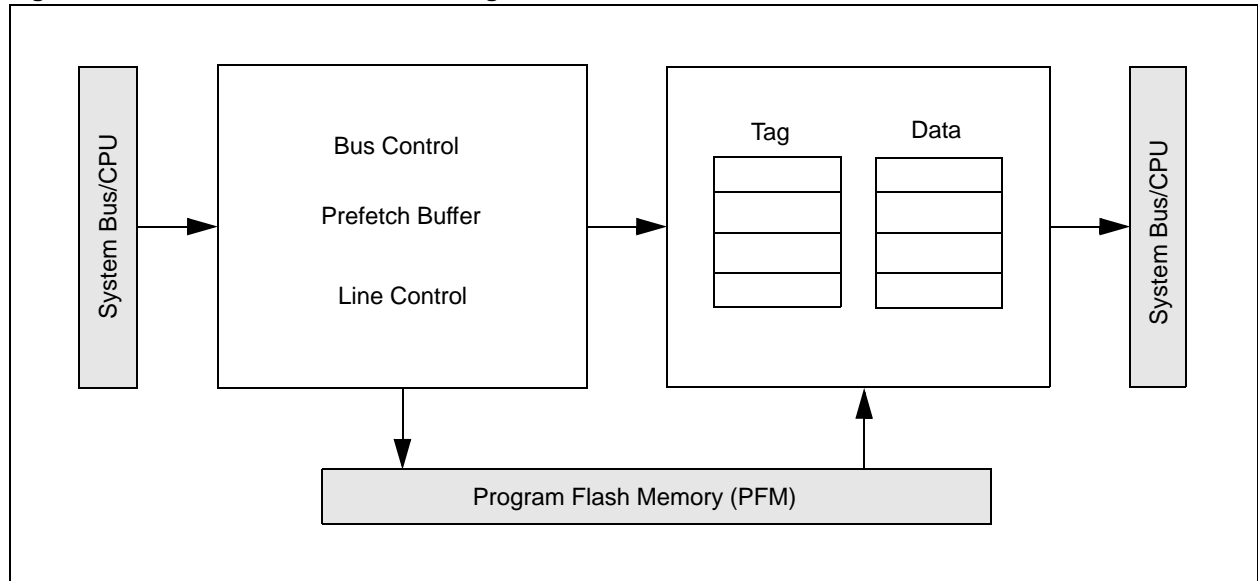
The Prefetch module is a performance enhancing module included in PIC32 devices with L1 CPU caches. When running at high-clock rates, Wait states must be inserted into Program Flash Memory (PFM) read transactions to meet the access time of the PFM. Wait states can be hidden to the core by prefetching and storing instructions in a temporary holding area that the CPU can access quickly. Although the data path to the CPU is 32 bits wide, the data path to the PFM is 128 bits wide. This wide data path provides the same bandwidth to the CPU as a 32-bit path running at four times the frequency.

The Prefetch module holds a subset of PFM in temporary holding spaces known as lines. Each line contains a tag and data field. Normally, the lines hold a copy of what is currently in memory to make instructions or data available to the CPU without Wait states.

Data located in the PFM may be requested by the CPU or by a peripheral. If the requested data is not currently stored in a Prefetch module line, a read is performed to the PFM at the correct address, and the data is supplied to the Prefetch module and to the CPU or peripheral. If the requested data is stored in the Prefetch module and is valid, the data is supplied to the CPU or peripheral without Wait states.

Figure 41-1 shows a block diagram of the Prefetch module. Logically, the Prefetch module fits between the System Bus module and the PFM.

Figure 41-1: Prefetch Module Block Diagram



41.3 CONTROL REGISTERS

The Prefetch module for PIC32 devices with L1 CPU cache contains the following Special Function Registers (SFRs):

- **PRECON: Prefetch Module Control Register**

This register manages configuration of the Prefetch module and controls Wait states.

- **PRESTAT: Prefetch Module Status Register**

This register contains status information for error correction and detection.

[Table 41-1](#) provides a brief summary of the related Prefetch module registers. Corresponding registers appear after the summary, followed by a detailed description of each bit.

Table 41-1: Prefetch Module SFR Summary

Name		Bit 31/15	Bit 30/14	Bit 29/13	Bit 28/12	Bit 27/11	Bit 26/10	Bit 25/9	Bit 24/8	Bit 23/7	Bit 22/6	Bit 21/5	Bit 20/4	Bit 19/3	Bit 118/2	Bit 17/1	Bit 16/0
PRECON ⁽¹⁾	31:16	—	—	—	—	—	PFMSECEN	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	—	—	—	—	—	—	—	—	PREFEN<1:0>			PFMWS<2:0>		
PRESTAT ⁽¹⁾	31:16	—	—	—	—	PFMDDED	PFMSEC	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	—	—	—	—	—	—	PFMSECCNT<7:0>							

Legend: — = unimplemented, read as '0'.

Note 1: These registers have associated Clear, Set and Invert registers at offsets of 0x4, 0x8, and 0xC bytes, respectively. The Clear, Set and Invert registers have the same name with CLR, SET, or INV appended to the register name (e.g., PRECONCLR). Writing a '1' to any bit position in these registers will clear, set or invert valid bits in the associated register. Reads from these registers should be ignored.

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Register 41-1: PRECON: Prefetch Module Control Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0
	—	—	—	—	—	PFMSECEN	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1
	—	—	PREFEN<1:0>		—	PFMWS<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-27 **Unimplemented:** Write '0'; ignore read

bit 26 **PFMSECEN:** Flash SEC Interrupt Enable bit

1 = Generate an interrupt when the PFMSEC bit (PRESTAT<26>) is set

0 = Do not generate an interrupt when the PFMSEC bit is set

bit 25-6 **Unimplemented:** Write '0'; ignore read

bit 5-4 **PREFEN<1:0>:** Predictive Prefetch Enable bits

11 = Enable predictive prefetch for any address

10 = Enable predictive prefetch for CPU instructions and CPU data

01 = Enable predictive prefetch for CPU instructions only

00 = Disable predictive prefetch

bit 3 **Unimplemented:** Write '0'; ignore read

bit 2-0 **PFMWS<2:0>:** PFM Access Time Defined in Terms of SYSCLK Wait States bits

111 = Seven Wait states

110 = Six Wait states

101 = Five Wait states

100 = Four Wait states

011 = Three Wait states

010 = Two Wait states

001 = One Wait state

000 = Zero Wait state

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Register 41-2: PRESTAT: Prefetch Module Status Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	HS, R/C-0	HS, R/W-0	U-0	U-0
	—	—	—	—	PFMDDED	PFMSEC	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	HS, HC, R/W-0	HS, HC, R/W-0	HS, HC, R/W-0	HS, HC, R/W-0	HS, HC, R/W-0	HS, HC, R/W-0	HS, HC, R/W-0	HS, HC, R/W-0
	PFMSECCNT<7:0>							

Legend:	HS = Set by hardware	HC = Cleared by hardware	C = Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Write '0'; ignore read

bit 27 **PFMDDED:** Flash Double-bit Error Detected (DED) Status bit

This bit is set in hardware and can only be cleared (i.e., set to '0') in software.

1 = A DED error has occurred

0 = A DED error has not occurred

bit 26 **PFMSEC:** Flash Single-bit Error Corrected (SEC) Status bit

1 = A SEC error occurred when PFMSECCNT<7:0> was equal to zero

0 = A SEC error has not occurred

bit 25-8 **Unimplemented:** Write '0'; ignore read

bit 7-0 **PFMSECCNT<7:0>:** Flash SEC Count bits

Decrements by 1 its count value each time an SEC error occurs. Holds at zero. When an SEC error occurs when PFMSECCNT<7:0> is zero, the PFMSEC status bit is set. If PFMSECEN is also set, a Prefetch module interrupt event is generated.

41.4 PREFETCH MODULE OPERATION

The Prefetch module is designed to complement an L1 CPU cache rather than replace it. A single 128-bit (16-byte) line holds instructions or data from the PFM. The Prefetch module uses the Wait states value from the PFMWS<2:0> bits (PRECON<2:0>) to determine how long it must wait for a Flash access when it reads instructions or data from the PFM. If the instructions or data already reside in a Prefetch module line, the Prefetch module returns the instruction or data in zero Wait states. For CPU instructions, if prefetch is enabled and the code is 100% linear, the Prefetch module will provide instructions back to the CPU with Wait states only on the first instruction of the Prefetch module line.

One Prefetch module line is allocated to CPU data and two lines are allocated to peripheral data. Which of these lines are enabled is determined by the PREFEN<1:0> bits (PRECON<5:4>). Although the lines are enabled by type, the type is not used for matching. Therefore, the line allocated to CPU data and filled by CPU data can be read by a CPU instruction read or a non-CPU peripheral data read. A non-CPU peripheral could be DMA or any other peripheral that has read access to the PFM.

The Prefetch module does not support preloading, address masking, or line locking.

41.5 PREFETCH MODULE CONFIGURATIONS

The PRECON register controls the general configurations available for accelerating instruction and data accesses to the Flash memory system. The Prefetch module implements the following general options:

- The PFMWS<2:0> bits (PRECON<2:0>) control the number of system clock cycles required to access the PFM
- The PREFEN<1:0> bits (PRECON<5:4>) control which types of reads are predictively prefetched
- The PFMSECEN bit (PRECON<26>) controls whether the Prefetch module generates an interrupt event on a specific count of single bit errors corrected by the Flash Error Correction Code (ECC)

41.6 PREFETCH MODULE PREDICTIVE PREFETCH BEHAVIOR

When configured for predictive prefetch, the Prefetch module predicts the next line address, fetches the data, and then stores it in the prefetch buffer. If the requested instruction or data is not in a Prefetch module line, and the read address matches the predicted address, the contents of the prefetch buffer are loaded in the Prefetch module line while simultaneously returning the critical word to the read initiator.

If enabled, the prefetch function starts predicting based on the first address read to the PFM. When the first line is placed in the Prefetch module, the module simply increments the address to the next 16-byte aligned address and starts a PFM access.

Predictive prefetches, like all PFM read accesses, are never aborted. If a new address request does not match the predicted address, a new PFM access occurs after the current access finishes. The PREFEN <1:0> bits (PRECON<5:4>) control what types of requests can start a predictive prefetch. They can be CPU instruction only, CPU instruction and data, or CPU and peripheral reads. The use of CPU and peripheral data read prefetching is beneficial for reading large data structures in the PFM. One such case would be to verify the entire flash with a Hash or CRC value using DMA. For all other use models, it is best to only allow prediction on CPU instructions.

If the selected system clock speed is sufficiently low enough to access the Flash at zero Wait states, predictive prefetch is detrimental and should be disabled.

41.7 COHERENCY SUPPORT

When a PFM programming event occurs, the Prefetch module invalidates all lines and the contents of the prefetch buffer. If a transaction is in progress, the invalidation occurs after completion. When programming or erasing a Flash page, a read of that Flash page will cause the transaction to stall until the erase or program event completes.

41.8 EFFECTS OF RESET

41.8.1 On Reset

Upon a device Reset, the following occurs:

- All lines are invalidated
- All tag bits are cleared

41.8.2 After Reset

The module operates as per the values in the PRECON register ([Register 41-1](#)).

41.9 ERROR CONDITIONS

The Prefetch module handles and reports information about two error types: ECC Double-bit Error Detected (DED) and ECC Single-bit Error Corrected (SEC). The ECC Error detection logic is enabled and disabled using the configuration bits, FECCCON<1:0> (DEVCFG0<9:8>). Refer to the “**Special Features**” chapter in the specific device data sheet for information on the DEVCFG0 Configuration register.

The ECC logic increases the read access delay from the PFM. Depending on the frequency of the system clock, the wait states may be different between ECC enabled and ECC disabled. Please see the specific device data sheet for flash access timing specifications for a particular device.

Note: ECC errors are captured for predictive prefetch reads of the PFM. However, those errors are not reported until, and unless, that data is used by the system.

41.9.1 ECC Double-bit Error Detected (DED)

A read from the Flash memory that results in a PFM ECC DED causes the Prefetch module to return a bus exception error to the initiator. If that initiator is the CPU, it recognizes the bus exception error, prevents the instruction from executing, or read data from loading, and generates an exception using the bus exception error vector.

When an ECC DED error occurs, the PFMDDED bit (PRESTAT<27>) is set. The exception handling code can then check this bit to determine whether the exception was caused by a PFM ECC DED event. This bit must be cleared in software by the exception handler.

Note: CPU instructions or data prefetched from the PFM will always be loaded into the Prefetch module, even if a DED error is generated. The Prefetch module line containing the DED data will be tagged as valid until the line is replaced.

41.9.2 ECC Single Error Corrected (SEC)

A PFM ECC SEC event is not a critical error and as such is reported through an interrupt. The user has the option to enable or disable this interrupt through the PFMSECEN bit (PRECON<26>). The data in the Prefetch module is correct, and no further ECC events are generated for addresses that hit the data line as long as that data is in the Prefetch module.

Each read that returns from the PFM with an ECC SEC status causes the PFMSECCNT<7:0> bits (PRESTAT<7:0>) to decrement by one. If PFMSECCNT<7:0> is zero and a PFM ECC SEC event occurs, the PFMSEC bit (PRESTAT<26>) is set and an interrupt is generated. Therefore, the PFMSECCNT<7:0> bits should be set to the number of PFM ECC SEC events desired for an interrupt minus 1. For example, to generate an interrupt after five PFM ECC SEC events, PFMSECCNT<7:0> should be set to four ('00000100'). The Prefetch module does not reload the PFMSECCNT<7:0> bits when it reaches zero. Software must write the desired count each time it services the PFMSEC interrupt.

Software can generate an ECC SEC interrupt by setting the PFMSECEN bit and then setting the PFMSEC bit. If the PFMSEC bit is already set when PFMSECEN is set, the Prefetch module will also generate an ECC SEC interrupt. The ECC SEC interrupt persists as long as the PFMSECEN and PFMSEC bits remain set.

41.10 OPERATION IN POWER-SAVING MODES

41.10.1 Sleep Mode

When the device enters Sleep mode, the Prefetch module is disabled and placed into a low-power state where no clocking occurs in the module.

41.10.2 Idle Mode

When the device enters Idle mode, the Prefetch module and its clock source remain functional and the CPU stops executing code. Any outstanding prefetch completes before the Prefetch module stops its clock through automatic clock gating.

41.10.3 Debug Mode

The behavior of the Prefetch module is unaltered in Debug mode.

41.11 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC32 device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Prefetch Module for Devices with L1 CPU Cache are:

Title	Application Note #
No related application notes at this time.	N/A

<p>Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC32 family of devices.</p>
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41.12 REVISION HISTORY

Revision A (August 2012)

This is the initial released version of the document.

Revision B (September 2013)

This revision includes the following updates:

- All references to BMX and Bus Matrix were updated to System Bus
- Minor updates to text and formatting were incorporated throughout the document

NOTES:

Note the following details of the code protection feature on Microchip devices:

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