VLSI 기말 프로젝트

JPEG Compression with DCT

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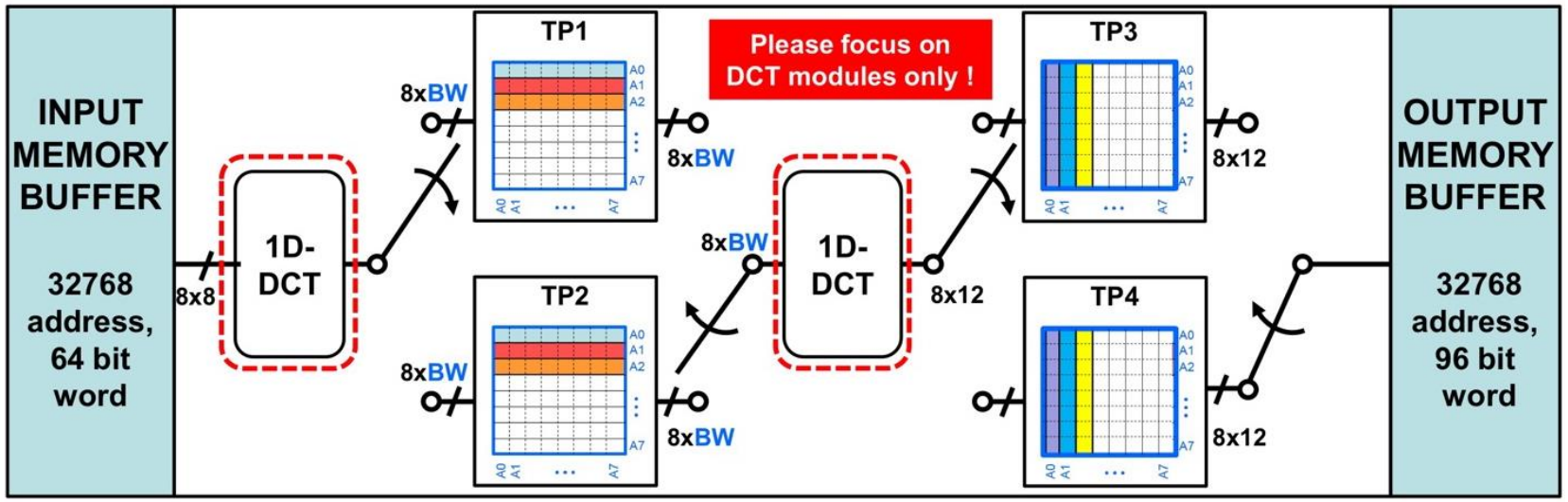
Overall



Overall Dataflow

- MATLAB-stage optimization
  - Small coefficient bit width & 2nd DCT bit width
  - DCT result Simplification
    - Decrease in DCT operations
    - Decrease in TP memory size
- Verilog-stage optimization
  - Reducing DCT area – coefficient multiplication overhead
  - Glitch resolution

$$T = \begin{bmatrix} c_4 & c_4 & c_4 & c_4 & c_4 & c_4 & c_4 & c_4 \\ c_1 & c_3 & c_5 & c_7 & -c_7 & -c_5 & -c_3 & -c_1 \\ c_2 & c_6 & -c_6 & -c_2 & -c_2 & -c_6 & c_6 & c_2 \\ c_3 & -c_7 & -c_1 & -c_5 & c_5 & c_1 & c_7 & -c_3 \\ c_4 & -c_4 & -c_4 & c_4 & c_4 & -c_4 & -c_4 & c_4 \\ c_5 & -c_1 & c_7 & c_3 & -c_3 & -c_7 & c_1 & -c_5 \\ c_6 & -c_2 & c_2 & -c_6 & -c_6 & c_2 & -c_2 & c_6 \\ c_7 & -c_5 & c_3 & -c_1 & c_1 & -c_3 & c_5 & -c_7 \end{bmatrix} \begin{bmatrix} x_0 \\ x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \\ x_7 \end{bmatrix}$$

$$c_k = \frac{1}{2} \times \cos\frac{k\pi}{16}$$

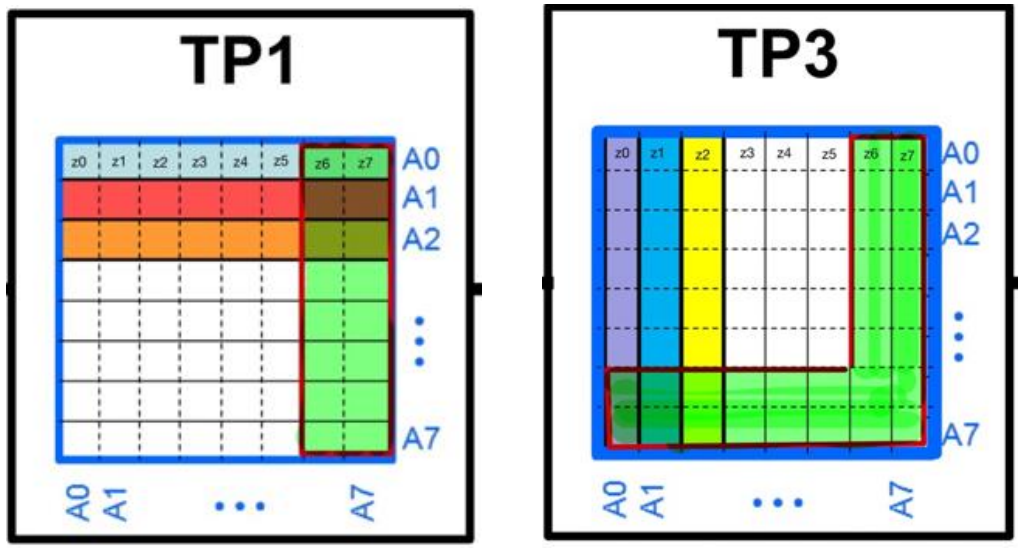
Discrete Cosine Transform

MATLAB-stage: Optimizations

- C_quantization_bit = 9
- Result_1D_DCT_quantization_bit = 8 (1st DCT&TP1,2 Bit Width)
  - Crucial factor of area for both 1st DCT and TP memory 1,2
- lead to the minimal PSNR of 29.5

- which lead to further optimization leg room for DCT-result simplification

DCT Result Simplification



- Inspired by results of naïve DCT - Sensitivity Differences

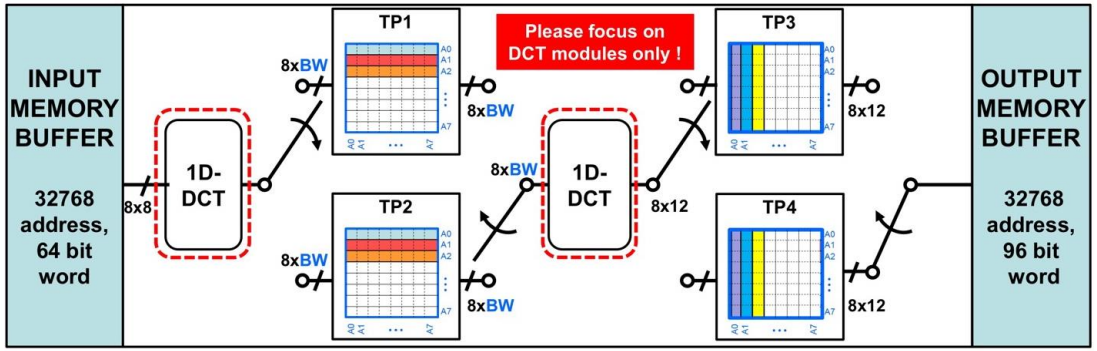
328	328	312	312	320	320	320	320
0	0	0	0	0	0	0	0
-8	0	0	0	0	0	0	0
0	0	-8	-8	0	-8	0	-8
0	0	-8	0	0	0	0	0
-8	0	-8	0	0	0	0	0
0	0	0	0	0	0	0	0
-8	0	0	-8	0	-8	0	-8

412	-5.7500	17	-22.7500	-59.7500	-34.2500	-51.2500	19.7500
67.5000	-12.7500	2	-41.5000	-63.5000	8	4.2500	48.5000
42.2500	-3.2500	-18	6	3.5000	31.2500	23.7500	18.2500
45.2500	21	-41	7.5000	6.2500	-10	-8	5
-8.7500	5.5000	17	-34.2500	-3	11.2500	-17.2500	-3
12	23.5000	-15.7500	-6.5000	1.5000	11.7500	1.5000	-5.5000
-8.5000	7.2500	1.2500	-14.7500	1.5000	-13	-16	7.5000
6	-10.7500	2	-10	1.2500	9	6.5000	-6

c.f. Operation is transposed before calculation

DCT Result Simplification

- More aggressive simplification of 2nd DCT result
  - 1st DCT result is reused for 2nd DCT
    - High freq. elements of 1st DCT result are used for z0,z1 of 2nd DCT
  - But 2nd DCT result is mere output



- Lead to decrease of DCT operation and TP memory size
  - Operations for deriving z6, z7 is no longer needed
  - TP memory for storing z6, z7 is no longer needed

MATLAB Simulation Result

Restored image #1
PSNR : 3.033914e+01

Restored image #2
PSNR : 3.316125e+01

Restored image #3
PSNR : 3.476616e+01

Restored image #4
PSNR : 3.307670e+01

Restored image #5
PSNR : 2.916061e+01

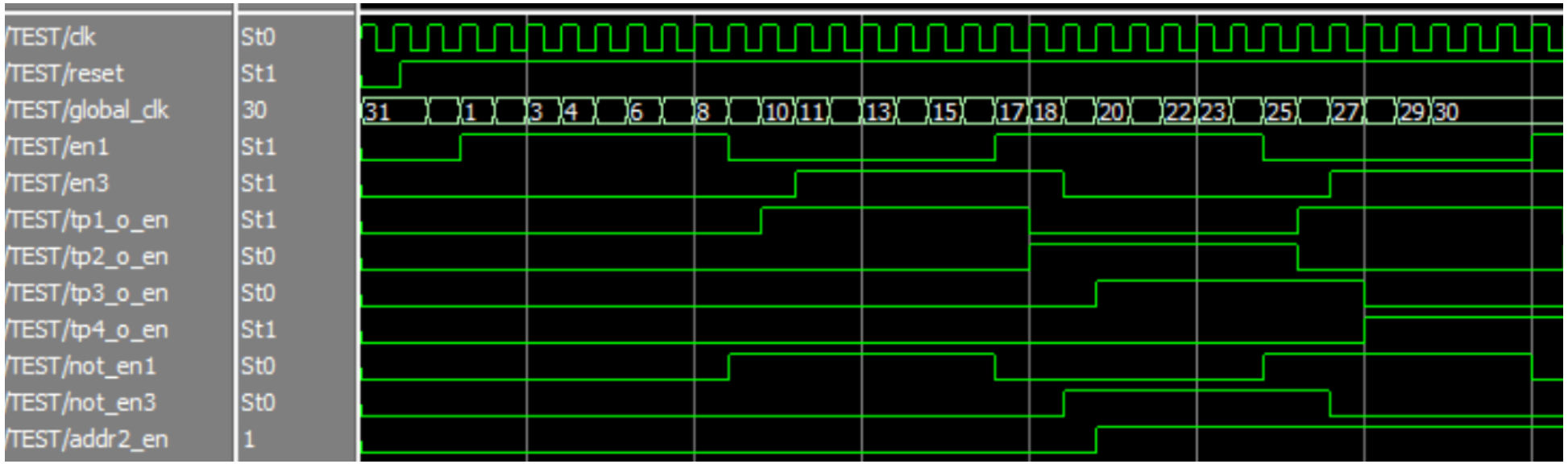
Restored image #6
PSNR : 3.481137e+01

Restored image #7
PSNR : 3.249734e+01

Restored image #8
PSNR : 3.600666e+01

Verilog-stage: Control signal and Address

- A global clock with stoppage point 30 to enable each TPs
- Address counter for each SRAM for input & output
- TP control module with reference to global clock



- Area of control & addr. unit was relatively small

Verilog-stage: Reducing DCT Area

- Even & Odd DCT
- Coefficient multiplier as shift operations
- Key Objectives
  - Reduce large-bit additions: Add before shifting

$$a_1 = x_0 + x_7 \qquad b_1 = a_1 + a_4$$

$$a_2 = x_1 + x_6 \qquad b_2 = a_2 + a_3 \qquad c = b_1 + b_2$$

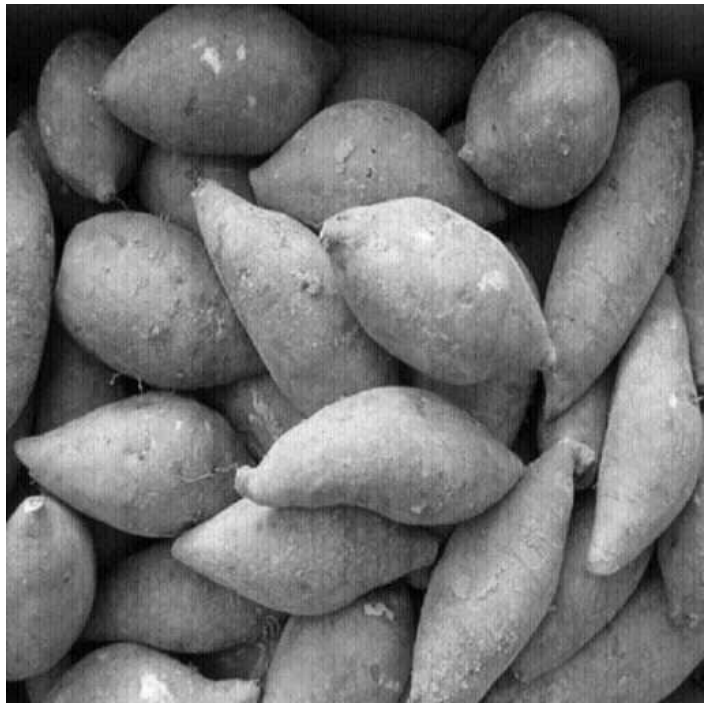
$$a_3 = x_2 + x_5 \qquad b_3 = a_1 - a_4 \qquad c_2 = b_1 - b_2$$

$$a_4 = x_3 + x_4 \qquad b_4 = a_2 - a_3$$

  - Operand Sharing
  - Omit unused operand and calculation
    - Unnecessary calculation for z6, z7 omitted

Verilog-stage: Glitch Resolution

- Occurs as a result of overflowing at points (1,2) and (2,1)
- Raise the truncation range of those points by 1-bit
  - controlled by a pixel address counter at 2nd DCT module
- Revise the corresponding MATLAB shifting



Performance

Restored image
PSNR : 3.027380e+01

Restored image
PSNR : 3.353156e+01

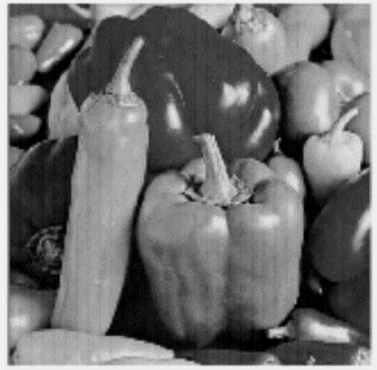
Restored image
PSNR : 3.517250e+01

Restored image
PSNR : 3.341888e+01

Restored image
PSNR : 2.918190e+01

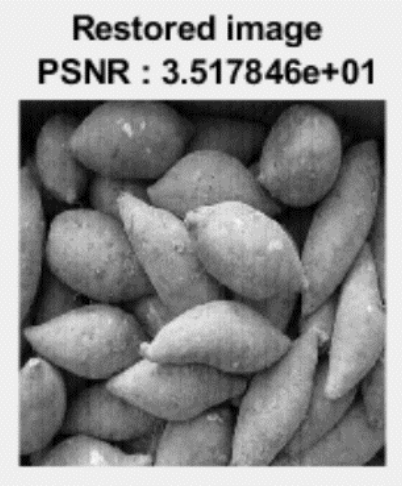
Restored image
PSNR : 3.504731e+01

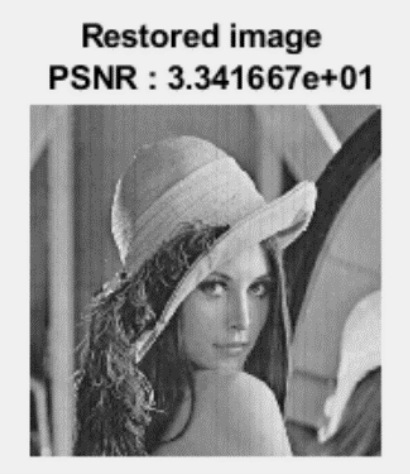
Restored image
PSNR : 3.268067e+01

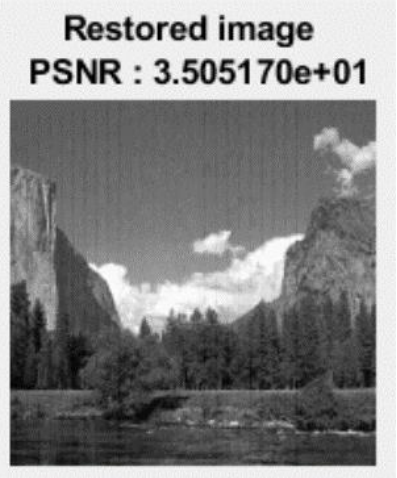


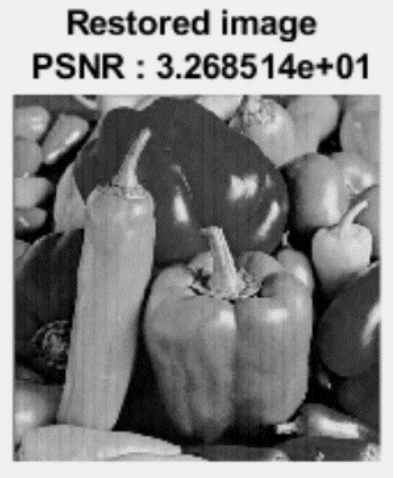
Restored image
PSNR : 3.650700e+01

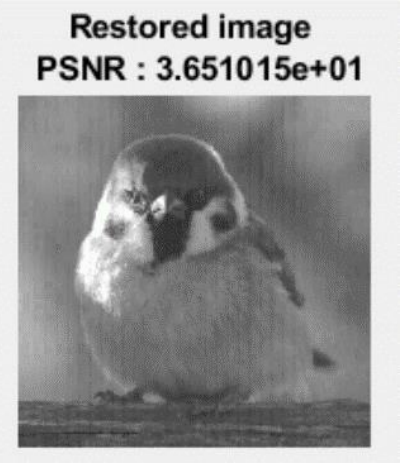
Performance: revised











Synthesis Result

Module name	Area (nm^2)	Percentage (%)
DCT1	143144.8594	17.3
DCT2	163796.8125	19.8
TP1	108755.5312	13.2
TP2	108738.9453	13.2
TP3	124083.5391	15.0
TP4	124083.5391	15.0
etc.	53667.0591	6.5
Total	825647.0625	100.0

- Small Bit width for DCT2 and TP memory 3,4
- TP Memory 1,2 : Column 6,7 Eliminated
- TP Memory 3,4 : Column, Row 6,7 Eliminated
- DCT: Calculation of z6, z7 Eliminated

Synthesis Result:final

Module name	Area (nm^2)	Percentage (%)
DCT1	143518.0938	17.3
DCT2	166857.3906	20.1
TP1	108556.4531	13.1
TP2	108639.3984	13.1
TP3	124083.5391	15.0
TP4	124083.5391	15.0
etc.	53920.3388	6.5
Total	829266.7500	100.0

- Small Bit width for DCT2 and TP memory 3,4
- TP Memory 1,2 : Column 6,7 Eliminated
- TP Memory 3,4 : Column, Row 6,7 Eliminated
- DCT: Calculation of z6, z7 Eliminated