ELEN2002 Transmission and Interface Design

Lab report 03

Measurement of typical digital IC performances

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DECLARATION

I hereby declare this is entirely my own work except for the references quoted. I declare that I have read the University's statement on plagiarism and copyright protection and that I have upheld them in producing this work.

Troyee
Signature

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Abstract

This study describes the experimental evaluation of a digital logic inverter's performance under both low and high load situations. Current draw, timing delays, signal rise/fall transitions, and voltage transfer response are among the important parameters that are analysed. Comparing the behaviour of the circuit under varying capacitive demands was made possible using 1-load and 5-load setups. Measurements made with an oscilloscope showed load-dependent changes in power and speed, which was consistent with theory.

Aims

The goal of this study is to evaluate the performance of a digital integrated circuit by exploring key operational characteristics and comparing experimental results to the logic family's standard specifications.

Introduction

A digital logic gate's performance was examined in this experiment by analysing several crucial electrical properties.

The first step was to identify the input voltage ranges that influence output transitions by analysing the voltage transfer curve. Next, the gate's response time to input changes was monitored by measuring timing metrics such rise time, fall time, and propagation delay.

In order to assess the circuit's power usage, voltage and current were monitored. This provided information on how various logic families manage energy efficiency.

Background

Digital logic circuits are vital in computing systems because they allow for the reliable switching between logic states. Electrical properties including voltage transfer behaviour, signal transmission time, and power consumption affect how well these circuits work.

This experiment's focus is the inverter logic gate, which is commonly implemented using TTL (Transistor-Transistor Logic) technology, such the 7404 IC. The voltage transfer characteristic, or VTC, explains how the gate's output voltage responds to variations in the input voltage. This makes it easier to locate the areas where the gate alternates between logic high and logic low.

The propagation delay is the time required for an output to respond to an input transition. It can be measured both low-to-high and high-to-low. Additionally, rise time and fall time show how fast the output voltage increases or decreases during changes.

Another crucial element of digital circuitry is power consumption. It describes the quantity of current that the gate draws while it is operating. To determine the energy consumption of the gate under various circumstances, current utilization was monitored in this experiment using various input signals and loads. Moreover, Both the timing characteristics and the current consumption may alter when the number of linked loads rises (for example, from 1 load to 5 loads). Measuring these effects helps to evaluate the logic gate's efficiency and performance in real-world applications.

Equipment

1. 100 MHz CRO and probes
2. 15 MHz function generator
3. Digital Multimeter
4. Cables
5. Twin DC power supply
6. IC: 7404
7. 1 Ω resistor
8. Matrix board
9. Wire cutters
10. Wires

Procedure

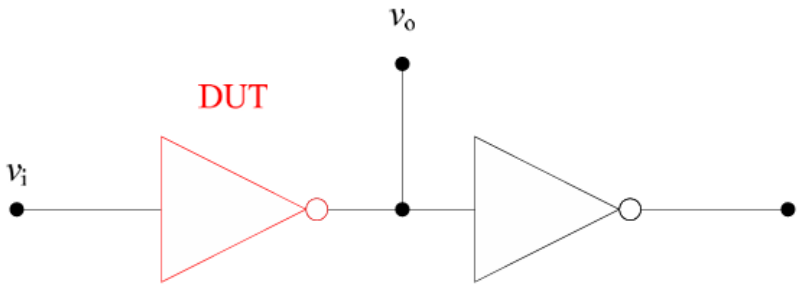

Figure 1 Inverter driving 1 load

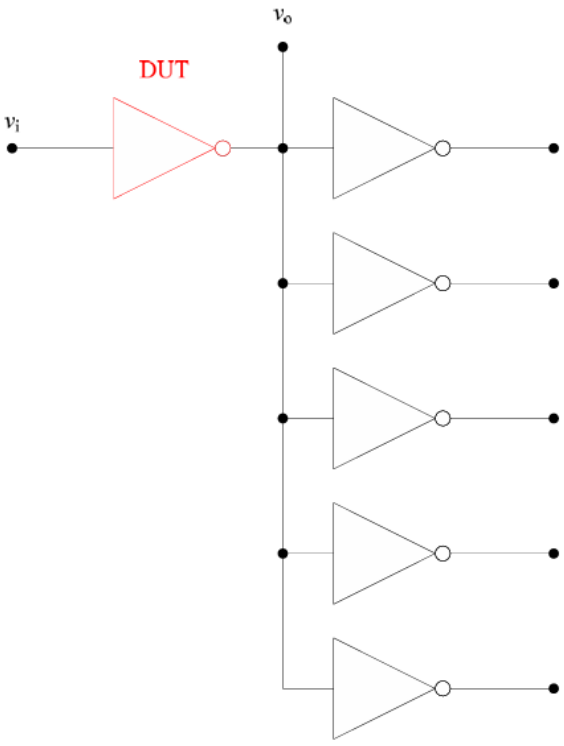

Figure 2 Inverter driving 5 loads

- ***Voltage Transfer Characteristics***

1. Using 7404 device to connecting the figure 1 circuit.
2. Now applying 5V to *Vcc* and a variable DC voltage to *vi*
3. Altering the voltage to *vi* from 0 V to 5 V in steps of 0.5 V.
4. Measuring and recording the output voltage.
5. Repeating all above steps for figure 2 with device load of 5

- ***Power Supply Range***

1. Implementing the figure 1.
2. Adjusting *Vcc* to 4 V
3. Supplying a10 kHz square wave to *vi using a function generator.*
4. Observing and recording input, output waveforms using oscilloscope.
5. Now ,repeating all the above steps for Vcc = 4.5 V, 5.0 V, 5.5 V and 6.0 V respectively.
6. Measuring the following parameters propagation delays (high-to-low ,low-to-high), rise time, fall time) from the oscilloscope.
7. Repeating all above steps to the figure 2 (5 load circuit configuration).

- ***Power Requirements***

1. Implementing the figure 2 (5 load circuit).
2. Inserting 1 Ω resistor between the DC power supply and VCC.
3. Building the DC power supply 5 V.
4. Building up the function generator to supply a square wave of 1 MHz to vi.
5. Measuring the DC current that flows through the 1 Ω resistor.
6. Repeating all the above steps but replacing the function generator with variable DC voltage source.
7. Measuring the current through the 1 Ω resistor.
8. Now, setting DC voltage source to 0V and then 5 V.

- ***Response of Logic Gates for Analog Signals***

1. Configuring the 5-load circuit from figure 2.
2. Supplying 5 V to Vcc.
3. Applying a 10KHz sinusoidal input signal with voltage range between 0 to 5V.
4. Adjusting peak-to-peak signal 5 V and +2.5 V offset
5. Now ,observing and recording the input, output waveforms.

Results and Observations

- ***Voltage Transfer Characteristics***

(i) **For Figure 1 (Inverter driving 1 load)**

Vi (V)	*Vo(V)*
0	5.04V
0.5	5.045 V
1.0	5.040 V
1.5	5.042V
2.0	5.0394V
2.5	5.029 V
3.0	6.97 mV
3.5	6.05 mV
4.0	3.37 mV
4.5	0.02mv
5.0	0.02m V

Key Obversions:

- When the input voltage (vo) less than 2.5 V the output maintained high (around 5 V).
- Between 2.5 V and 3V there was a noticeable decrease in output as input increased.
- The output voltage sharply decreased and eventually approached zero when the input voltage above 3 V.

(ii) For Figure 2 (Inverter driving 5 loads)

Vi (V)	Vo(V)
0	5.02V
0.5	5.025V
1.0	5.0256 V
1.5	5.028V
2.0	5.032 V
2.5	5.0307 V
3.0	1.04mV
3.5	0.45mV
4.0	0.05mV
4.5	0.04mV
5.0	0.05 mV

Key Obversions:

- The output voltage remained high until the input obtained close to 3 V which is consistent with the previous findings.
- Between 2.5 V and 3 V, the output voltage started reducing dramatically.
- At last, the output rapidly decreased and approached 0mV throughout this transition.

- ***Propagation Delay, and Rise and Fall Times***

(i) For Figure 1 (Inverter driving 1 load)

Output high-to-low propagation delay = 14.00 ns
Output low-to-high propagation delay = 12.00 ns

Output rise time = 11.0 ns
Output fall time =26.5 ns

(ii) For Figure 2 (Inverter driving 5 loads)

Output high-to-low propagation delay = 12.00 ns
Output low-to-high propagation delay = 12.00 ns
Output rise time = 13.20 ns
Output fall time = 17.00 ns

Key Obversions:

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- The fall time was dramatically reduced by increasing the load, suggesting better discharge efficiency.
- Under heavy loading, the rise time became slightly longer due to an increase in the input capacitance.
- The discharge rate of the circuit with 5 loads was slightly higher, but the propagation delays were the same in both scenarios.

- ***Power Requirements:***

For Figure 2 (Inverter driving 5 loads)

(i) Measured Current (Dynamic input):
Average current generated by a 1 MHz square wave input: 0.67mA.

(ii) Measured Current (DC input) :

Input voltage Vi (V)	Current (mA)
0	18.27
5	0.66

Key Obversions:

- When logic low (0 V) was set for the input, more current was used.
- When the input was set to logic high (5 V) in both situations, the current draw significantly decreased, suggesting that less power was used at high logic levels

Results

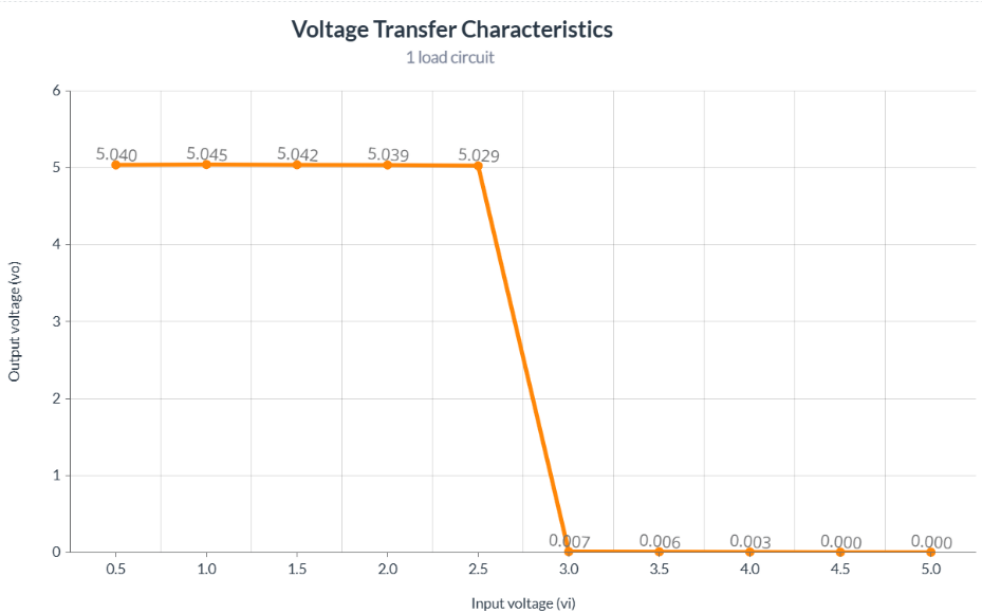

Figure 3: Voltage transfer characteristic for 1 load

With the input voltage (vi) on the x-axis and the output voltage (vo) on the y-axis, the above graph displays the voltage transfer characteristic for the one-load arrangement. The curve remains high until a dramatic decrease occurs between 2.5 and 3.0 V.

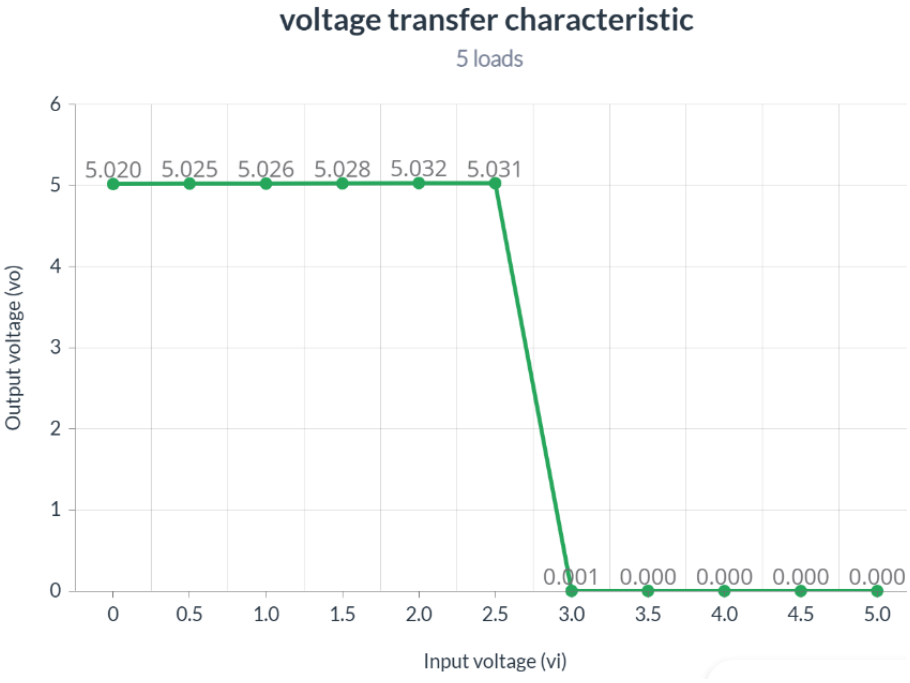

Figure 4: Voltage transfer characteristic for 5 loads

The above graph illustrates the response of the 5-load configuration, where a sharp drop in output voltage (vo) occurs when the input voltage (v_i) increases between 2.5 V and 3.0 V. here, vo is plotted on y-axis and vi is on x-axis.

Discussion

Figure 5: Square waveforms from 1 load Circuit when Vcc = 4.5V

Figure 6: Square waveforms from 1 load Circuit when Vcc = 5 V

Figure 7: Square waveforms from 1 load Circuit when Vcc = 5.5V

Figure 8: Square waveforms from 1 load Circuit when Vcc = 6 V

Figure 9: square waveforms from 5-load circuit Vcc = 4.5V

Figure 10: square waveforms from 5-load circuit Vcc = 5 V

Figure 11: square waveforms from 5-load circuit Vcc = 5.5V

Figure 12: square waveforms from 5-load circuit Vcc = 6V

Here, the waveform outputs for the 1-load circuit are shown in Figures 5 to 8, while the corresponding outcomes for the 5-load design are shown in Figures 9 to 12. The inversion of these waveforms validates the usage of a NOT gate, which is designed to output the logical inverse of the input signal. The input is shown by the yellow line in each waveform picture, and the equivalent output is shown by the green line.

As expected from an inverter, the output remains high when the input is low, and vice versa. The inverter's response time is shown by the visible delay between input and output transitions. The waveforms clearly demonstrate the gate's inverting behaviour under dynamic switching situations, with the green (output) signal dropping as the yellow (input) signal rises and the output rising as the input decreases.

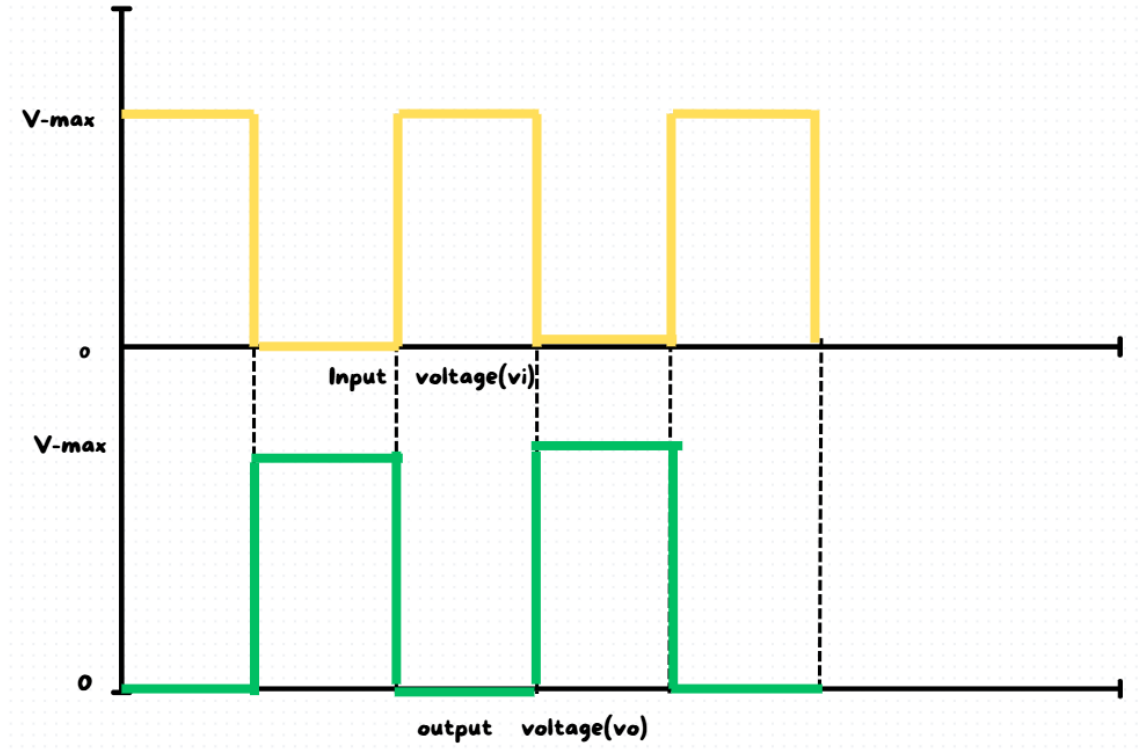

Figure13: sketch for square waveform of 1 load when Vcc =6V

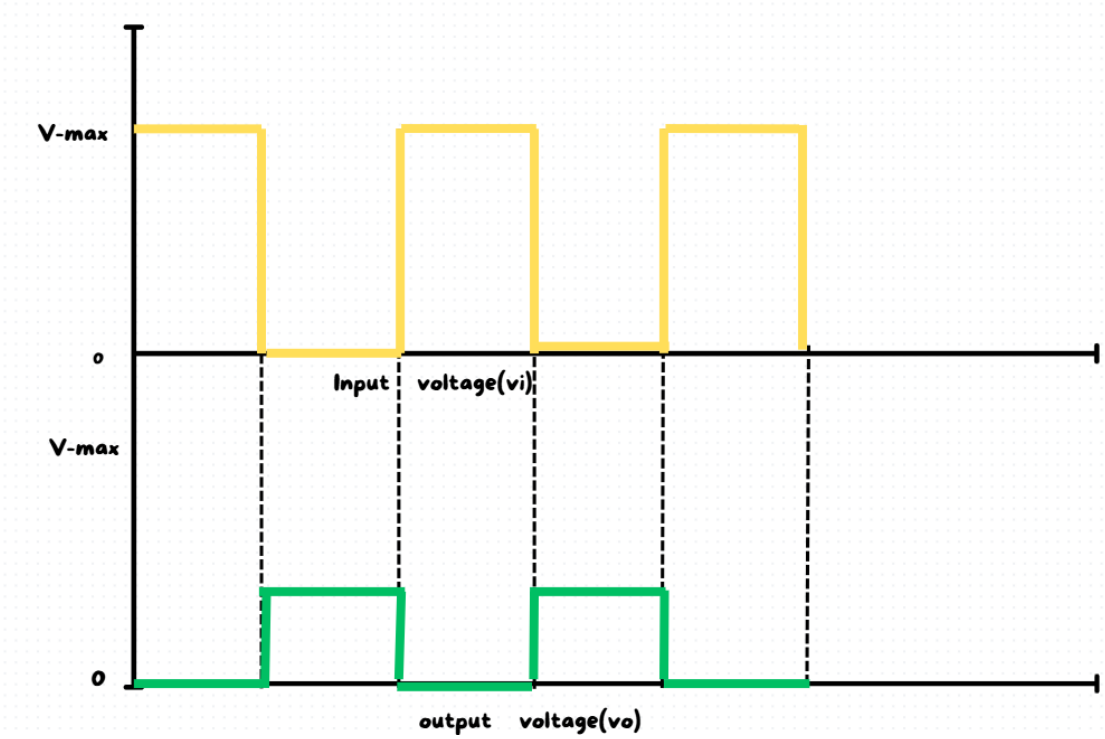

Figure14: sketch for square waveform of 5 load when Vcc =4.5V

The time between the high and low levels in both designs was carefully matched to the intervals observed in the oscilloscope waveforms.

Figure15 : Low to High when 1 load =12 ns

Figure16: High to low when 1 Load =14ns

Figure17: Fall time when 1 load = 26 ns

Figure 18: Rise time when 1-load = 11 ns

Figure 19: High-to-low when 5-load = 12 ns

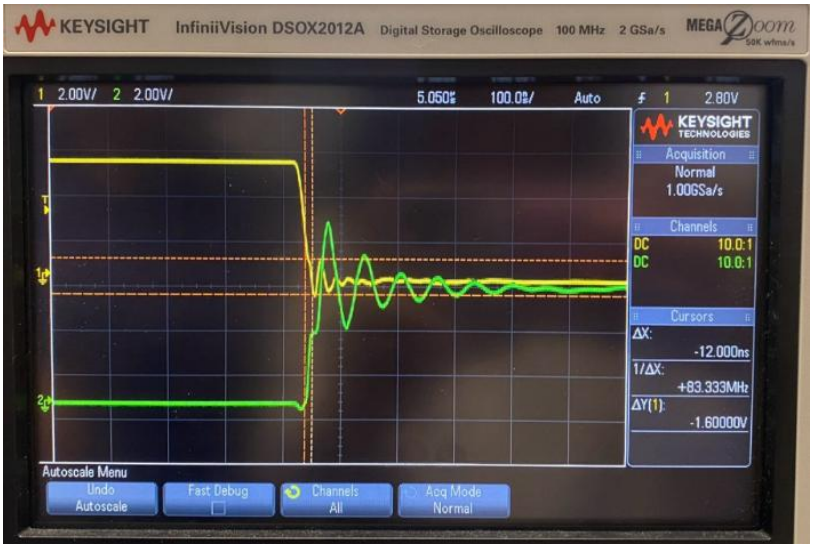

Figure 20: Low-to-high 5-load = 12 ns

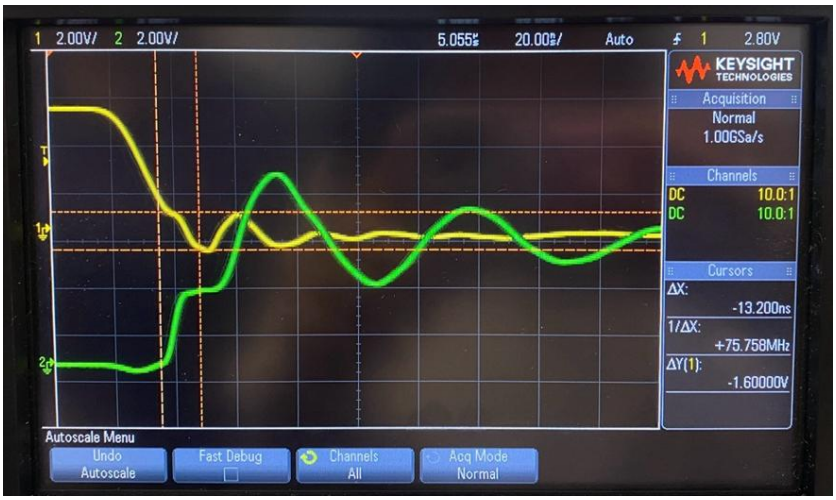

Figure 21: Rise time when 5-load = 13 ns

Figure 22 : Fall time when 5-load = 17 ns

These above figures (15-22) present the recorded waveforms captured using an oscilloscope for each of the given loading conditions. Variable X which stands for time, is included in every image to analyse features like rise time, fall time and delay of the signal waveform. To accurately examine the time relationship between the input and output signals, the cursors were carefully placed.

Measurements of propagation delay were performed in both directions (High-to-Low , Low-to-High)) using both types 1-load and 5-load settings. Theoretically, adding more loads leads to extra delays because of higher capacity and energy costs, but the difference was rarely noticeable at the practical . For instance, the 1-load circuit's recorded fall time of 26 ns was significantly longer than the 5-load setup's 13 ns. Similarly, in the single-load scenario as opposed to the 5-load scenario, the high-to-low delay was marginally higher. The outcome may have been affected by improved switching behaviour with increased load or small problems with the cursor during measurements

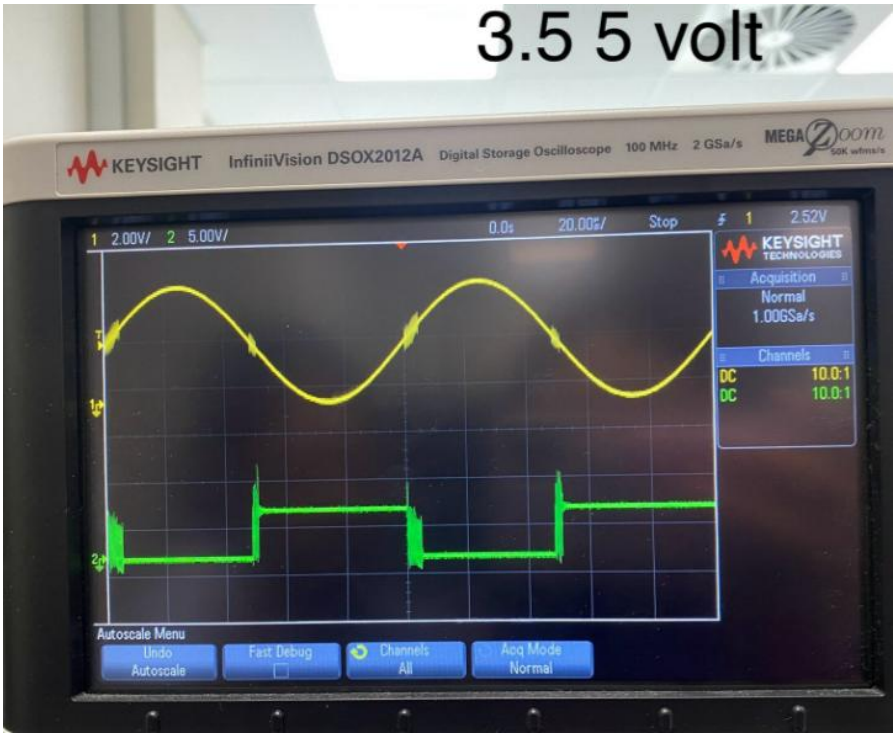

Figure 23 : Input and output waveforms of inverter circuit operating at 5V with a 10Khz sinusoidal input(5 load circuit)

This waveform of figure 23 shows the final stage of the experiment, conducted with a supply voltage (Vcc) of 5 V and a 10Khz sinusoidal input in 5 load circuit. Here, the output signal is green line and input signal is yellow. The output changes from low to high when the input decreases and from high to low when the input increases, as is typical of a NOT gate. With the output waveform maintaining a clear square shape and the voltage levels remaining within acceptable digital logic bounds, the inverter performed exactly as expected under the 5-load condition. This indicates that even with additional loading, the circuit operated as predicted.

Conclusions

This experiment successfully demonstrated how changing output load situations in digital circuits impact important performance characteristics such as voltage transfer behaviour, propagation delay, rise/fall times, and current consumption. The results of comparing the 1-load and 5-load designs showed that higher loading generally modifies power consumption and signal timing, with transition characteristics showing the most significant effects. Small measurement variations were probably caused by manual oscilloscope alignment problems. Overall, the experiment provided a fundamental understanding of how

References

load impacts the performance and effectiveness of digital logic gates.
Lecture Notes.
https://www.visme.co/graph-maker/ -- line graph
https://www.canva.com/ -- sketch of waveforms

Appendix

NIL