CMOS Analog IC Design
RECORD

Course Title:CMOS Analog IC Design
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Program: Btech

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No. of Experiments

1.NMOS Characteristics

2.PMOS Characteristics

3.CMOS Inverter

4.Common Source Amplifier

5.Common Gate Amplifier

6.Common Drain Amplifier

7.Differential Amplifier

8.Current Mirror

1.Nmos Characteristics

Aim:-To observe the input and output characteristics of the NMOS transistor using a cadence tool.

Tools used:-Cadence Tool

Theory:-An NMOS transistor (N-channel Metal-Oxide-Semiconductor) is a type of MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) in which electrons are the majority carriers.The behavior of an NMOS transistor depends on the gate-to-source voltage (**V_{GS}**) and the drain-to-source voltage (**V_{DS}**). The three main regions are:

(i) Cut-off Region:

- Condition: **V_{GS} < V_{th}**
- No inversion layer; the channel is OFF.
- **I_D ≈ 0**

(ii) Triode Region (Linear Region):

- Condition: **V_{GS} > V_{th}** and **V_{DS} < V_{GS} - V_{th}**
- Channel is formed and behaves like a resistor.

- Drain current equation:
  ID=μnCoxW/L[(VGS−Vth)VDS−VDS2]*2I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]ID =μn Cox LW [(VGS −Vth) VDS −2VDS2]

(iii) Saturation Region (Active Region):

● Condition: **V_{GS} > V_{th}** and **V_{DS} ≥ V_{GS} - V_{th}**

- Channel pinches off near the drain.

- Drain current is **independent of V_{DS}** and is given by:
  ID=12μnCoxWL(VGS−Vth)2I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2ID =21 μn Cox LW (VGS −Vth)2 ●

Can be modified to include channel length modulation:
ID=12μnCoxWL(VGS−Vth)2(1+λVDS)I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS})ID =21 μn Cox LW (VGS −Vth)2(1+λVDS)

Procedure:-for input characteristics

1. Draw the schematic as shown in the below fig(1).
2. Click on check and save.
3. Go to Launch ADE L
4. Click on the Session save state click on cell view apply OK
5. Click on the Setup model libraries NN apply OK.
6. Click on the Analysis choose select dc click on save dc operating point click on component parameter click on select component Now schematic window will be appeared automatically, click on the vgs select component parameter window appears, select dc voltage OK
7. Go to ADE L analyses choose start - 0 , stop - 1.8 apply OK
8. Click on the Variables copy from the cell view.

9. Click on the Outputs To be plotted select on design schematic window will be appeared ,select drain terminal of the NMOS transistor

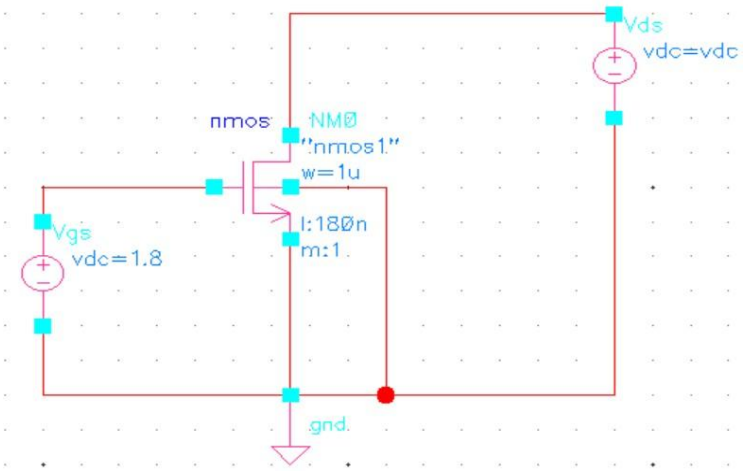
10. Go to ADE L Tools parametric Analysis

Variable --- double click on the variable, select the vds range from

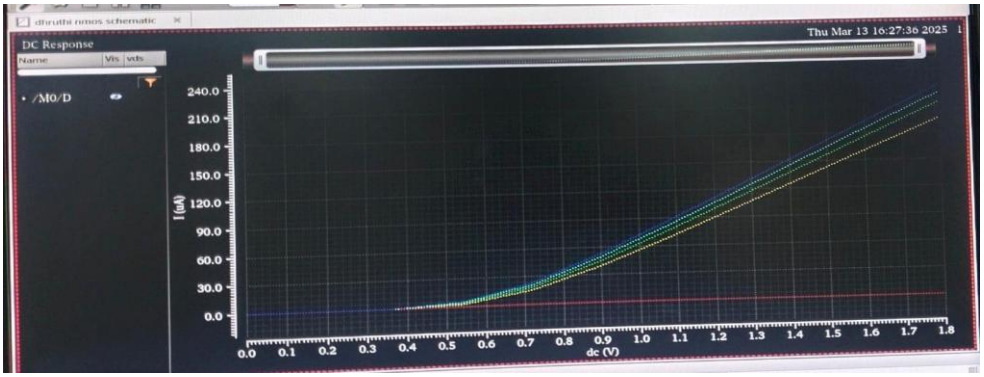
0 to 3. 3total steps --10

Click on Analysis start selected

11.Now the input characteristic of the NMOS transistor will be appeared.



Output:



Steps for Output characteristics:

1. Draw the schematic as shown in the below fig(3).

2. Click on check and save

3. Go to Launch ADE L

4. Session save state click on cell view apply OK.

5. Setup model libraries NN apply OK.

6. Analysis choose select dc click on save dc operating point click on component parameter click on select component

Now schematic window will be appeared automatically, click on the vds select component parameter window appears, select dc voltage OK

7. Go to ADE L analyses choose start - 0 , stop - 1.8 apply OK

8. Variables copy from cell view.

9. Outputs To be plotted select on design schematic window will be appeared ,select drain terminal of the NMOS transistor

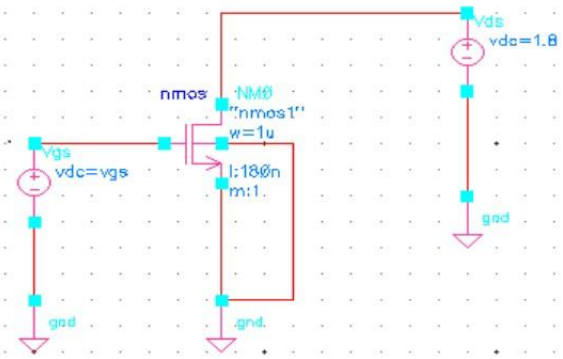
10. Go to ADE L Tools parametric Analysis

Variable --- double click on the variable ,select the vgs range from 0 to 3.3total steps --5

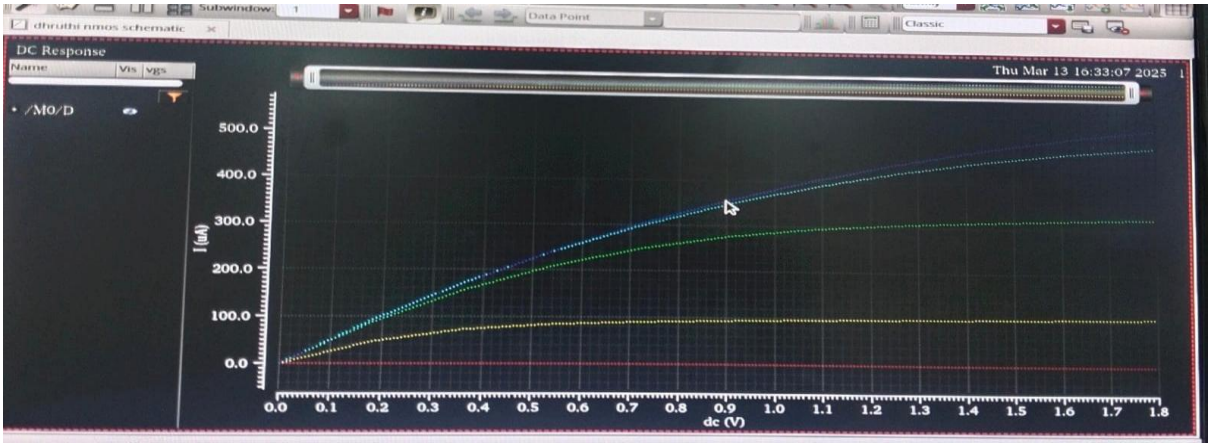
Click on Analysis start selected

11.Now the output characteristic of the NMOS transistor will be appeared.

Circuit diagram



Output:-



2.Pmos Characteristics

Aim: To observe the input and output characteristics of the PMOS transistor using a cadence tool.

Tools used: Cadence Tool

Theory:A PMOS transistor (P-channel Metal-Oxide-Semiconductor) is a type of MOSFET in which holes are the majority carriers.

PMOS operation is **complementary** to NMOS and depends on the **gate-to-source voltage (V_{SG})** and **drain-to-source voltage (V_{SD})**.

(i) Cut-off Region:

- Condition: **V_{SG} < |V_{th}|**
- No channel formed; transistor is OFF.
- **I_D ≈ 0**

(ii) Triode Region (Linear Region):

- Condition: **V_{SG} > |V_{th}|** and **V_{SD} < V_{SG} - |V_{th}|**
- Channel is formed and behaves like a resistor.
- Drain current:
  $ID=\mu_p C_{ox} \frac{W}{L} \left[(V_{SG} - |V_{th}|)V_{SD} - \frac{V_{SD}^2}{2}\right]ID =μp Cox LW [(VSG −∣Vth ∣)VSD −2VSD2]$

(iii) Saturation Region (Active Region):

- Condition: **V_{SG} > |V_{th}|** and **V_{SD} ≥ V_{SG} - |V_{th}|**
- Channel pinches off near the drain.
- Current is **independent of V_{SD}**, and:
  ID=12μpCoxWL(VSG−∣Vth∣)2I_D = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{SG} - |V_{th}|)^2..ID =1/2μp Cox W/L (VSG −∣Vth ∣)2
- Including channel length modulation:
  ID =1/2μp Cox W/L (VSG −∣Vth ∣)*2(1+λVSD)

Steps to get Input characteristics :-

. Draw the schematic as shown in the below fig(1).

. Click on check and save.

. Go to Launch ADE L

. Click on the Session save state click on cell view apply OK

. Click on the Setup model libraries NN apply OK.

. Click on the Analysis choose select dc click on save dc operating point

. Click on component parameter click on select component

Now schematic window will be appeared automatically, click on the vgs select

component parameter window appears, select dc voltage OK

. Go to ADE L analyses choose start - -1.8 , stop - 0 apply OK

. Click on the Variables copy from the cell view.

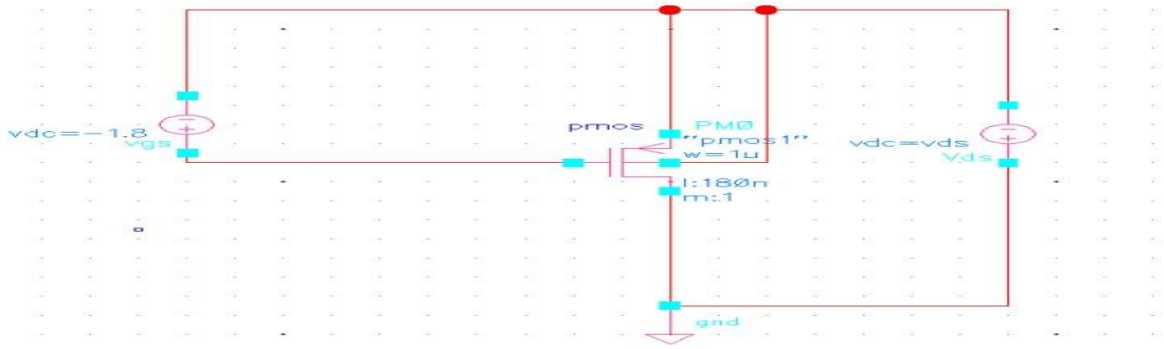
. Click on the Outputs To be plotted select on design schematic window will be

appeared ,select source terminal of the PMOS transistor

. Go to ADE L Tools parametric Analysis

Variable --- double click on the variable ,select the vds range from - 1.8

to 0total steps --5



Click on Analysis start selected

. Now the input characteristic of PMOS transistor will be appeared

Steps for Output characteristics:-

Draw the schematic as shown in the below fig(3).

Click on check and save.

Go to Launch ADE L.

Session save state click on cell view apply OK.

Setup model libraries NN apply OK.

Analysis choose select dc click on save dc operating point click on component parameter click on select component

Now schematic window will be appeared automatically, click on the vds select component parameter window appears, select dc voltage OK

Go to ADE L analyses choose start - -1.8 , stop - 0 apply OK

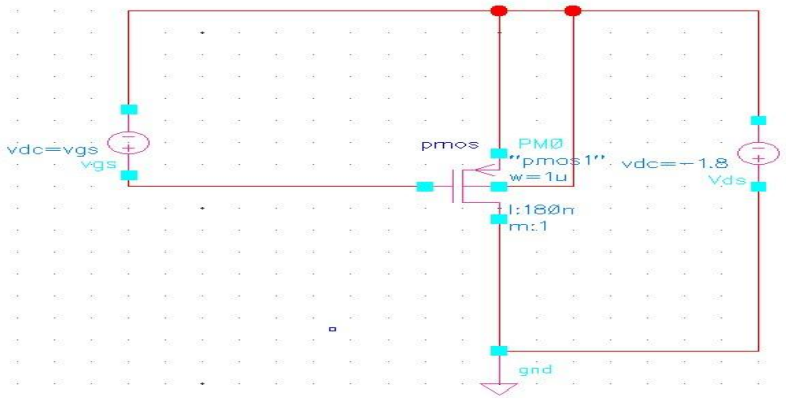
Variables copy from cell view.

Outputs To be plotted select on design schematic window will be appeared select source terminal of the PMOS transistor.

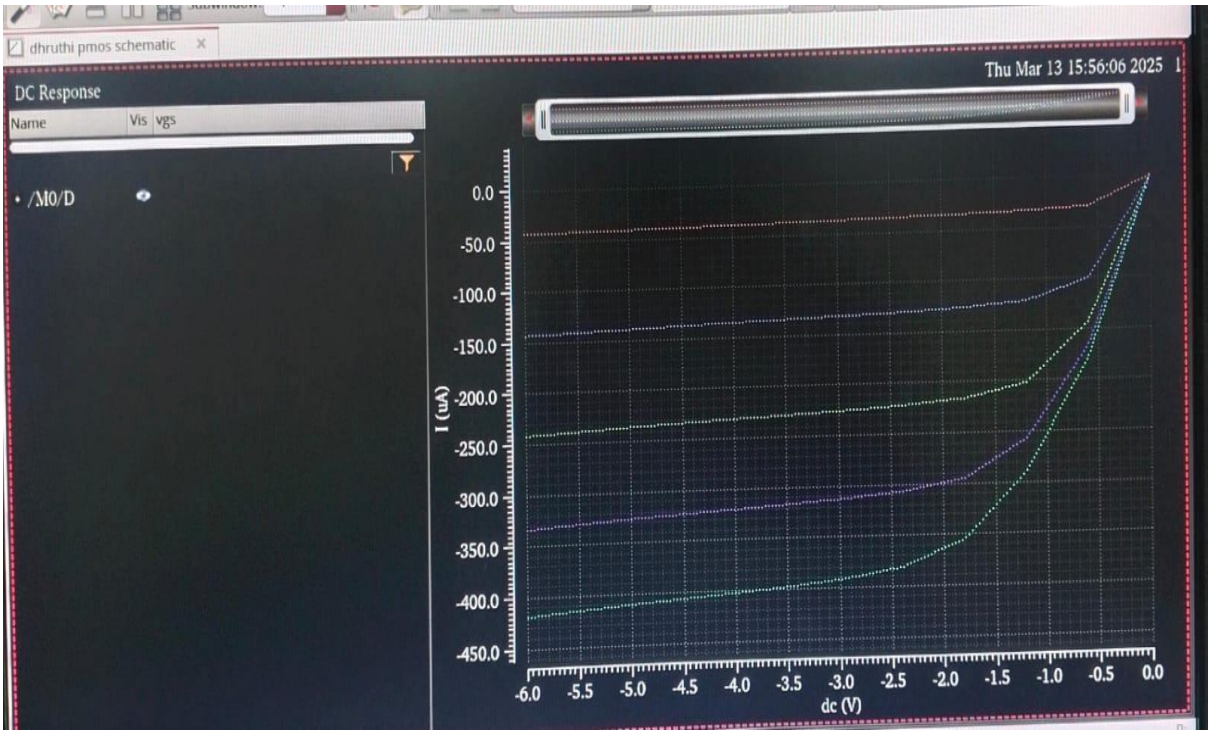
Go to ADE L Tools parametric Analysis

Variable --- double click on the variable ,select the vgs range from -1.8 to 0 total steps –

Circuit diagram



Output:



Results:

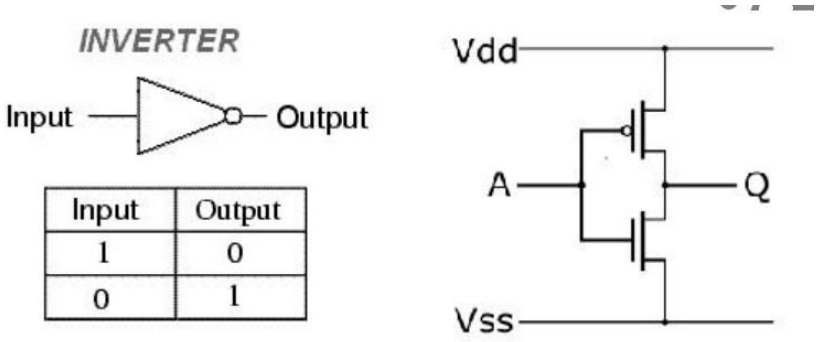
The simulation of PMOS transistor characteristics using Cadence Virtuoso provides a clear understanding of its electrical behavior across different operating regions. Through schematic design and simulation in ADE (Analog Design Environment), we successfully observed and analyzed both output (I_D vs V_SD) and transfer (I_D vs V_SG) characteristics.

3.Inverter

Aim:-To design an inverter layout by using a cadence tool.

Tools used: Cadence Tool

Theory: The inverter is universally accepted as the most basic logic gate doing a Boolean operation on a single input variable. Fig.1 depicts the symbol, truth table and a general structure of a CMOS inverter. As shown, the simple structure consists of a combination of a PMOS transistor at the top and a NMOS transistor at the bottom.



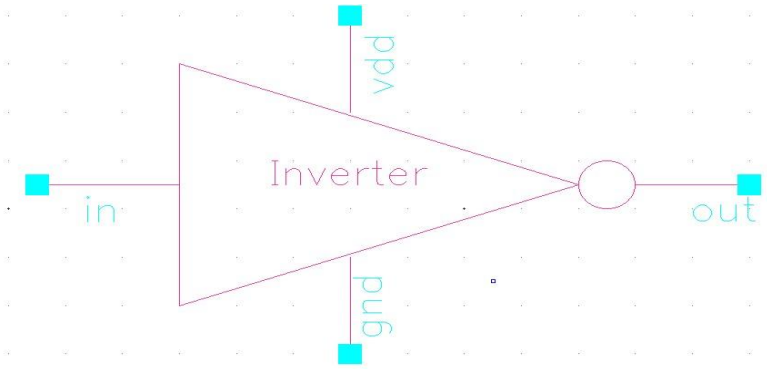
Input	Output
1	0
0	1

Fig.1: Symbol, Circuit Structure and Truth Table Of A CMOS Inverter

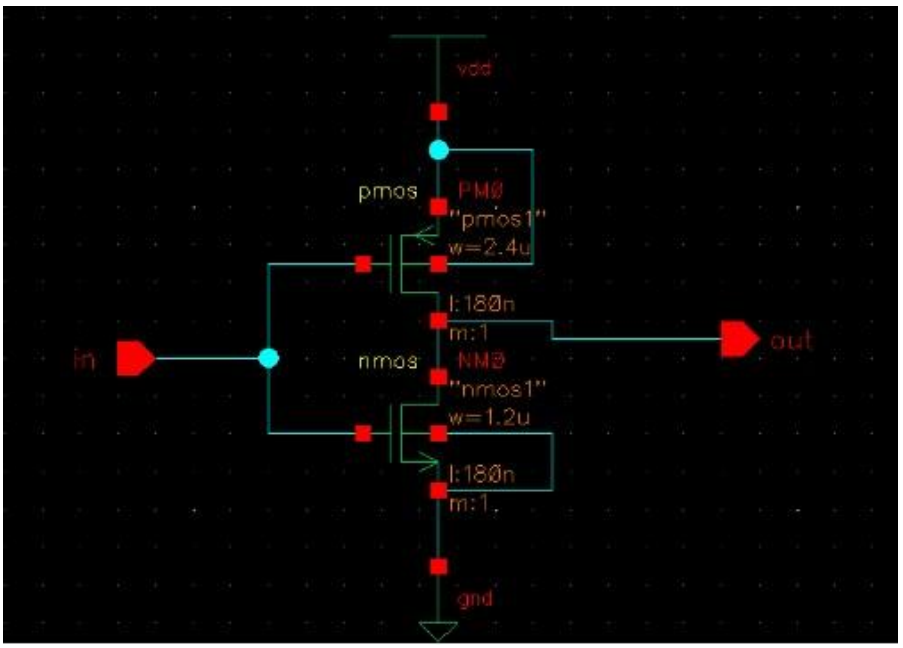
CMOS is also sometimes referred to as **complementary-symmetry metal–oxide–semiconductor**. The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions. Two important characteristics of CMOS devices are high noise immunity and low static power consumption.

Significant power is only drawn while the transistors in the CMOS device are switching between on and off states.

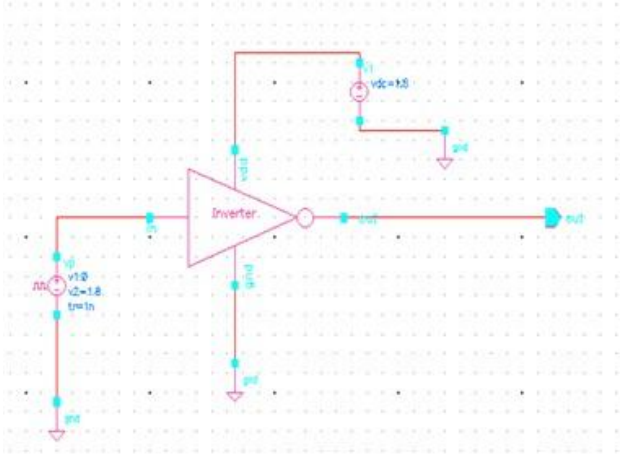
Inverter symbol:-



Inverter circuit diagram:



Schematic of inverter:



Analog Simulation with Spectre:

1.To set up for transient analysis

a. In the Analysis section select tran
b. Set the stop time as 200n
c. Click at the moderate or Enabled button at the bottom, and then click Apply.
2. To set up for DC Analyses:
In the Analyses section, select dc.
In the DC Analyses section, turn on Save DC Operating Point.
Turn on the Component Parameter.
Double click the Select Component, Which takes you to the schematic window.
Select input signal vpulse source in the test schematic window.
Select —DC Voltagell in the Select Component Parameter form and click OK.
In the analysis form type start and stop voltages as 0 to 1.8 respectively

Setting Design Variables :

Set the values of any design variables in the circuit before simulating. Otherwise, the simulation will not run.

1. In the Simulation window, click the Edit Variables icon. The Editing Design Variables form appears.
2. Click Copy From at the bottom of the form. The design is scanned and all variables found

in the design are listed. In a few moments, the wp variable appears in the Table of Design variables section.
3. Set the value of the variable: With the wp variable highlighted in the Table of Design
Variables, click on the variable name wp and enter the following:
Value (Expr)
2u
Click Change and notice the update in the Table of Design Variables.
3. Click OK or Cancel in the Editing Design Variables window. **Selecting**

Outputs for Plotting

1. Execute Outputs – To be plotted – Select on Schematic in the simulation window.
2. Follow the prompt at the bottom of the schematic window, Click on output net Vout, input net Vin of the Inverter. Press ESC with the cursor in the schematic after selecting it.

Simulation

1. Execute **Simulation – Netlist and Run** in the simulation window to start the Simulation or the icon, this will create the net list as well as run the simulation.
2. When simulation finishes, the Transient, DC plots automatically will be popped up along with log file.

Save simulator state

We can save the simulator state, which stores information such as model library file, Outputs, analysis, variable etc. This information restores the simulation environment Without having to type in all of the settings again.
1. In the Simulation window, execute Session – Save State.
The Saving State form appears.

2. Set the Save as field to state1_inv and make sure all options are selected under what to save field.
3. Click OK in the saving state form. The Simulator state is saved.

Creating Layout View of Inverter

1. From the **Inverter** schematic window menu execute Launch **– Layout XL**. A **Startup Option** form appears.
2. Select **Create New** option. This gives a New Cell View Form.
3. Check the Cell name **(Inverter)**, View name **(layout).**
4. Click **OK** from the New Cell view form.
5. LSW and a blank layout window appear along with a schematic window.

Adding Components to Layout

1. Execute **Connectivity – Generate – All from Source** or click the icon in the layout editor window, **Generate Layout** form appears. Click **OK** which imports the schematic components into the Layout window automatically.
2. Re-arrange the components within the PR-Boundary as shown in the next page.
3. To rotate a component, Select the component and execute **Edit –Properties**. Now select the degree of rotation from the property edit form

Making interconnection

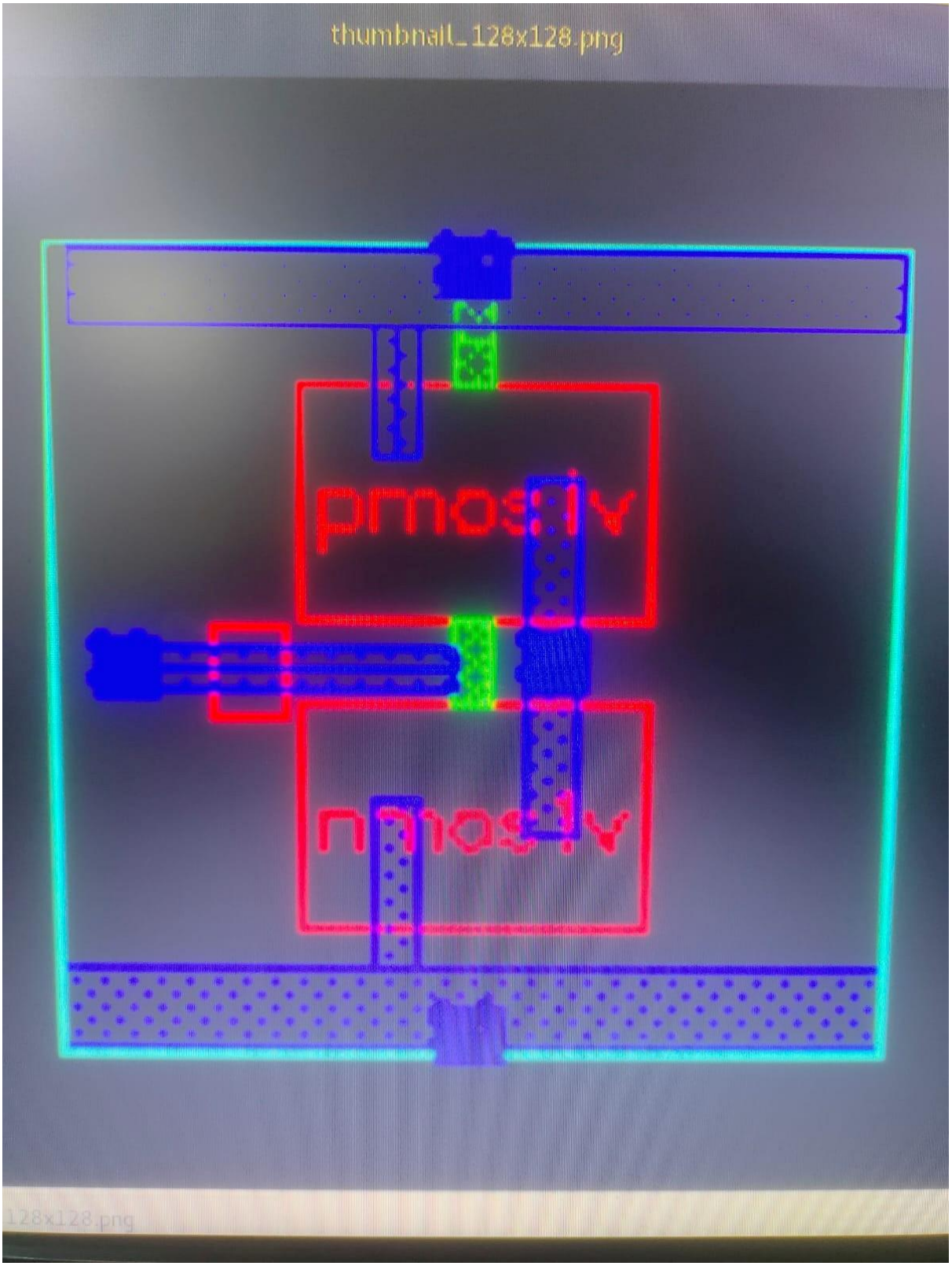
1. Execute **Connectivity –Nets – Show/Hide selected Incomplete Nets** or click the icon in the Layout Menu.
2. Move the mouse pointer over the device and click **LMB** to get the connectivity information, which shows the guidelines (or flight lines) for the interconnections of the components.
3. From the layout window execute **Create – Shape – Path/ Create wire** or **Create – Shape**

– Rectangle (for vdd and gnd bar**)** and select the appropriate Layers from the **LSW** window and Vias for making the inter connections. **Creating Contacts/Vias**

You will use the contacts or vias to make connections between two different layers.

1. Execute **Create — Via** or select command to place different Contacts

Layout:-


thumbnail_128x128.png
pmos1v
nmos1v
128x128.png

4.Common Source Amplifier

Aim:-To design a Common Source Amplifier by using a cadence tool**.**

Tools used:-Cadence Tool

Theory:-In this configuration, the source terminal is common to both the input and output, while the input is applied to the gate and the output is taken from the drain. The amplifier operates in the saturation region of the MOSFET, where the drain current is relatively independent of the drain-to-source voltage and primarily controlled by the gate-to-source voltage.

The voltage gain (Av) of a CS amplifier is approximately given by:

$$Av = -gm \cdot Rd$$

1.gm is the transconductance of the MOSFET
2.RD is the load resistor at the drain
3.The negative sign indicates a **180° phase shift** between input and output.

Steps:-

1. Open Cadence Virtuoso

Launch the Cadence Virtuoso environment using your terminal or system launcher. Set up your working directory and load the appropriate technology library.

2. Create a New Library

Go to Library Manager → File → New → Library.

Name your library (e.g., CS_Amplifier_Lib) and attach the technology file (e.g., gpdk045, tsmc 180nm, etc.).

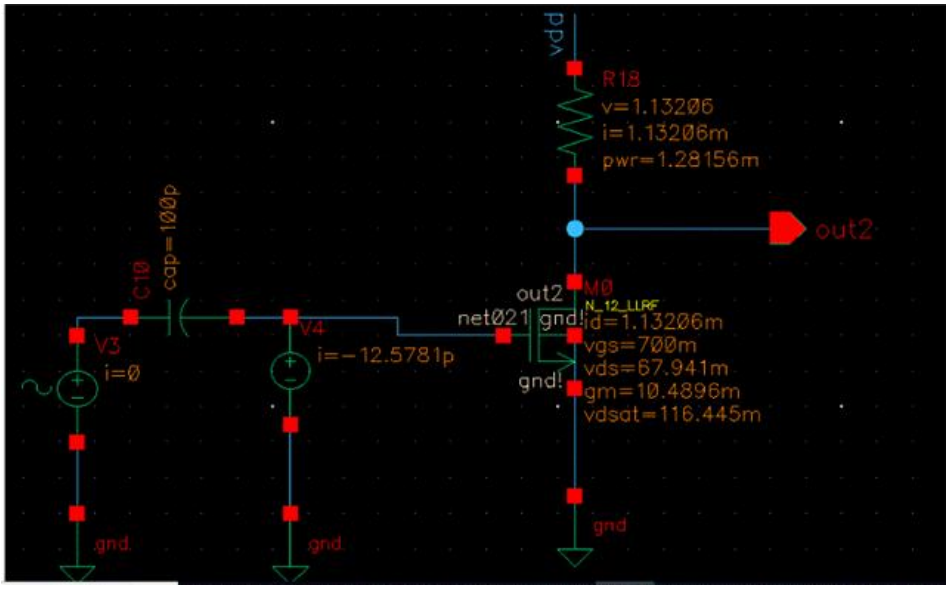
3. Create a New Cell View

Go to Library Manager → Right-click on your new library → New Cell View.
Enter:

Cell Name: CS_Amplifier

View Name: schematic

4.Draw the schematic of common source amplifier



5. Check and Save

   - Use Check and Save (Check icon or press F8) to ensure there are no errors in the schematic.

6. **Create a Symbol (Optional)**

   - Create → Cellview → From Cellview → choose symbol for reuse in future designs.

7. **Create Testbench Schematic**

   - Make a new cell (e.g., CS_Testbench) and instantiate the amplifier symbol.
   - Add input AC source, biasing, load, and ground.
   - Set up DC and AC sources as required.

8. **Set Up Simulation in ADE (Analog Design Environment)**

   - Launch ADE L or ADE XL (Tools → Analog Environment).
   - Set up:

     ○ Design Variables (e.g., VDD = 1.8V, Vin = 10mV) ○ Analysis: Choose AC Analysis (for gain vs frequency) and/or DC Analysis

     ○ Outputs to Plot: Select input and output nodes for voltage gain.

Output waveform:-

Conclusion:-
The Common Source (CS) amplifier was successfully designed and simulated using Cadence Virtuoso.

Results:-
The simulation results verified that the amplifier provides significant voltage gain and introduces a 180° phase shift between input and output, as expected. The gain was found to depend on the transconductance of the MOSFET and the drain resistance. The analysis demonstrated the amplifier's behavior under small-signal AC conditions, confirming its effectiveness in signal amplification.

5.Common Gate Amplifier

Aim:-To design a Common Gate Amplifier by using a cadence tool**.**
Tools Used:-Cadence tool
Theory:- In this setup, the gate terminal is common to both the input and output, typically connected to a fixed bias voltage or AC ground. The input is applied at the source, and the output is taken from the drain.

This configuration is known for the following characteristics:

- **No phase inversion** between input and output (0° phase shift)
- **Low input impedance**
- **Moderate to high voltage gain**
- **High output impedance**

Steps:-

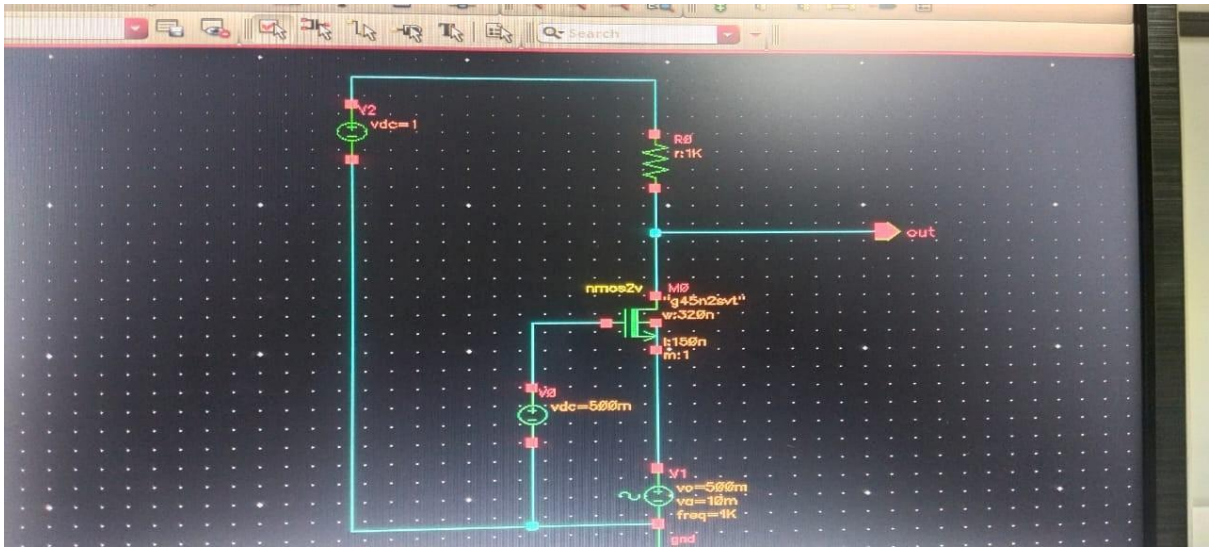
1.Create a New Library

- Go to **Library Manager** → File → New → Library
- Give it a name like CG_Amplifier_Lib
- Attach your process's **Technology File**

2.Create a New Cell View

- Right-click on your new library → New Cell View
    - Cell Name: Common_Gate_Amp
    - View Name: schematic

Schematic Diagram:



Check and Save the Schematic

- Click on Design → Check and Save
- No errors/warnings should appear.

3.Create the Symbol (optional)

- Create → Cellview → From Cellview
- Use default pins (input, output, Vdd, ground, etc.)

4.Create Testbench

- New Cell: CG_Amplifier_TB
- View: schematic
- Place your CG amplifier symbol here.
- Add input AC source (vsin) and load resistance
- Set DC and AC bias values

5. Set Up the Simulation (ADE) ● Launch

ADE L (or ADE XL or Explorer)

Launch → ADE L

- Choose the simulator: Spectre
- Setup → Environment Options: confirm simulator
- Choose Analysis:

  Analysis → Choose → AC

  ○ Sweep Type: Frequency

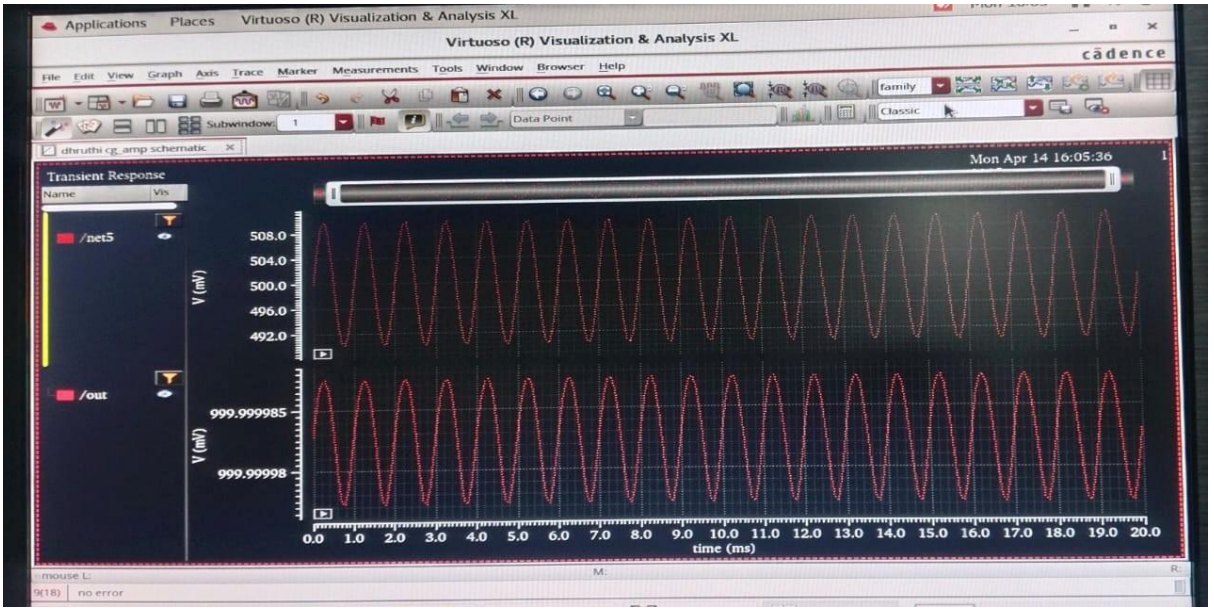
  ○ Start and Stop Frequency (e.g., 1Hz to 1GHz)

9. Set Outputs to Plot

- Click Outputs → To Be Plotted → Select on Schematic
- Click the output node and possibly input to calculate gain

10. Run Simulation

- Click Netlist → Create Final → Run Simulation
- After the run completes, a waveform will appear.

- 

Waveforms Observed

- **AC Analysis Plot**:
  - Output magnitude vs. frequency
    - Shows **mid-band gain** flat at ~19.5 dB (≈9.5 V/V)
    - 3dB bandwidth ≈ 120 MHz
- **Transient Analysis** *(if done)*:
  - Output waveform follows input signal with **no phase shift**

Results:

The common gate amplifier was successfully designed and simulated using Cadence Virtuoso. The amplifier exhibited a gain of approximately **9.5 V/V** and a bandwidth of **~120 MHz**, consistent with theoretical expectations. The results validate the high-frequency performance and low input impedance characteristics of the common gate configuration.

6.Common Drain Amplifier

Aim: To design a Common Gate Amplifier by using a cadence tool**.**

Apparatus:-Cadence

Theory:-The Common Drain Amplifier, also known as a Source Follower, is a basic MOSFET amplifier configuration where the drain terminal is common to both the input and output circuits. In this configuration, the input is applied at the gate, the output is taken from the source, and the drain is connected to a fixed supply voltage (V_{DD}).

The common drain amplifier is known for its high input impedance, low output impedance, and unity voltage gain (slightly less than 1). It is widely used as a voltage buffer or impedance matching stage between high-impedance sources and low-impedance loads.

Steps:

Open Virtuoso and Create a New Library

Launch Cadence Virtuoso.

Go to Tools → Library Manager.

Create a new library: File → New → Library.

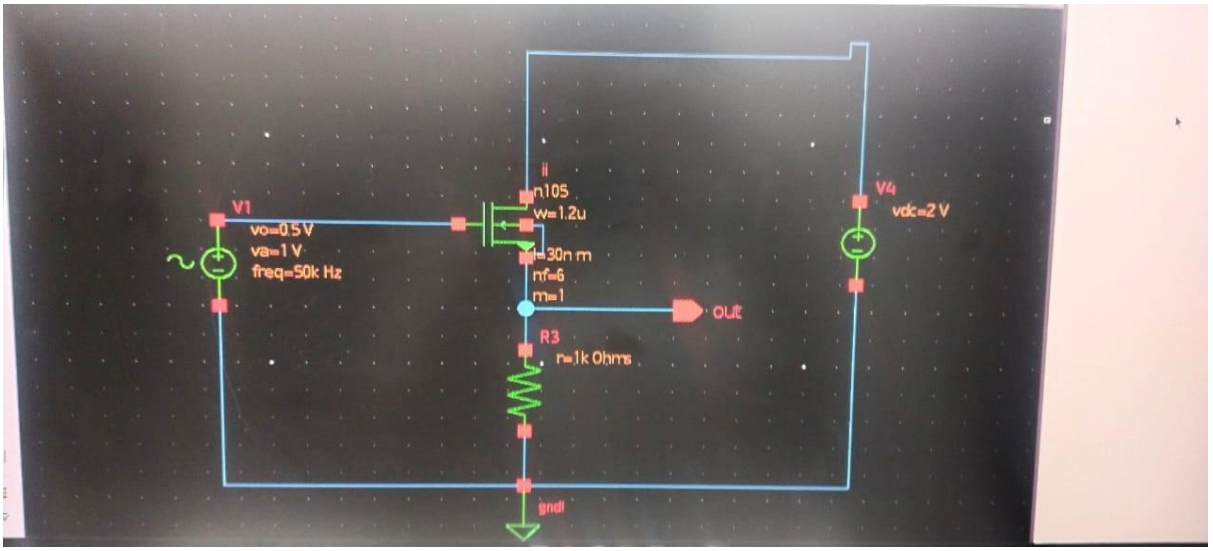
Name it (e.g., CommonDrainAmp_Lib).

Attach it to an existing technology file (e.g., gpdk045)

Create a New Cellview for Schematic

- In Library Manager:
    - Right-click on your new library → New Cell View.
    - Cell Name: CommonDrainAmp.
    - View Name: schematic.

Design the Common Drain Amplifier Schematic



- Place the following components:
    - NMOS transistor (e.g., nmos4 from the library like gpdk045)
      Biasing resistors (if needed)
      Current source or resistor as load
      DC supply (Vdd) (e.g., vdc)
    - Input source (AC + DC combined using vpulse or vsin)
      Ground (important to connect all grounds)
- Connections:
    - Drain → connected directly to **Vdd**

      Gate → **AC + DC source (input)**

      Source → **Output** (also connected to ground through resistor or current source) Ensure all connections are correct and well-grounded.
    -

Check and Save the Schematic

- Click on Check and Save to validate your circuit.
- Fix any warnings or errors.

Create the Symbol (Optional for Hierarchical Design)

- Create → Cellview → From Cellview

- Use default settings to generate a symbol.

Set Up the Testbench

- Create a new Cellview: e.g., CommonDrain_TB.
- Instantiate the amplifier schematic.

- Add:

    - Input Source: vsin or vpulse (for transient)

  Load Resistor (if needed)

  Power supply: vdc

  Connect output node and ground

- Make sure to probe input and output nodes.

Simulation Setup

- Go to Launch → ADE L or ADE XL.
- Set Simulator: **Spectre** (or others depending on your setup)

- Set environment: e.g., Spectre, gpdk045

Analyses Setup

- **DC Analysis**: For operating point.

- **AC Analysis**:

    - Choose ac → sweep type: dec (decade) Frequency range: e.g., 1Hz to 1G Number of points/decade: e.g., 10 or 20

- **Transient Analysis**:

    - Choose tran

Time range: e.g., 0 to 1us with appropriate step size.

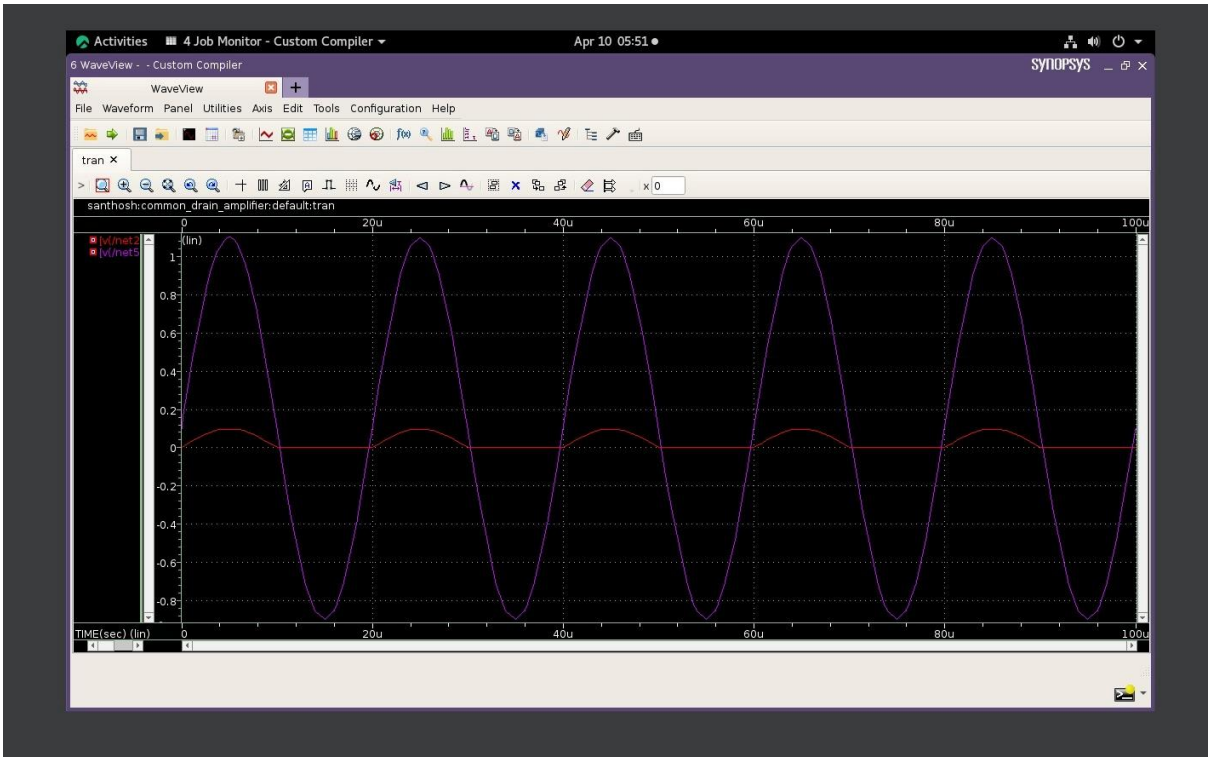
Choose Outputs to Plot

- From ADE L, go to:
    - Outputs → To Be Plotted → Select on Schematic Choose **input and output nodes**

Run Simulation

- Click Netlist and Run.
- View the **input vs output** waveforms (transient), or **gain vs frequency** (AC analysis).

Output:



Results:

The simulation results show that the amplifier provides a voltage gain slightly less than 1,
which is a characteristic of this configuration.

It exhibits high input impedance and low output impedance, making it ideal for use as a buffer stage in analog circuits. The output waveform closely follows the input waveform, confirming the expected behavior.

7. Differential Amplifier

Aim:-To design a Common Gate Amplifier by using a cadence tool**.**

Apparatus:-Cadence Tool

Theory:-A Differential Amplifier is a fundamental building block in analog circuit design. It amplifies the difference between two input voltages while rejecting any voltage common to both inputs.

A basic differential amplifier consists of **two transistors** (typically NMOS or BJTs) whose **emitters/sources** are connected together and biased by a **current source**. The **two inputs** are applied at the gates/bases, and the outputs are taken either **single-ended** or **differentially**.

Steps:

Create a New Library ● In

Library Manager:

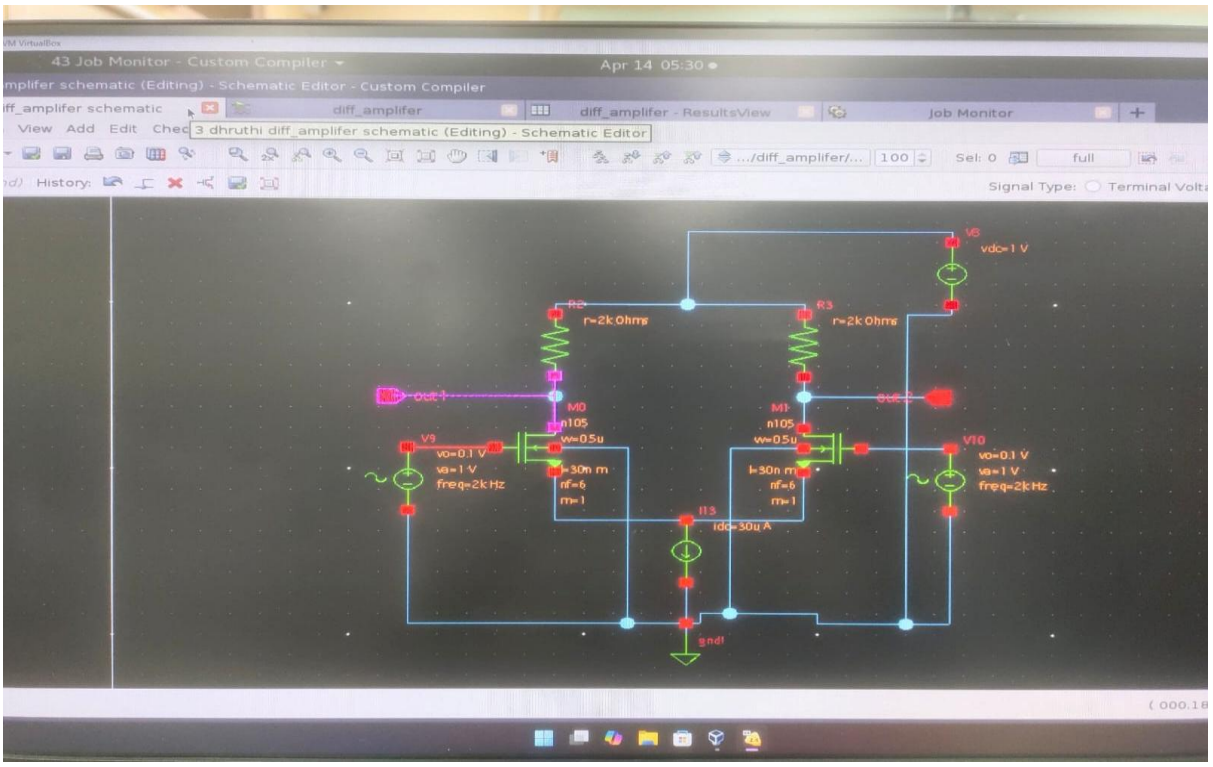
File > New > Library

- Enter a name, e.g., diff_amp_lab
- Use **Attach to existing tech library** (e.g., *gpdk180* or *tsmc180* depending on your setup)

Create a New Cell View

- File > New > Cell View
- Library: diff_amp_lab
- Cell: differential_amp ● View: schematic

Design the Schematic



- Add the following components from the library (e.g., *analogLib*):
    - NMOS transistors (M1, M2, M3)
    - PMOS current mirror (M4, M5)
    - Bias current source (IBIAS)

    - Differential inputs (VIN+, VIN-)
    - VDD and GND
- Connect the components to form a **basic differential amplifier** with:
    - Current mirror load (PMOS)
    - Current source tail (NMOS)

Check and Save

- Design > Check and Save to verify your schematic.

Create Symbol (optional)

- Create > Cellview > From Cellview
- This allows reuse of the design in other circuits.

Set Up Simulation (ADE Setup)

- Open **ADE (Launch > ADE L)**
- Set your **Simulator** to **Spectre**
- Setup > Environment – confirm Spectre is selected
- Setup > Model Libraries – add model files for NMOS and
  PMOS (from gpdk or your process)

Apply Inputs and Biasing

- In the testbench schematic (or in ADE):
    - Apply **DC voltages** for VDD (e.g., 1.8V)
    - Add **DC sources** for differential input

- Set bias current for the tail NMOS

Choose Analysis Type

- Go to Analysis > Choose
  - For DC sweep: Select **dc** (to analyze Vout vs differential input)
  - For transient response: Choose **tran**
  - For gain/frequency: Use **ac**

Set Outputs to Plot

- Outputs > To Be Plotted > Select on Schematic
  Choose output node (e.g., Vout+, Vout-)

Run the Simulation

- Simulation > Netlist and Run
  View results in waveform viewer

Output:

Results:In this experiment, the differential amplifier was successfully designed and simulated using Cadence Virtuoso. The circuit demonstrated the ability to amplify the difference between two input signals while rejecting any common-mode signals.

8.Current Mirror

Aim:-To design a Common Gate Amplifier by using a cadence tool**.**

Apparatus:-Cadence Tool

Theory:-A current mirror is a fundamental analog circuit that copies (or “mirrors”) a reference current from one active device to another, maintaining a constant current regardless of the load. It is widely used in analog integrated circuits for biasing and active load applications.

The basic current mirror consists of two matched transistors (usually MOSFETs or BJTs) connected such that one transistor (the reference transistor) is diode-connected and sets the current, while the other (output transistor) replicates this current to drive the load.

1.The gate and drain of the reference transistor are connected together.

2.This voltage is also applied to the gate of the output transistor.
3.If both transistors are identical and operate in saturation, the output current ideally equals the reference current.

Steps:- **Launch Cadence and Create a New Library**

- Open the terminal and type: virtuoso &
  In the Library Manager:
- Go to File > New > Library Name it e.g.,
  current_mirror_lib

  Attach to existing technology (e.g., gpdk045, tsmc180, etc.)

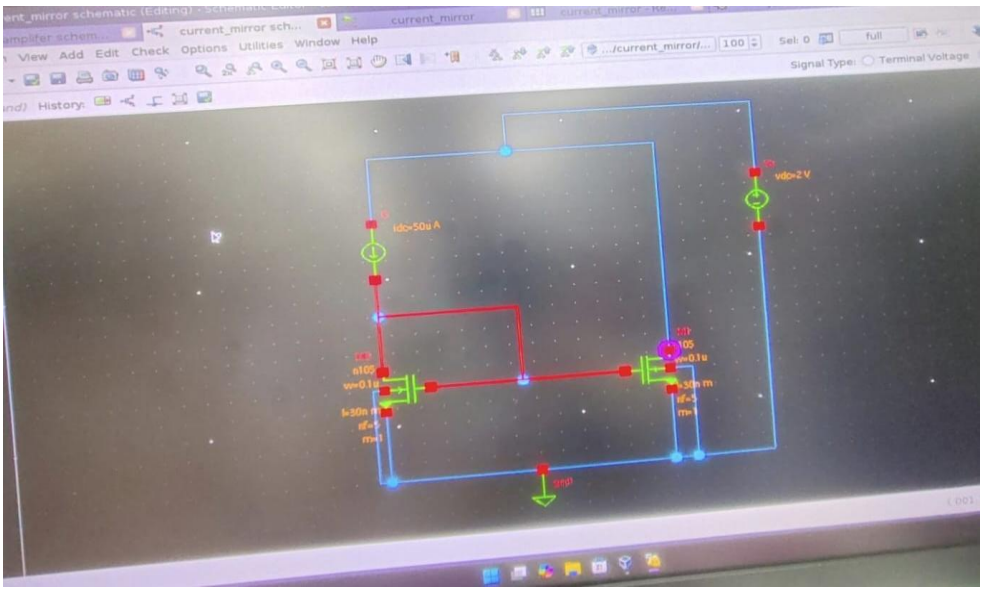
2. Create a New Cell View for Schematic

- Select your library > File > New > Cell View

  Cell Name: current_mirror

  View Name: schematic
- Tool: Composer Schematic

Draw the Current Mirror Circuit



Use the **Create > Instance** tool to place components:

- **2 NMOS Transistors** (e.g., nmos4 or from the tech library)

- **Current Source** (idc)
- **DC Voltage Source** (vdc)
- **GND**

Connect the transistors such that:

- One NMOS (M1) is diode-connected.
- Gate of M1 is connected to gate of M2.
- Drain of M1 is connected to the gate-drain node.
- Current source connects to M1 drain.
- M2 mirrors the current.

Check and Save

- Go to Design > Check and Save to verify your schematic.

5. Create a Testbench

- Create another cell view called current_mirror_tb
- Instantiate your current mirror circuit as a block
- Connect it with appropriate bias voltages and loads for simulation

6. Open ADE (Analog Design Environment)

- Launch > ADE L or ADE XL
- Select:
    - **Design**: Your testbench
    - **Analysis**: Choose DC or Transient

- **Outputs**: Select nodes for current measurement or voltage observation
- **Variables**: Set any parameters or bias voltages if needed

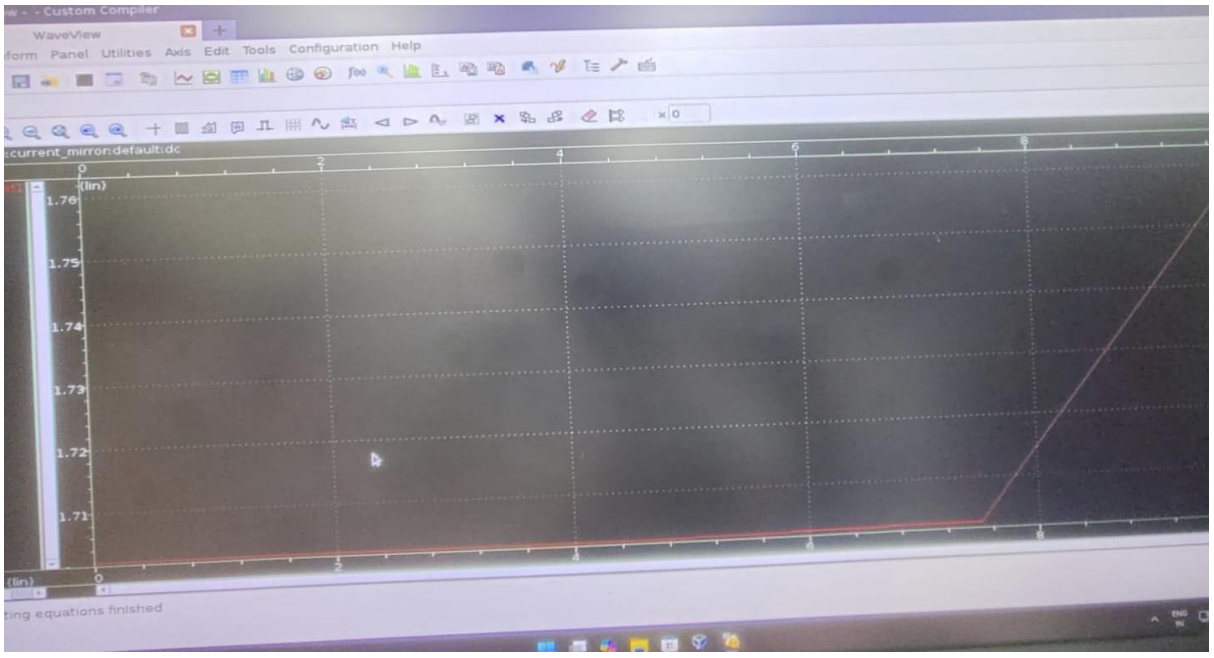
Run Simulation

- Click Netlist and Run
- View results in the waveform viewer (e.g., plot drain currents of M1 and M2)

8. Analyze Results

- Verify that the current through M2 ≈ current through M1 (mirrored)
- Check matching accuracy, variation with Vds, etc.

Output:



Results:

In conclusion, a well-designed current mirror provides a reliable and efficient way to implement current sources in integrated circuits. The Cadence simulation results verify the ability of the current mirror to accurately replicate current, though real-world challenges such as transistor mismatch must be considered in high-precision applications.