

## CERTIFICATE OF TRAINING COMPLETION

This certifies that

**Y.Dhruthi**

has successfully completed the training in

**VLSI RTL Design & Verification Using Synopsys Tool**



Period of Training From: **21-07-2025** To: **25-07-2025**

During this period she has gained expertise on the following:

- Understanding ASIC Design Flow
- Design and Verify Asynchronous FIFO with Verilog
- Master Lint, CDC, and UPF Concepts
- Develop TB Components and Achieve Coverage.
- Set Up SV and UVM TB for Asynchronous FIFO
- Hands-on Labs



**26-07-2025**

Issue Date



Signature