# High Speed and Ultra Low Power Design of Carry-Out Bit of 4-Bit Carry Look-Ahead Adder

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***Abstract*— A new carry generation scheme for carry out bit of a 4-bit carry look-ahead (CLA) adder is presented. To analyze performance, proposed design for carry-out bit was implemented and verified in Cadence Virtuoso environment in 90nm technology. Performance parameters were compared with the conventional design of carry-out bit of 4-bit CLA adder. The proposed design achieved 19.69% improvement in propagation delay over the conventional CLA design. Due to low transistor count and low dynamic power dissipation, an improvement of 75.973 % was achieved in average power consumption over the conventional carry-out bit of CLA design. As a result, the obtained improvement in PDP was 79.003 %. Due to enhancements in performance parameters and reduced transistor count, the proposed CLA carry-out bit is expected to have extensive impact on overall adder performance.**

**Keywords—c4-bit adder, carry-out bit, carry generation, carry look-ahead, low power.**

## I. INTRODUCTION

Performance and power consumption are crucial parameters for modern complex integrated circuits. High-performance, area-efficient and low-power consuming systems are rapidly gaining importance in devices such as mobile and portable devices, bio-medical instruments, digital signal processing systems and wireless receivers which have limited area and power budget but require fast computing [1], [2]. Adders play the most important role in arithmetic and logic units (ALUs) because subtraction, multiplication and division operations require adders to compute result [3]-[5]. Hence, design of an efficient adder improves the entire performance of ALU.

In order to cope up with the power and speed requirement, various design methods for full adder have been developed [6] The simplest way of adding binary numbers can be done using Ripple Carry Adder (RCA) [7]. But RCA is quite inefficient since output of one step relies on the output from preceding step. Therefore, carry propagation is an important factor as it limits the performance of adders.

Utilization of speedy gates may bring about positive change in delay. However, physical components are not ideal. Therefore, speed can be obtained to a specified level by utilizing fast gates [8], [9]. Utilizing components in optimized manner enhances performance. Several types of adders employing various methods have been developed to reduce the carry propagation time [10]-[12]. Recently, approximate adders have gain interest in case of error tolerant applications which enhance circuit performance by trading off accuracy [13], [14]. CLA adder reduces delay by generating all the carry bits at a time using the input bits. Therefore, carry terms for the most significant bits (MSB) need not to wait for the least significant bits (LSB) to propagate [15].

Many design processes employ 4-bit adders as an elementary building block to design wide adders [16], [17], [18]. Therefore, the performance of carry out bit plays a key role in wide adders because carry out bit of one block is used as input in next block. Hence, performance level of carry out bit of 4-bit adders should be enhanced in order to achieve fast adding operation.

## II. CONVENTIONAL DESIGN OF 4-BIT CLA

CLA method employs the technique of generating carry bits all at a time to reduce delay [15]. If we denote S as sum, C as carry, and A, B as the input bits, then sum and carry bit using CLA method can be expressed as:

$$S_i = P_i \oplus C_i$$

$$C_{i+1} = G_i + P_i C_i$$

Where,

$$P_i = A_i \oplus B_i$$

$$G_i = A_i B_i$$

According to [17], conventional design of carry out bit of 4-bit CLA method can be represented as:

$$C_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0$$

Where

$$C_0 = \text{input carry bit}$$

$$C_4 = \text{output carry bit}$$

According to [19], complete schematic of the of carry-out bit $C_4$ including the AND gates and the XOR gates is represented by Fig. 1.

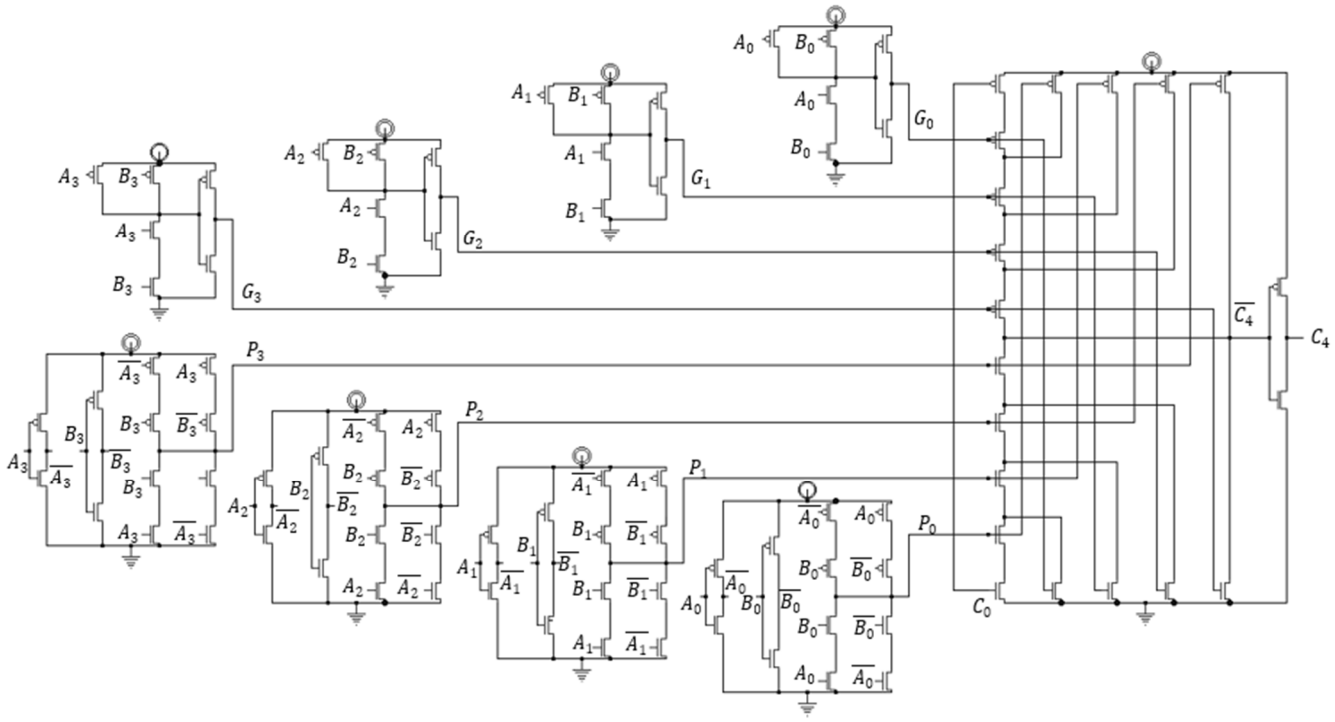


Fig. 1. Conventional design of carry-out bit $C_4$.

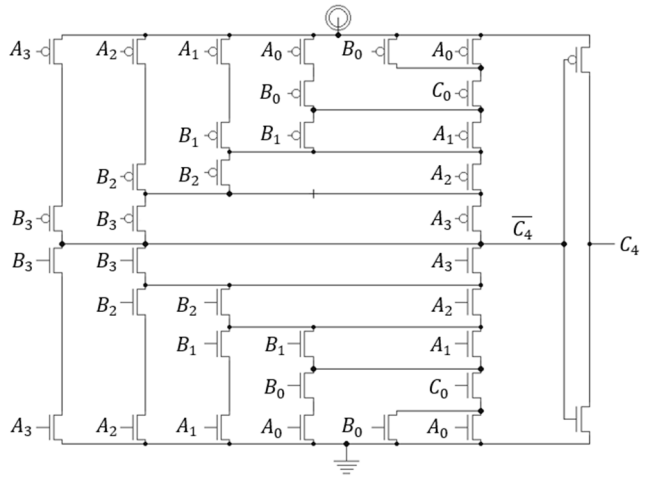


Fig. 2. Proposed design of carry-out bit $C_4$.

## III. Proposed Design of Carry-Out Bit

To design the proposed circuit, at first, we have generated the truth table for carry bits $C_1$, $C_2$, $C_3$, $C_4$ by using the input bits in the sequence-$B_3$, $A_3$, $B_2$, $A_2$, $B_1$, $A_1$, $B_0$, $A_0$, $C_0$. Here, $B_3$ and $A_3$ are the MSBs and $C_0$ is input carry. By using the truth table, carry bits $C_1$, $C_2$, $C_3$, $C_4$ can be expressed as the following simplified sum of products:

$$C_1 = C_0(A_0 + B_0) + B_0A_0 \quad (1)$$
$$C_2 = C_1(A_1 + B_1) + B_1A_1 \quad (2)$$
$$C_3 = C_2(A_2 + B_2) + A_2B_2 \quad (3)$$
$$C_4 = C_3(A_3 + B_3) + B_3A_3 \quad (4)$$

With careful observation of (1), (2), (3), and (4), we can see that each carry-out equation $C_i$ works as a base for the subsequent carry-out term $C_{i+1}$. Therefore, to design the n-channel Field Effect Transistor (nFET) network for carry bit $C_2$, nFET network for carry bit $C_1$ needs to be utilized.

Now, to obtain the nFET network for $C_2$, two series connected nFETs are parallelly connected with the nFET network of $C_1$. To complete the design, two parallelly connected nFETs are connected in series with this circuit. In the same way, nFET network for carry terms $C_3$ has been generated. Finally, applying same technique, nFET network for $C_4$ has been obtained using nFET network of $C_3$.

In case of designing the proposed carry-out bit, a mirror equivalent circuit has been used for pull-up network (pFET network) which provides more symmetrical layout. Structure of pull down network (nFET network) and pull up network (pFET network) in mirror circuit are exactly the same [20]. Complete schematic of the carry-out term $C_4$ is represented by Fig. 2.

Transistor count for proposed and conventional carry-out bit design is presented in Table I.

TABLE I
TRANSISTOR COUNT

| Design | Transistor count |
|---|---|
| Conventional | 92 |
| Proposed | 36 |

## IV. Simulation Result and Performance Analysis

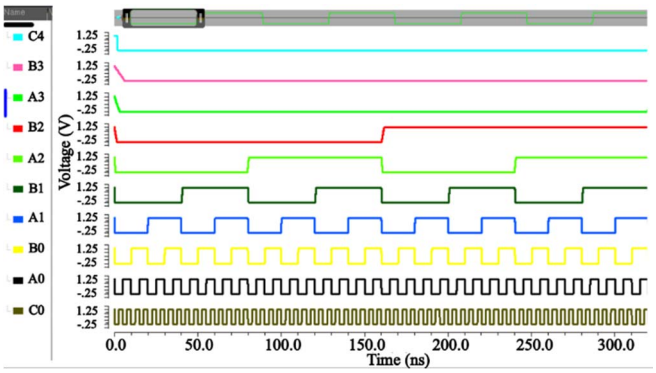
Simulation result is expressed in details in the following sub-sections.

### A. Propagation Delay:

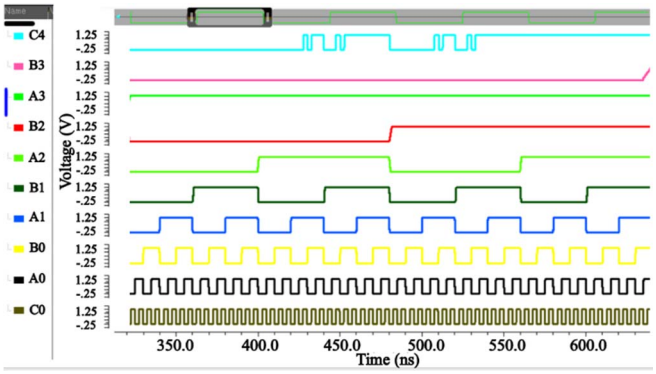
Simulation results of propagation delay for proposed design and conventional CLA design are listed in Table II.

TABLE II
SIMULATION RESULT FOR PROPAGATION DELAY

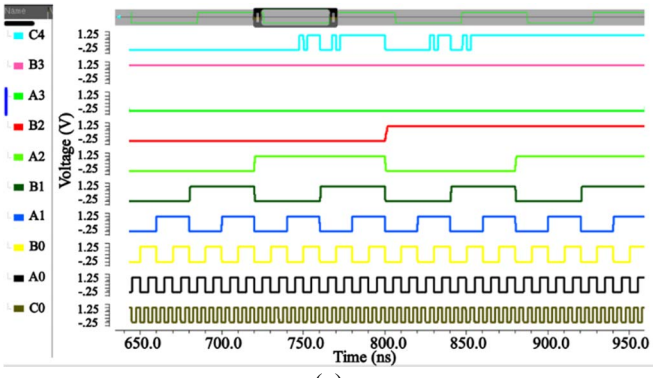
| Design | Delay (ps) | Improvement |
|---|---|---|
| Conventional | 166 | 19.277% |
| Proposed | 134 | |



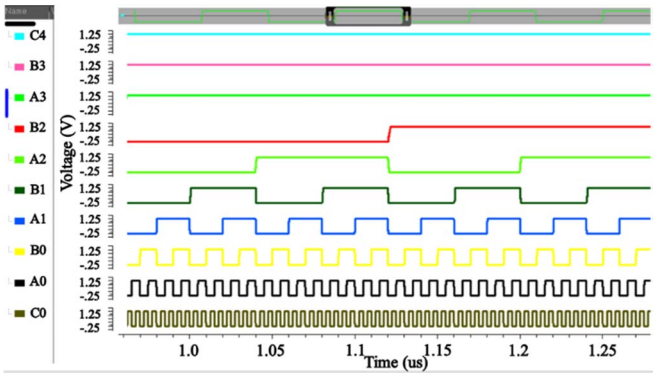

(a)




(b)




(c)




(d)

Fig. 3. (a) Output graph for input combination from 000000000 to 001111111. (b) Output graph for input combination from 010000000 to 011111111. (c) Output graph for input combination from 100000000 to 101111111. (d) Output graph for input combination from 110000000 to 111111111.

*B. Power Dissipation:*

According to [21], power in a logic gate be expressed as:

$$P = V_{DD} I_{DDQ} + C_{out} V_{DD}^2 f \quad (5)$$

Where

$$V_{DD} = supply\ voltage$$

$$I_{DDQ} = leakage\ current$$

$$C_{out} = load\ capacitance$$

$$f = frequency\ of\ input\ signal$$

The term $V_{DD} I_{DDQ}$ in (5) represents DC power. It occurs due to the leakage current of the transistors. The term $C_{out} V_{DD}^2 f$ represents Dynamic Power. It occurs due to dynamic switching events.

*1) DC Power Dissipation*

The leakage current is in a MOSFET is quite small (usually in the order of pico-ampere per transistor). Therefore, the value of DC power is quite small. Since, the conventional carry-out circuit requires more transistors than the carry-out circuit design presented in this paper, DC Power for the conventional design is more as well.

*2) Dynamic Power Dissipation (DPD)*

Dynamic power in logic gate is the dominating factor in case of power loss. If we look at Fig. 3(a), we can see that output bit $C_4$ remains to logic 0 even if the input combination keeps changing. Therefore, no current flow occurs from power source to ground. As a result, there is no DPD for the input combinations in Fig. 3(a) for the proposed design. For the same reason, no DPD happens for the proposed design for input combinations of Fig. 3(d) because the output remains at logic 1. Now, if we consider Fig 3(b) and Fig. 3(c), we can see transitions are happening as output changes from logic 0 to logic 1 and then again back to logic 0. This causes dynamic power dissipation.

On the contrary, conventional CLA design dissipates power for every change in input combination. It happens because inputs to the XOR gate consist of inverters and an inverter change its output if the input signal is changed. Moreover, based on the change in input combinations, transitions occur in AND gates and XOR gates which make them dissipate dynamic power. In addition, the complex logic also dissipates dynamic power whenever transition occurs.

Now, based on the discussion, we have observed that the proposed design consumes no dynamic power for input combinations in Fig. 3(a) and Fig. 3(b), which consist 50% of the input combinations. On the other hand, the conventional CLA design consumes dynamic power for every change in input combination. Therefore, power loss in proposed design is supposed to be quite lower than the power loss in conventional design.

To get a clear view of the power dissipation, simulations were performed in Spectre and power graph was plotted for all the input conditions. Fig. 4 represents the power graph for proposed design and Fig. 5 represents the power graph for conventional design. The topmost waveforms (blue colored) of Fig. 4 and Fig. 5 depicts power dissipation according to input combinations.

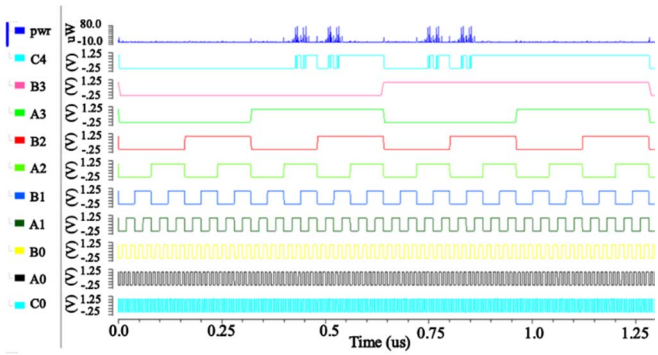



Fig. 4. Power graph of proposed design.

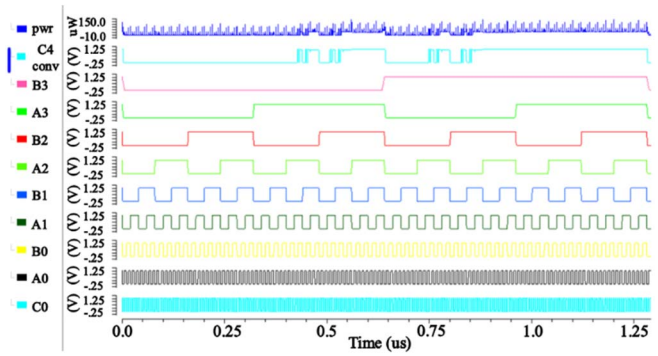



Fig. 5. Power graph of existing design.

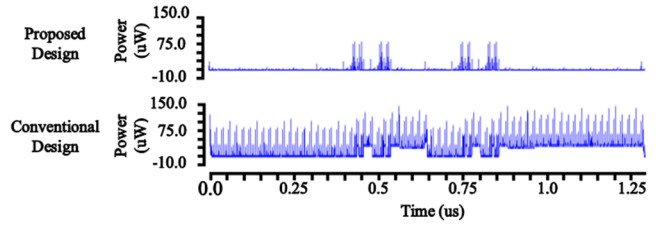



Fig. 6. Waveform of power dissipation for proposed design and conventional design.

*3) Average Power*

Average power for proposed design and conventional design were calculated using Calculator option in the waveform window.

TABLE III
AVERAGE POWER

| Design | Power (µW) | Improvement |
|---|---|---|
| Conventional | 16.44 | 73.739 % |
| Proposed | 4.28 | |

## C. Power Delay Product (PDP)

PDP represents average energy absorbed or consumed by a logic circuit for every switching event. PDP for proposed and conventional design are listed in Table IV.

TABLE IV
PDP OF PROPOSED DESIGN AND CONVENTIONAL DESIGN

| Design | Power (fJ) | Improvement |
|---|---|---|
| Conventional | 2.729 | 79.004 % |
| Proposed | 0.573 | |

## V. CONCLUSION

In this article, design of carry-out bit of 4 bit adder has been proposed and its performance analysis has been done. To compare the proposed circuit with the conventional CLA circuit, Cadence Virtuoso tools were used to carry out simulation in 90nm technology. The proposed design of the carry out bit offered significant improvement in speed and power over the conventional CLA design. An improvement of 19.6856% has been achieved for propagation delay. The most significant improvement has been achieved in case of average power which is 75.973%. As a result, 79.003% improvement in PDP has been obtained.

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