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Design an Area Efficient Kogge Stone Adder using Pass Transistor Logic

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Abstract- **In recent technologies of Electronics applications, Adder is an important source of any devices such as DSP, VLSI applications. For which, many electronics application devices used the high speed adders namely Parallel Prefix Adder (PPA). Generally, PP Adders have less delay due to its less waiting time of carry for next addition. But the area consumption is more, in which the performance of the adders will decrease for higher order bits' addition. This paper is to design an area efficient Kogge Stone PPA which performs the parallel arithmetic operations in CMOS applications and analysed the design based on the parameters like area and power individually. The proposed area efficient KSA design used the Pass Transistor Logic (PTL) and analysed the performance of particular design. The Performance results of PTL with PP-KSA design used the reduce number of MOS devices which yields less area consumption compared to basic design of 4-bit PP-KSA. Entire analysis results of these designs can be done in Microwind CMOS tool.**

Keywords – Pass Transistor Logic, Kogge Stone Adder, Area consumption, Very Large Scale Integrated design, Parallel Prefix Adder, Microwind.

I. INTRODUCTION

To attain a well organised mathematics basic operations like Addition, Subtraction, Division and Multiplication which are used in Digital Signal Processing and VLSI applications; preferred high speed parallel design algorithm [13]. In previous works, the fundamental addition operations are calculated by the use of various binary (logic 0's & 1's) carry adders [17] such as Carry Skip (CS), Ripple Carry (RC), Carry Select (CSL), Carry Save (CSA) and Carry Look Ahead (CLA) Adders etc. The basic binary adders are half adder and Full Adder. All binary cascaded adders are built by full Adder. A 4-bit RCA design requires 4 full adders to do the addition process. Each full adder have to wait once the before full adder process is completed.

Due to applied of these carry binary adders, the design yields the high power consumption and low speed of operation. Because every output carry value is needed for proceeding successive Full adder in cascade binary adders. In the carry save adder, the area consumption and power consumption is more, since every outcome value of full adder is saved before next processing. To recover the high delay problem, the DSP and VLSI-CMOS applications used the high speed Parallel Prefix Adder [4]. The Parallel Prefix Adders design is same as the Carry Look ahead adder. Normally the Parallel Prefix Adders have provided the quick and fast CMOS design applications with minimum power consumption [9]. In Earlier days, the several PPA like Brent Kung Adder – BKA, Ladner Fischer Adder – LFA, Kogge Stone Adder - KSA were designed [2].

The performance of the design can be examined on the aspects of delay, area and power in previous research paper [11]. From compared analysis results of Parallel Prefix Adders given that the (PP-KSA) produced less delay and low power than PP-LFA and PP-BKA clearly. But the area consumption of the Kogge Stone Parallel Prefix Adder design can be increased [5]. To achieve an area efficient PP-KSA, the proposed design used the pass transistor logic in DSP and VLSI-CMOS technologies [10].

This research paper is structured as follows, in section 2; defined the basic design of Kogge Stone Parallel Prefix Adder, in section 3; it explained the design of Kogge Stone Parallel Prefix Adder with proposed Pass Transistor Logic, in section 4; it described the compared results of performance analysis of both designs, the last section is concluded with the performance evaluation results and discussion.

II. DESIGN OF KOGGE STONE ADDER WITH BASIC ALGORITHM

The Digital Signal Processing and VLSI-CMOS digital electronics applications used the Parallel Prefix Adder due to its high speed performance of arithmetic operations [14]. In the Parallel Prefix Adders, initially the carry value is measured for both 0's and 1's inputs by parallel manner [3]. Because of this, the timing constraints of operations are less and didn't wait for carry value in further sum calculation. The Parallel Prefix Algorithm mainly consists of three basic steps which are Pre computation [15], Carry generation, and Post computation. In the initial step, Propagation (P) and generation (G) values are measured based on the given values of 0's and 1's. In the Carry generation stage [1], CG and CP values are measured by the use of pre computation results [16]. In the last step, the final sum and carry out values are measured by the previous step results [7].

The basic 4 bit PP-KSA design [8] used the XOR logic function of propagation and previous carry values to yield the sum output separately. The propagate functions (P) and Generate functions (G) are measured by the equation (1).

$$P[i] = X[i] \oplus Y[i] \quad (1)$$

$$G[i] = X[i] \bullet B[i] \quad (2)$$

In the equations (1), X and Y are the given input signals which are computed by logic gate XOR function. In the equations (2), X and Y are the given input signals which are computed by logic gate AND. The sample sum calculations are given in equation (3) & equation (4).

$$\text{Sum}[0] = \text{Propagation}[0] \text{ XOR Carry in}; \quad (3)$$

$$\text{Sum}[1] = \text{Propagation}[1] \text{ XOR Carry}[0]; \quad (4)$$

The 4 bit design of PP- KSA with basic Parallel Prefix algorithm using Microwind tool is given below

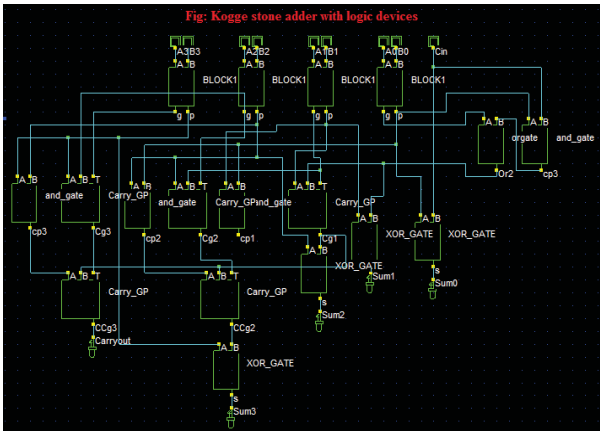

Fig. 1. PP-KSA design with basic PPA algorithm

Here the design used the 4 input bits as A [0:3], B [0:3] and Cin; Here both generation and propagation calculations are done in parallel manner so that it helps to minimize the area consumption of adder design and propagation delay completely based upon the size of the bit which is preferred at the input. The design is performed with the normal logic gates like OR, AND, XOR. In OR logic gates [6], whenever anyone input have high (1), then the output automatically turns to high (1). The OR logic gate used in PP-KSA is given in Fig.2.

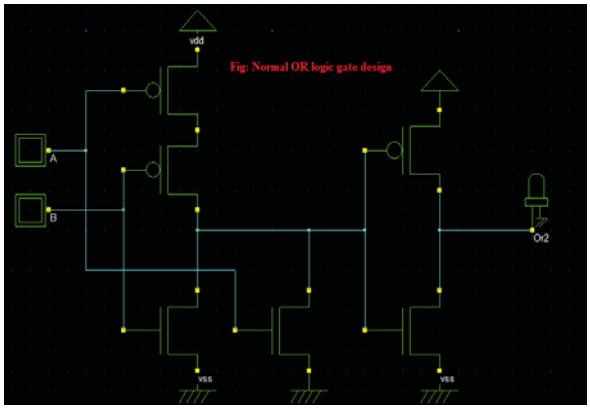

Fig. 2. OR logic gate used in basic PP-KSA design

III. PP-KSA DESIGN WITH PROPOSED PASS TRANSISTOR LOGIC

As discussed in previous works, the 4-bit PP-KSA provides better performance compared to other Parallel Prefix Adders due to low delay operation [12]. In this section, explained the 4 bit Kogge Stone Adder design with proposed Pass Transistor logic operation. The proposed Pass Transistor logic (PTL) operation is directly used instead of OR logic function in the block diagram of basic PP-KSA design algorithm. All remaining processing of design procedure is similar as the basic PP design algorithm.

The normal OR gate logic calculation is given by following: Usually, anyone of the input is high (1), then automatically, the output sum results will be high (1), if two inputs are given as low (0) then automatically the OR gate logic output becomes low (0). This OR gate circuit is processed with one NOR gate logic function with one Inverter (NOT) gate logic function in 4 bit KSA adder output. In NOR gate logic, the PMOS transistors are connected in series manner and NMOS transistors are connected in parallel manner to produce the resultant output. The 4-bit PP-KSA design with proposed PTL is given in Fig.3.

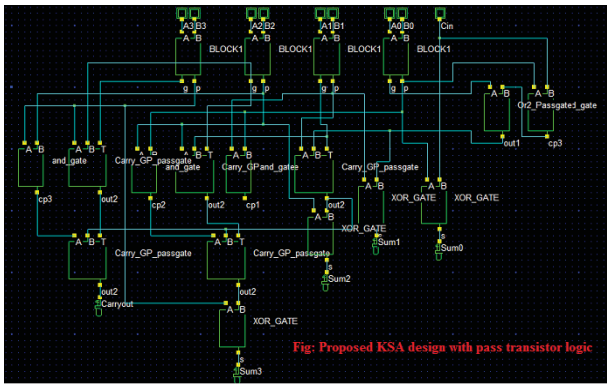

Fig. 3. Proposed PP-KSA design using Pass Transistor logic

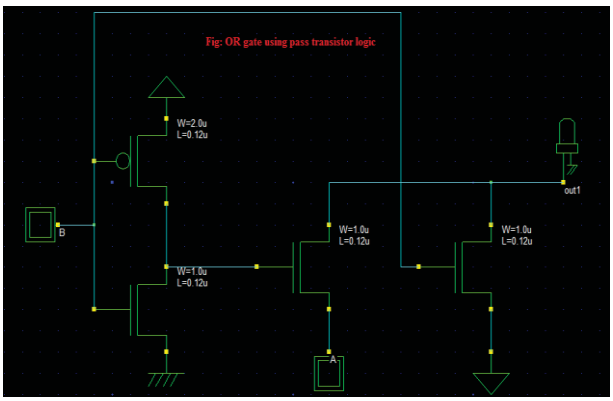

Fig. 4. Pass Transistor logic used in PP-KSA design

The Fig 4 shows the PTL logic which is applied in basic PP-KSA design algorithm of OR gate logic. If applied the Pass Transistor Logic in any design, the number of inverters used in that design is automatically reduced. In the figure, noted that the number of PMOS transistors used in the proposed design is decreased. Since the area consumption of that particular design is reduced with less number of transistors.

IV. COMPARISON OF PP-KSA DESIGN PERFORMANCES

This section describes the comparison analysis results of both KSA design with basic Parallel Prefix algorithm and Pass Transistor logic algorithm. The comparison analysis has preceded with the performance parameters such as area utilization and power consumption. In the design process, all results of synthesized and simulated can be done in Microwind CMOS tool. The execution results of CMOS design with basic PP-KSA is shown in Fig.5. Here, the three inputs A, B with the range 0-3 and Cin is used which is given in the top of the CMOS design circuit. When the execution, the LED is in ON condition for all high values (1) and the OFF for all low values (0). In Figure, Carry input values is given as high value (1) which is indicated with LED is ON condition.

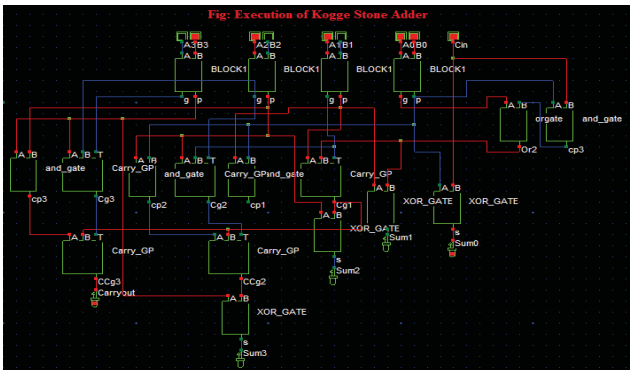

Fig. 5. Execution results of PP-KSA with regular Algorithm

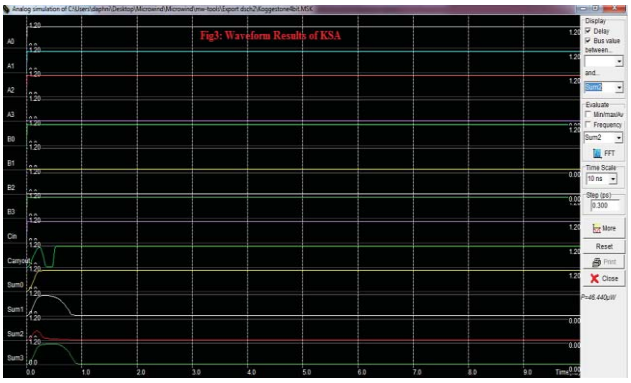

Fig. 6. Waveform results of PP-KSA with basic PP Algorithm

Here applied the input values for 4 bit to precede the execution of basic PP-KSA design. Now put the given values as A=1110, B=1001, and Cin=1. Here it has two outputs named as sum(S) and carry out (Cout). According to the input values, the output of basic Parallel Prefix Kogge Stone Adder design is Sum (0) =0, Sum (1) =0, Sum (2) =0, Sum (3) =1 and Carry out=1. In addition to that, the results have verified by waveform results for PP-KSA with basic PP algorithm which are shown in Fig.6.

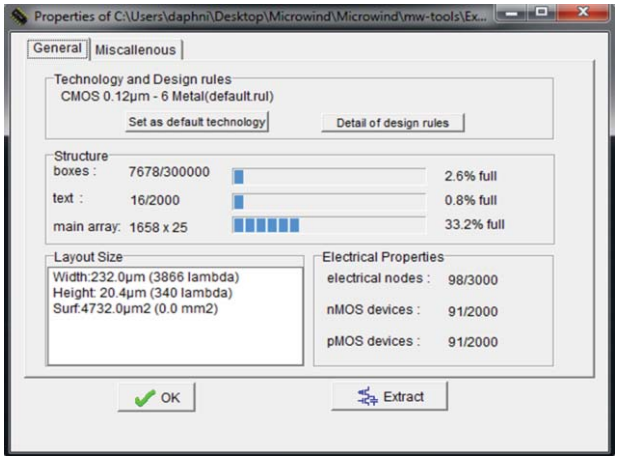

Fig. 7. Area results of PP-KSA with regular Algorithm

If focused the usage of Metal Oxide Semiconductor (MOS) devices, here both the devices NMOS and PMOS devices used the same number as 91, and the power used is 46.440 Micro Watt. The area reports of PP-KSA with basic algorithm are given in Fig.7. In proposed stage, an area efficient KSA with Pass Transistor Logic is designed to reduce the usage of number of MOS devices. For this purpose, change the OR logic gate of basic PP-KSA design with pass transistor logic. The execution results of PP-KSA with modified pass transistor logic are shown in Fig.8.

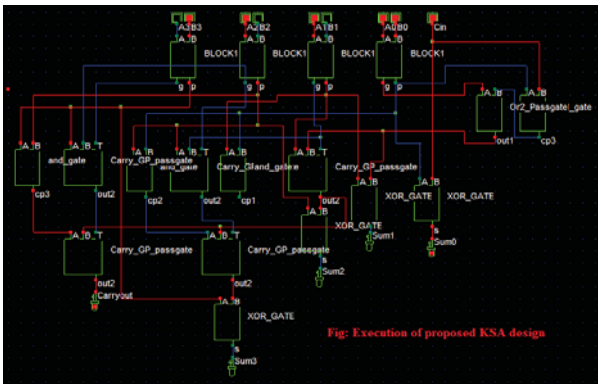

Fig. 8. Execution results of PP-KSA with modified Pass Transistor logic

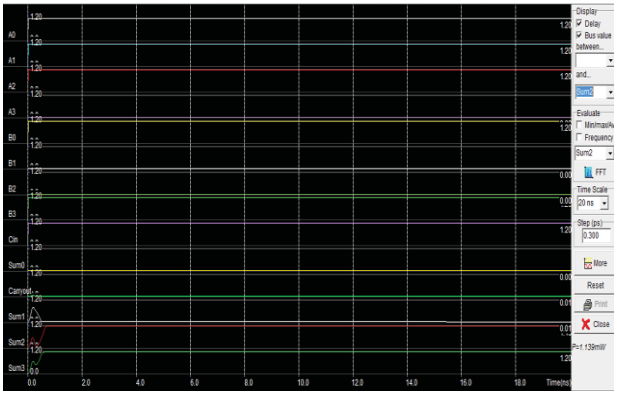

Fig. 9. Waveform results of PP-KSA with modified Pass Transistor logic

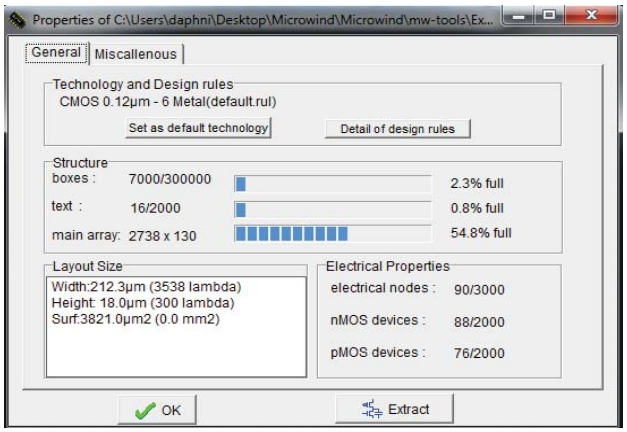

Fig. 10. Area results of PP-KSA with modified Pass Transistor logic

The waveform results of PP-KSA with modified PTL are shown in Fig.9. The area performance results of PP-KSA with modified PTL algorithm is shown in Fig.10. For execution, put the given values as A=1110, B=1001, and Cin=1. Here it has two outputs named as sum(S) and carry out (Cout). According to the input values, the output of basic Parallel Prefix Kogge Stone Adder design is Sum (0) =0, Sum (1) =0, Sum (2) =0, Sum (3) =1 and Carry out=1. If focused the usage of Metal Oxide Semiconductor (MOS) devices, here the usage of NMOS devices as 88 and PMOS devices as 76, and the power used is 46.440 Micro Watt.

V. CONCLUSION

An effective area efficient 4-bit PP-KSA design is done with Pass Transistor logic algorithm. This Proposed logic of KSA with Pass Transistor Logic design is best suitable in DSP and VLSI technologies, due to less area consumption. Here two designs of PP-KSA are discussed and compared the analysed performance on the aspects of area and power. From the result analysis, compared to the area consumption, the proposed PP-KSA design with Pass Transistor Logic is better than PP-KSA design with basic algorithm due to less number of MOS devices used. To attain more action, which is necessary in performance of recommended logic as less delay, this will be the future action of this paper.

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