Assignment Week 2 : Computer Architecture and Operating Systems

Q1. CPU Clock and Instruction Timing

- Make a simple square wave clock using a Pulse Generator.
- Add a Counter block to count instructions executed per tick.
- Plot on Scope — they'll see how more frequency = more instructions executed.

  Report the observations

Q2. Memory Read/Write Simulation

- Use **Constant** blocks as "data inputs" and a **Switch** block to choose Read or Write.
- Use **Memory** block to store values.
- Visualize read/write process on **Scope** or **Display**.

  Report your observations

Q3. Simulation Task (Using Simulink) – 35 marks

a) Build a simple Simulink model which simulates an instruction-pipeline of 3 instructions with 5 stages (IF, ID, EX, MEM, WB).

   - Use delay (e.g., Unit Delay or Transport Delay) blocks to represent the stage progression.
   - Use a Scope block to show the progression of instructions through each stage over time.

b) Modify the model to introduce a stall (e.g., due to data hazard) and simulate the effect on the pipeline timeline. Include screenshots of your model and simulation output.

c) *Bonus:* Extend the model to include a simple cache access delay (e.g., every MEM stage has an extra delay if "cache miss" flag is set). Simulate two cases (hit vs miss) and compare execution timelines.

Q4. The Five-Stage Pipeline and Instructions (20 marks)

a) Explain the purpose of each stage (Instruction Fetch, Decode, Execute, Memory Access, Write-Back) in your own words.

b) Discuss **one advantage** and **one limitation** of pipelining (e.g., structural hazard, data hazard, or branch hazard).

c) In a short paragraph, describe how pipelining improves CPU throughput but not latency.

d) List and briefly explain the **six main types of instructions**.

e) Explain the difference between **R-type, I-type, and J-type** instruction formats (if using MIPS).

Q5. Memory Hierarchy and Caching (15 marks)

a) Explain different levels of memory and draw a labeled memory hierarchy diagram.

b) Explain the concept of **volatile and non volatile memory** with one everyday example.

c) In one paragraph, describe what happens when a CPU requests data not found in the cache (cache miss).

d) Explain the 3 types of data transfer methods (Programmable I/O , Interrupt based I/O , Direct Memory Access).

Q6. Explain what is Task Scheduling and Context Switching.(15 marks)

Submission Deadline
For Task 3:- 27th November
For rest of the tasks :- 14th November

Partial Submissions are also allowed , but submitting something meaningful is necessary to continue electroverse.

PS:- You can refer to LLMs for the 1st Task for understanding how to setup and use simulink on your system.

Resources

For MATLAB Simulink

Basic guide on how to use simulink in Matlab

https://in.mathworks.com/help/simulink/gs/create-a-simple-model.html
https://youtu.be/vxzR3W2BcRk?si=OT2EXLUZTTeu-gHu
https://youtube.com/playlist?list=PL484BA2AD3AE4C2D0&si=r34OEwyQnk0XLh15

Operating systems
https://www.geeksforgeeks.org/operating-systems/operating-systems/
https://www.geeksforgeeks.org/operating-systems/cpu-scheduling-in-operating-systems/
https://www.geeksforgeeks.org/operating-systems/context-switch-in-operating-system/

Can refer to this playlist for task scheduling and also if you find the subject interesting
https://youtube.com/playlist?list=PLEBQazB0HUyQ4hAPU1cJED6t3DU0h34bz&si=FSfYI_mh1Jtor5jq

.Types of instruction and RISC architecture.

https://youtu.be/zYW8NU8OfwQ?si=HnR5QchmE63mhyNw
https://youtu.be/5i-_nZIvW6M?si=wQnO76vdGV_uNsXH
https://youtu.be/IuH_8t7vPu8?si=Hf5mMQhDzD9hMh2U

For memory hierarchy
https://youtu.be/zwovvWfkuSg?si=fv6x0J4KKbYJZUVy
https://youtu.be/KhFqQlbz2i8?si=JVfz36CpwpnGWkz5

You can refer to this playlist for a variety of topics
https://youtube.com/playlist?list=PLxCzCOWd7aiHMonh3G6QNKq53C6oNXGrX&si=Zo0AIFQcdZWocROG

Enjoyyy💕💕