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Lab Exercise 2

Write the Verilog code for designing 1 bit half adder and full adder circuit.

Design code:

```
// Code your design here
module half_adder (
   input wire A, B,
   output wire Sum, Carry
);
   assign Sum = A ^ B;     // XOR for sum
   assign Carry = A & B;   // AND for carry
endmodule



module full_adder (
   input wire A, B, Cin,
   output wire Sum, Cout
);
   assign Sum = A ^ B ^ Cin;                  // XOR for sum
   assign Cout = (A & B) | (B & Cin) | (A & Cin); // OR of AND terms for carry
endmodule
```

testbench:

```
// Code your testbench here
// or browse Examples
module tb;
   reg A, B, Cin;
   wire Sum_HA, Carry_HA, Sum_FA, Cout_FA;
```

```
    // Instantiate Half Adder
    half_adder ha(.A(A), .B(B), .Sum(Sum_HA), .Carry(Carry_HA));

    // Instantiate Full Adder
    full_adder fa(.A(A), .B(B), .Cin(Cin), .Sum(Sum_FA), .Cout(Cout_FA));

    initial begin
        $display("A B Cin | Sum_HA Carry_HA | Sum_FA Cout_FA");
        $display("-----------------------------------------------");

        for (integer i = 0; i < 8; i = i + 1) begin
            {A, B, Cin} = i;  // Assign binary values
            #10;
            $display("%b %b  %b   |   %b      %b     |   %b    %b", A, B, Cin, Sum_HA, Carry_HA, Sum_FA, Cout_FA);
        end

        $finish;
    end
endmodule
```

output: