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## Lab Exercise 4

**Aim: Write the Verilog code for designing 4 bit ripple carry adder circuit and verify.**

**Code:**

// Code your design here

```
module ripple_carry_adder (input [3:0] A, input [3:0] B, input Cin, output [3:0] Sum,  
output Cout);  
    wire c1, c2, c3;
```

// Full Adder Instances

```
    full_adder FA0 (A[0], B[0], Cin, Sum[0], c1);  
    full_adder FA1 (A[1], B[1], c1, Sum[1], c2);  
    full_adder FA2 (A[2], B[2], c2, Sum[2], c3);  
    full_adder FA3 (A[3], B[3], c3, Sum[3], Cout);  
endmodule
```

// Full Adder Module

```
module full_adder (input A, input B, input Cin, output Sum, output Cout);  
    assign Sum = A ^ B ^ Cin;  
    assign Cout = (A & B) | (B & Cin) | (A & Cin);  
endmodule
```

**Testbench:**

// Code your testbench here

// or browse Examples

```
module tb_ripple_carry_adder();  
    reg [3:0] A, B;  
    reg Cin;  
    wire [3:0] Sum;  
    wire Cout;  
  
    // Instantiate the Ripple Carry Adder  
    ripple_carry_adder uut (A, B, Cin, Sum, Cout);  
  
    initial begin
```

```
$monitor("Time=%0t A=%b B=%b Cin=%b | Sum=%b Cout=%b", $time, A, B, Cin,  
Sum, Cout);
```

```
// Test cases
```

```
A = 4'b0000; B = 4'b0000; Cin = 1'b0; #10;
```

```
A = 4'b0101; B = 4'b0011; Cin = 1'b0; #10;
```

```
A = 4'b1111; B = 4'b0001; Cin = 1'b0; #10;
```

```
A = 4'b1010; B = 4'b0101; Cin = 1'b1; #10;
```

```
A = 4'b1111; B = 4'b1111; Cin = 1'b0; #10;
```

```
A = 4'b1111; B = 4'b1111; Cin = 1'b1; #10;
```

```
$stop;
```

```
end
```

```
endmodule
```

## Output:

[Log](#)[Share](#)

```
[2025-03-08 06:16:58 UTC] iverilog '-wall' '-g2012' design
```

```
Time=0 A=0000 B=0000 Cin=0 | Sum=0000 Cout=0
```

```
Time=10 A=0101 B=0011 Cin=0 | Sum=1000 Cout=0
```

```
Time=20 A=1111 B=0001 Cin=0 | Sum=0000 Cout=1
```

```
Time=30 A=1010 B=0101 Cin=1 | Sum=0000 Cout=1
```

```
Time=40 A=1111 B=1111 Cin=0 | Sum=1110 Cout=1
```

```
Time=50 A=1111 B=1111 Cin=1 | Sum=1111 Cout=1
```

```
testbench.sv:23: $stop called at 60 (1s)
```

```
** VVP Stop(0) **
```

```
** Flushing output streams.
```

```
** Current simulation time is 60 ticks.
```

```
Execution interrupted or reached maximum runtime.
```