Name: Dhruvi Patel
Enroll No: 92200133029
Sub: DDV

Lab Exercise 4

Aim: Write the Verilog code for designing 4 bit ripple carry adder circuit and verify.

Code:

```
// Code your design here
module ripple_carry_adder (input [3:0] A, input [3:0] B, input Cin, output [3:0] Sum,
output Cout);
    wire c1, c2, c3;

    // Full Adder Instances
    full_adder FA0 (A[0], B[0], Cin,  Sum[0], c1);
    full_adder FA1 (A[1], B[1], c1,   Sum[1], c2);
    full_adder FA2 (A[2], B[2], c2,   Sum[2], c3);
    full_adder FA3 (A[3], B[3], c3,   Sum[3], Cout);
endmodule

// Full Adder Module
module full_adder (input A, input B, input Cin, output Sum, output Cout);
    assign Sum = A ^ B ^ Cin;
    assign Cout = (A & B) | (B & Cin) | (A & Cin);
endmodule
```

Testbench:

```
// Code your testbench here
// or browse Examples
module tb_ripple_carry_adder();
    reg [3:0] A, B;
    reg Cin;
    wire [3:0] Sum;
    wire Cout;

    // Instantiate the Ripple Carry Adder
    ripple_carry_adder uut (A, B, Cin, Sum, Cout);

    initial begin
```

```
        $monitor("Time=%0t A=%b B=%b Cin=%b | Sum=%b Cout=%b", $time, A, B, Cin, Sum, Cout);

        // Test cases
        A = 4'b0000; B = 4'b0000; Cin = 1'b0; #10;
        A = 4'b0101; B = 4'b0011; Cin = 1'b0; #10;
        A = 4'b1111; B = 4'b0001; Cin = 1'b0; #10;
        A = 4'b1010; B = 4'b0101; Cin = 1'b1; #10;
        A = 4'b1111; B = 4'b1111; Cin = 1'b0; #10;
        A = 4'b1111; B = 4'b1111; Cin = 1'b1; #10;

        $stop;
    end
endmodule
```

Output: