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Lab Exercise 3

Aim: Write the Verilog code for designing 16x1 Multiplexer with 2x1 multiplexer and verify.

code:

```
// 2x1 Multiplexer
module mux2x1(input d0, input d1, input sel, output y);
   assign y = sel ? d1 : d0;
endmodule

// 16x1 Multiplexer using 2x1 Multiplexers
module mux16x1(
   input [15:0] d,  // 16 data inputs
   input [3:0] sel, // 4-bit selection input
   output y        // Output
);
   wire [7:0] mux_level1;
   wire [3:0] mux_level2;
   wire [1:0] mux_level3;

   // Level 1: 8 mux2x1
   genvar i;
   generate
      for (i = 0; i < 8; i = i + 1) begin
         mux2x1 m1 (.d0(d[2*i]), .d1(d[2*i+1]), .sel(sel[0]), .y(mux_level1[i]));
      end
   endgenerate

   // Level 2: 4 mux2x1
   generate
      for (i = 0; i < 4; i = i + 1) begin
         mux2x1 m2 (.d0(mux_level1[2*i]), .d1(mux_level1[2*i+1]), .sel(sel[1]), .y(mux_level2[i]));
      end
```

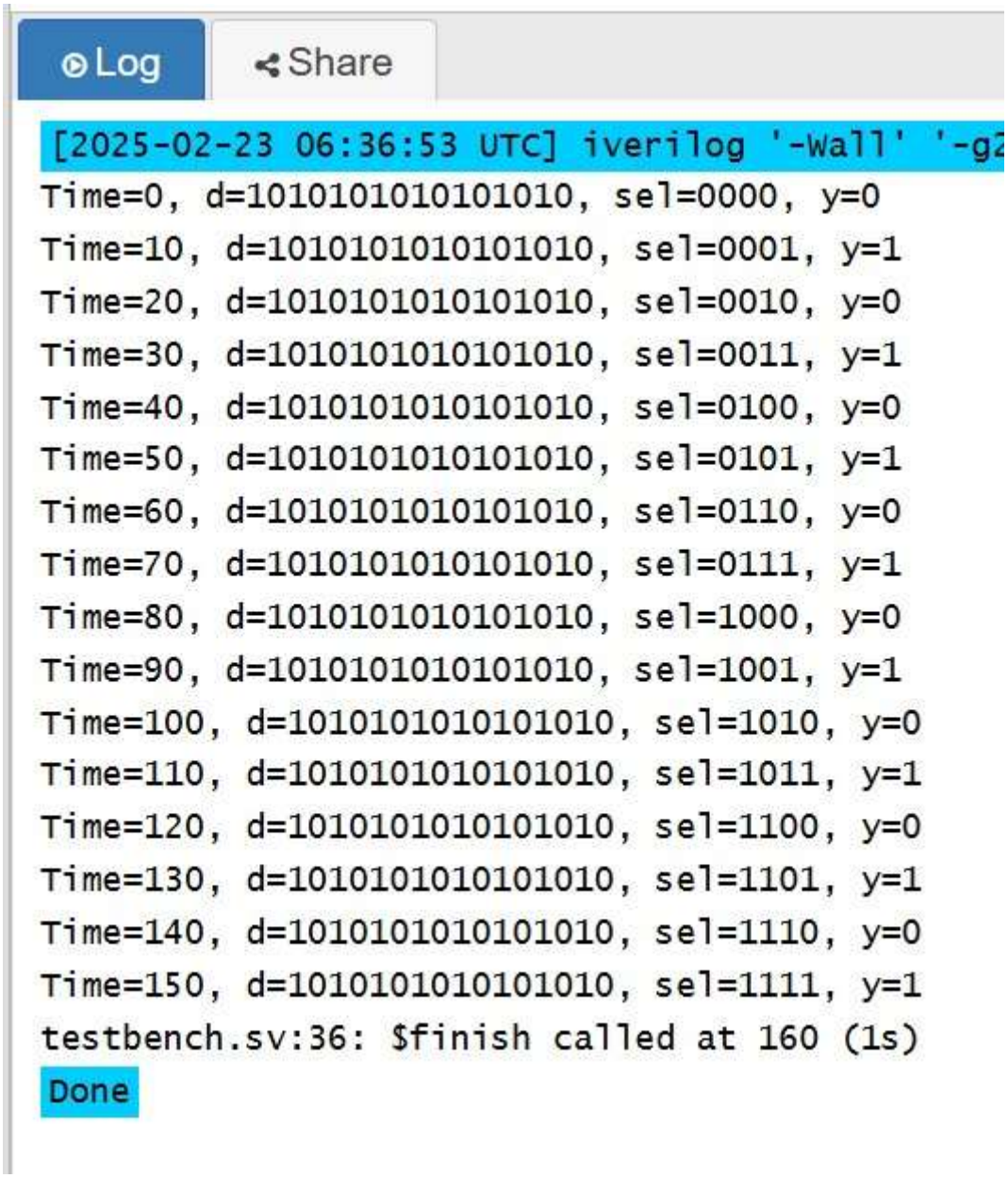
```
    endgenerate

    // Level 3: 2 mux2x1
    generate
        for (i = 0; i < 2; i = i + 1) begin
            mux2x1 m3 (.d0(mux_level2[2*i]), .d1(mux_level2[2*i+1]), .sel(sel[2]), .y(mux_level3[i]));
        end
    endgenerate

    // Final Level: 1 mux2x1
    mux2x1 m4 (.d0(mux_level3[0]), .d1(mux_level3[1]), .sel(sel[3]), .y(y));
endmodule
```

testbench:

```
// Testbench for 16x1 Multiplexer
module testbench;
    reg [15:0] d;
    reg [3:0] sel;
    wire y;

    mux16x1 uut (
        .d(d),
        .sel(sel),
        .y(y)
    );

    initial begin
        $monitor("Time=%0t, d=%b, sel=%b, y=%b", $time, d, sel, y);

        d = 16'b1010101010101010;
```

```
// Test different select values
sel = 4'b0000; #10;
sel = 4'b0001; #10;
sel = 4'b0010; #10;
sel = 4'b0011; #10;
sel = 4'b0100; #10;
sel = 4'b0101; #10;
sel = 4'b0110; #10;
sel = 4'b0111; #10;
sel = 4'b1000; #10;
sel = 4'b1001; #10;
sel = 4'b1010; #10;
sel = 4'b1011; #10;
sel = 4'b1100; #10;
sel = 4'b1101; #10;
sel = 4'b1110; #10;
sel = 4'b1111; #10;

$finish; enddmodule
```

OUTPUT:


Log
Share
[2025-02-23 06:36:53 UTC] iverilog '-Wall' '-g2
Time=0, d=1010101010101010, sel=0000, y=0
Time=10, d=1010101010101010, sel=0001, y=1
Time=20, d=1010101010101010, sel=0010, y=0
Time=30, d=1010101010101010, sel=0011, y=1
Time=40, d=1010101010101010, sel=0100, y=0
Time=50, d=1010101010101010, sel=0101, y=1
Time=60, d=1010101010101010, sel=0110, y=0
Time=70, d=1010101010101010, sel=0111, y=1
Time=80, d=1010101010101010, sel=1000, y=0
Time=90, d=1010101010101010, sel=1001, y=1
Time=100, d=1010101010101010, sel=1010, y=0
Time=110, d=1010101010101010, sel=1011, y=1
Time=120, d=1010101010101010, sel=1100, y=0
Time=130, d=1010101010101010, sel=1101, y=1
Time=140, d=1010101010101010, sel=1110, y=0
Time=150, d=1010101010101010, sel=1111, y=1
testbench.sv:36: $finish called at 160 (1s)
Done