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Lab Exercise 1

Write the Verilog code to implement given logic functions using continuous assignments.

g= x1x3 + x2x4
h = (x1 + x3 bar)(x2bar + x4)
f = g + h

Design code:

```
// Code your design here
module logic_functions(
   input wire x1, x2, x3, x4,
   output wire g, h, f
);
   assign g = (x1 & x3) | (x2 & x4);
   assign h = (~x3 | x1) & (~x2 | x4);
   assign f = g | h;
endmodule
```

testbench:

```
// Code your testbench here
// or browse Examples
module tb;
   reg x1, x2, x3, x4;
   wire g, h, f;

   // Instantiate the design module
   logic_functions uut(.x1(x1), .x2(x2), .x3(x3), .x4(x4), .g(g), .h(h), .f(f));

   // Simulation block
   initial begin
```

```
        $display("x1 x2 x3 x4 | g h f");
        $display("--------------------");

        for (integer i = 0; i < 16; i = i + 1) begin
            {x1, x2, x3, x4} = i;  // Assign binary values to inputs
            #10;  // Wait for simulation update
            $display("%b  %b  %b  %b  | %b %b %b", x1, x2, x3, x4, g, h, f);
        end

        $finish;  // End simulation
    end
endmodule
```

Output:

Log Share

```
[2025-02-15 15:16:26 UTC] iverilog '-Wall' '-g2012' design.sv testbench.sv  && unbuffer vvp a.out
x1 x2 x3 x4 | g h f
--------------------
0  0  0  0  | 0 1 1
0  0  0  1  | 0 1 1
0  0  1  0  | 0 0 0
0  0  1  1  | 0 0 0
0  1  0  0  | 0 0 0
0  1  0  1  | 1 1 1
0  1  1  0  | 0 0 0
0  1  1  1  | 1 0 1
1  0  0  0  | 0 1 1
1  0  0  1  | 0 1 1
1  0  1  0  | 1 1 1
1  0  1  1  | 1 1 1
1  1  0  0  | 0 0 0
1  1  0  1  | 1 1 1
1  1  1  0  | 1 0 1
1  1  1  1  | 1 1 1
testbench.sv:21: $finish called at 160 (1s)
Done
```