

Dhruv Agrawal

CONTACT INFORMATION Senior Year Undergraduate Student
Indian Institute of Technology
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date of birth: January, 7 '1991

RESEARCH INTERESTS Computer Vision, Machine Learning, Robotics

| EDUCATION | Year | Degree/Exam | Institute | GPA/Marks |
|-----------|------|-------------------------|--------------------------------------|------------------|
| | — | B.Tech Electrical Engg. | Indian Institute of Technology Delhi | 7.38/10.0 |
| | 2009 | High School CBSE | DAV Public School Kota | 89.8% |
| | 2007 | Senior School CBSE | Maharana Mewar Public School Udaipur | 95.8% |

SELECTED PUBLICATIONS Abstract ID- 392, Abstract Title- **“Design and User-Study of an affordable Indoor Navigation System for Visually Impaired”**, accepted for presentation in 13th International Conference on “Mobility and Transport for Elderly and Disabled People” **TRANSED 2012**

SCHOLASTIC ACHIEVEMENTS

- Summer Undergraduate Research Award 2011, a research project **funded by the Ministry of HRD, India** for project on FPGA acceleration of sequence alignment algorithms.
- IITD Semester Merit Award for being in top 7% of all the undergraduate 2009 batch students.
- All India Rank 1(PD) in IIT JEE and AIEEE 2009.

PROJECTS

INDOOR NAVIGATION SYSTEM FOR VISUALLY IMPAIRED

(Prof. M. Balakrishnan, Prof. P.V.M. Rao)

Embedded Systems, Assistive Technology

(May, 2011 – April, 2012)

Low-cost (< **INR 800**) setup to help a visually impaired individual navigate freely inside a building via acoustic messages from mobile phone. The Infrared based system requires minimal additional building infrastructure and a small user waist-worn device. (www.roshni.info)

- Surveyed and tested different technologies for localization(RSSI, RFID, Ultrasound, Infrared)
- Developed the waist-worn device consisting of accelerometer, Infrared and bluetooth modules which communicates with hand-held android phone application
- Developed the wall mounted network with IRs, microcontrollers and buzzers
- **Demonstrated in an institute building during IIT Delhi - Open House '2012.**
- **Received considerable media attention**
- **Field testing with 5 visually impaired users** gave a positive and encouraging feedback

WHITESPACE NETWORK FOR VIDEO UPLINK FROM VEHICULAR SYSTEMS

(Prof. Vinay Ribeiro, Prof. Manish Sharma)

Computer Networks

(July, 2011 – April, 2012)

This is a joint project of IIT Delhi and Univ. of Wisconsin, Madison. It aims to send video surveillance information collected through a network of city buses to a central location via the cognitive radio technology. I worked on the simulation and implementation of MAC-layer protocol.

- Explored wireless technologies(WiFi, WiMAX, GSM, CDMA) to choose the appropriate one
- **Designed the complete physical layout of the APs and the MAC-Layer** based on two different technologies: Distributed polling with RSSI based localisation and TDMA with GPS
- Lab tested polling and handoff mechanisms on USRP2 boards using GNU Radio software suit

Research Assistantship

Univerisity of Wisconsin, Madison

(Prof. Suman Banerjee)

(May, 2011 – Present)

Working on modifying OFDM design of Rice Univerisity's WARP board to achieve shrinkage of the default bandwidth by disabling subcarriers.

FPGA AS ACCELERATORS FOR NEXT GENERATION SEQUENCING

(Prof. M. Balakrishnan)

Embedded Systems, Computational Biology

(Mar, 2011 – Feb, 2012)

Hardware-Software co-design for Bioinformatics applications to

(www.seq-align-fpga.info)

explore FPGAs for speeding up DNA sequence alignment algorithms.

- Surveyed and selected some of the best known algorithms(BWA, MAQ, SOAP etc.)
- Profiled the software-tools in terms of usage and running time and noted their critical areas
- Selected one algorithm and designed the modules for its parallelized implementation on FPGA

Course Projects –

- **Multiplayer Ping Pong Game** (Networking) (July, 2010 - Nov, 2010) : Multiplayer networking game supporting upto four players. Game was coded in C++ using OpenGL. Only submission which used UDP broadcasting for the clients to automatically search for the available servers
- **MIPS-32 Processor Design** (Computer Architecture) (July, 2010 - Nov, 2010) : Designed a subset of MIPS-32 instruction set on a simulator. The application computes and displays the day of the week corresponding to the specified date
- **Implementation of Systolic Sorting Architecture on FPGA Board** (Embedded Systems) (Jan, 2011 - Apr, 2011) : Implemented sorting of numbers on FPGA board via the systolic array of Digital Processing Units (DPUs) Code was written in VHDL
- **Android Application for GPS Navigation** (Design Practices) (July, 2010 - Nov, 2010) : An android application in Java and Web interface in PHP, Javascript, JQuery and Ajax for finding the shortest path from one point to another based on current traffic density
- **Interpreters for subsets of Prolog and SML** (Programming Languages) (Jan - Apr, 2011) : Built a lexer, parser and an interpreter for a subset of the functions provided by SML and prolog
- **Sorting Algorithms -CatapultC** (System Level Design and Modelling) (Jan - Apr, 2012) : Explored the performance of various sorting algorithms on HLL Design tool - CatapultC
- **Enhanced Pintos Operating System** (Operating Systems) (Jan - Apr, 2013): Coded the relevant parts of basic inefficient Pintos OS to make it more reliable and improve performance
- **New Algorithm for Gene Prediction** (Bioinformatics) (Jan - March, 2013): Developed a faster and more reliable algorithm for Human Gene Prediction based on existing softwares.

Independent Projects –

- **Animation Clip display** (Embedded Systems) (Nov, 2010 - Jan, 2011) : Created a colour-encrypted animation clip on VGA screen from a sequence of images using FPGA board
- **Rationality in Decision Making** (Social Psychology) (July, 2011 - Nov, 2011) : To explore whether human beings are rational in their approach of making decisions and how their rationality is influenced by social factors like ambitions and moral values

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| RELEVANT COURSES | System Level Design and Modelling Digital Hardware Design Embedded System Design Lab Analysis and Design of Algorithms | Operating Systems Bioinformatics Signals and Systems Digital Electronics | Computer Aided Design Computer Networks Computer Architecture Programming Languages |
| POSITION OF RESPONSIBILITY | <ul style="list-style-type: none"> • Served as a volunteer for International Conference on Field Programmable Technology held in New Delhi, India. Successfully organised the FPGA design competition “Connect6”. • Served as a Student Mentor for the CSE Department First Year Students. Helped them get acquainted with the college studies and environment. | | |
| OTHER ACTIVITIES | <ul style="list-style-type: none"> • Attended the summer camp on Information Retrieval and Web Search by Yahoo in Bangalore. • Active member of Topcoder Programming Community with the current rating of 1496(Blue Coder). • Went for a rural group exposure with a team of 12 students as part of an NGO programme(Pravah). • Built websites for Startups: “Goshti” and “thewittyshit” and developed facebook applications. | | |
| PROGRAMMING LANGUAGES | VHDL, Java, C/C++, Python, SML, Lex, Yacc, Prolog, PHP, Javascript/Jquery, Ajax, MySQL, ASP.NET, HTML/CSS, Bash, L ^A T _E X 2 _ε , Assembly Language, FBML/FBJS, SystemC, Bluespec | | |
| SOFTWARES | Xilinx ISE, Xilinx Platform Studio, Eclipse/Android, Netbeans, Jcreator, MS Visual Studio, Matlab, Drupal, Wordpress, Joomla, Ideas, SolidWorks, GNU Radio, Mentor Graphics CatapultC, Intel Vtune | | |
| HARDWARES | FPGAs(Virtex, Spartan), Microcontrollers(Arduino/Atmega, PIC), PCB Design(Diptrace/Eagle), WARP, USRP, Xilinx Zynq EPP, Alpha Data | | |
| INTERESTS | Web-Development, Swimming, Humanistic Psychology, Musical Instrument- Keyboard | | |
| REFEREES | <div> Prof. M. Balakrishnan Professor and Deputy Director of Faculty Indian Institute of Technology New Delhi, India mbala@cse.iitd.ernet.in </div> <div> Prof. Vinay Joseph Ribeiro Assistant Professor Indian Institute of Technology New Delhi, India vinay@cse.iitd.ernet.in </div> | | |