Nirma University

Institute of Technology
Semester End Examination (IR), December - 2016
B. Tech. in Computer Engineering, Semester-VII
IT794 Compiler Construction

RollNo/ Exam N					Supe with	ervisor's Ini date	itial		
Time:	3 Hours					Max	Marks: 10	0	
Instruc	1	2. Section	wise sepa	arate ans al informa	wer book ation if rec	to be used	e full mark l.	cs.	
0-1	Answer	the follo	wing que		ON – I				[18]
A)					r be left r	ooureivo?			(T)
50.500		2 C 200						[3]	
	B) New languages 'H' and 'HS' is designed for distinct HPC systems (HPC1, [3] HPC2, HPC3, HPC4). Compilers are to be designed for these languages. Advisor 1 suggest to assign one compiler design to one developer team. Advisor 2 proposes to divide compiler tasks into 2 pass: front-end phases and back-end phases, and distribute each pass to distinct developer teams. Which proposal do you prefer? Justify.								
C)	Write R	ecursive of	descent pa	erser for t	he followi	ng parse t	table \$		[4]
		S	TS	[S]S)S	ε	ε		
		T	(X)						
		X	TX	[X]X	ε	ε			
D)	Write a	regular from its	expressio augmente	n to ider d regular	ntify emai expression	l address n.	. Construc	et DFA	[4]
E)	Is Error	r handling	g required	at each p	phase of c	ompiler?	Justify.		[4]
Q-2	Answe	the follo	owing que	estions:					[16]
A)	derivat recogni	ion of th ize classA	e string and inter ss identifie	"class cla faceB as er X Y	assA implidentifier. X - Y - I -	ements in extends in impleme	rsing table nterface B " identifier nts $I \mid \varepsilon$ if $I \mid identifien$. Lexer	
A)	functio	n matrix	for opera	cedence tors "+ -	* / ()",	token ID	rator pred , and deline ence parsi	miter \$: [8]

B) Eliminate Left-Recursion (if exist) from the following grammar: $S \rightarrow Aa \mid b$

[4]

 $A \rightarrow Ac \mid Sd \mid Bf$ $B \rightarrow Sa \mid Ab \mid d$

C) Analyze syntax of "ID + ID * ID" using operator precedence parsing for [4] grammar: $E \rightarrow E + E \mid E * E \mid ID$

Q-3 Answer the following questions:

[16]

A) Show that the following grammar is LALR(1) but not SLR(1).

[8]

 $S \rightarrow Aa \mid bAc \mid dc \mid bda$ $A \rightarrow d$

B) Trace LR parsing for input string "(() ())" using given parsing table for a grammar containing production rules 1) S → (S)S 2) S→ null

	S	()	\$
0	1	s2	r2	r2
1				acc
2	3	s2	<i>r</i> 2	r2
3			s4	
4	5	s2	r1	r1

OR

B) LR parsing table need more space than LL parsing table. Describe an [4] approach to reduce its space complexity.

C) Give an example of grammar, which is LL(1) but not LR(0)

[4]

SECTION - II

Q-4 Answer the following questions:

[18]

A) Rewrite following Grammar G to avoid ambiguity considering given [4] precedence, and associatively of symbols. $G = \{S \rightarrow S + S \mid S - S \mid S^*S \mid S^*S \mid D^*S \mid NUM \mid D \mid (S)\}$

Symbols	Precedence	Associatively		
NUM, ID, (1 (highest)	Left to Right		
٨	2	Right to Left		
/, *	3	Left to Right		
+, -	4	Left to Right		
= 9	5 (lowest)	Right to Left		

B) State whether the following statements are true or false. Justify your answer

[6]

i. Every L-attributed definition is S-attributed definition.

ii. A non-left recursive and left-factored grammar may not be LL(1).

iii. SLR(1) parser has same number of states as LALR(1) parser

C) Trace code generation and register allocation using register and address descriptor for following IR code:

[8]

$$t1 := a + b;$$

 $t2 := a - c;$
 $t3 := t1 + t2;$
 $a := t3$

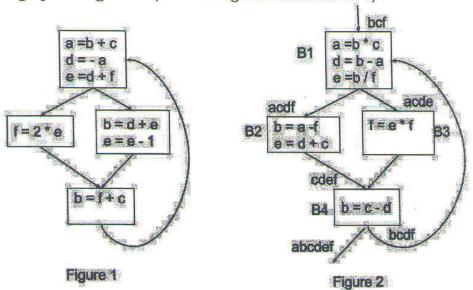
Q-5 Answer the following questions:

[16]

- A) What is advantage of register allocation using Graph coloring? Explain [10] using register allocation for flow graph given in Figure 1.
- B) Design a Syntax Directed definition to identify undeclared and re- [6] declared variables.

OR

B) Considering variable usage count, which variables will get register in [6] flow graph of Figure 2? (assume register bank size is 3)



Q-6 Answer the following questions:

[16]

A) Translate following 'C' code fragment to IR. Convert it into flow graph. [6] while(a<b) {

if(c<d) x=a[i]+2; else x=a[i]*3;

OR

A) Explain any four code optimization approaches.

[6]

B) Write top-down evaluation code for following SDD:

[6]

 $A \rightarrow B$ {print(B.n0), print(B.n1)} $B \rightarrow 0 B_1$ {B.n0=B₁.n0+1, B.n1=B₁.n1} $B \rightarrow 1 B_1$ {B.n0=B₁.n0, B.n1=B₁.n1+1}

 $B \rightarrow \varepsilon$ {B.n0=0, B.n1=0}

C) Explain shift/reduce conflict, reduce/reduce conflict using proper [4] example.