E3-277 Introduction to Integrated Circuit Design

Lab Assignment 3

Submitted

by

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0.1 Two-Stage Op-amp

In this homework, you are to design a basic two-stage CMOS operational amplifier (op-amp), as shown in Fig.1, for the specifications given in Table 1. The op-amp consists of a differential input stage (M3 and M4) driving a current mirror load (M1 and M2) followed by a common-source amplifier stage (M6). The devices M5 and M7 form the tail current source for the differential stage and the current source load for the common-source stage. Cc and Rz are the compensation capacitor and the zero-nulling resistor.

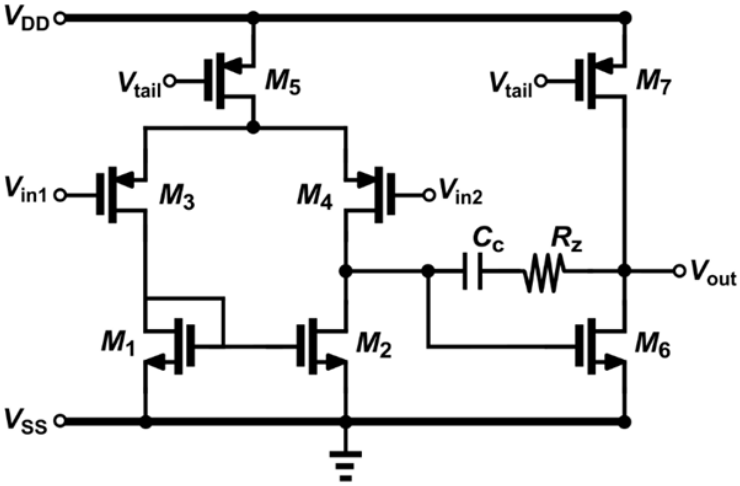
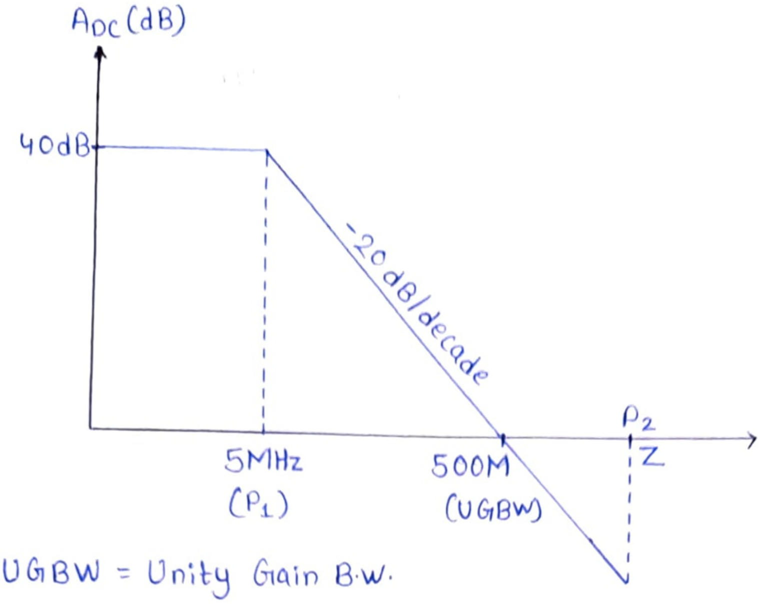


FIGURE 1: A basic two-stage operational amplifier.

TABLE 1: Design specifications @ supply voltage = 1.2V, Load = 100pF, and temperature = 27°C

S.N.	Parameter	Symbol	Value
1.	Open-loop, differential-mode, DC voltage gain	A_0	$\geq 100\ V/V\ (40\ dB)$
2.	-3dB-Bandwidth	f_{-3dB}	$\geq 5\ MHz$
3.	Phase margin	PM	$\geq 60°$
4.	Common-mode rejection ratio	$CMRR$	$\geq 30\ dB$
5.	Power dissipation	P_d	$\leq 800\ \mu W$

Design Steps



UGBW = Unity Gain B.W.

$$\because \frac{V_{out}}{V_{in}} = \frac{A_{DC}\left(1-\frac{s}{z}\right)}{\left(1+\frac{s}{P_1}\right)\left(1+\frac{s}{P_2}\right)}$$

$$\angle \frac{V_{out}}{V_{in}} = -\tan^{-1}\left(\frac{\omega}{z}\right) - \tan^{-1}\left(\frac{\omega}{P_1}\right) - \tan^{-1}\left(\frac{\omega}{P_2}\right).$$

Take $Z = P_2$

$$\angle \frac{V_{out}}{V_{in}} = -2\tan^{-1}\left(\frac{\omega}{P_2}\right) - \tan^{-1}\left(\frac{\omega}{P_1}\right).$$

$$\angle \frac{V_{out}}{V_{in}}\Bigg|_{\omega = UGBW} = -2\tan^{-1}\left(\frac{UGBW}{P_2}\right) - \tan^{-1}\left(\frac{UGBW}{P_1}\right)$$

$$UGBW = \frac{g_{m1}}{C_c} = 500MHz$$

$$P_1 \approx \frac{1}{g_{m2}\, r_{o2}\, r_{o1}\, C_c}.$$

$$P_2 \approx \frac{g_{m2}}{C_L}$$

$$\left.\angle\frac{V_{out}}{V_{in}}\right|_{\omega=GBW} = -2\tan^{-1}\left(\frac{UGBW}{P_2}\right) - \tan^{-1}\left(g_{m1}g_{m2}r_{o1}r_{o2}\right).$$

$$= -2\tan^{-1}\left(\frac{UGBW}{P_2}\right) - \tan^{-1}(A_{DC})$$

$$\therefore -180^\circ + PM = -2\tan^{-1}\left(\frac{UGBW}{P_2}\right) - 90^\circ$$

$\because A_{DC}$ is very high.

$\therefore$ For $PM = 60^\circ$,

$$\tan^{-1}\left(\frac{UGBW}{P_2}\right) = 15^\circ.$$

$$\therefore \frac{UGBW}{P_2} \approx 0.27$$

$$\therefore P_2 = \frac{500\,MHz}{0.27} = 1851.85\,MHz.$$

$$\therefore \frac{g_{m_2}}{C_L} = 1851.85 \times 10^6 \times 2\pi$$

Let $C_L = 500fF$ (including parasitics)

$$\therefore g_{m_2} \geqslant 5.85mS.$$

$UGBW = 500MHz$

$$\therefore \frac{g_{m_1}}{C_c} = 500 \times 10^6 \times 2\pi$$

Let $C_c = 900fF$ (including parasitics).

$$\therefore g_{m_1} \geqslant 2.83mS.$$

$$\because R_Z = P_2 \Rightarrow R_Z = \frac{1}{g_{m_2}}$$

In our design $g_{m_2} = 6.04mS$

$$\therefore R_Z = \frac{1}{6.04 \times 10^{-3}} \approx 165\Omega.$$

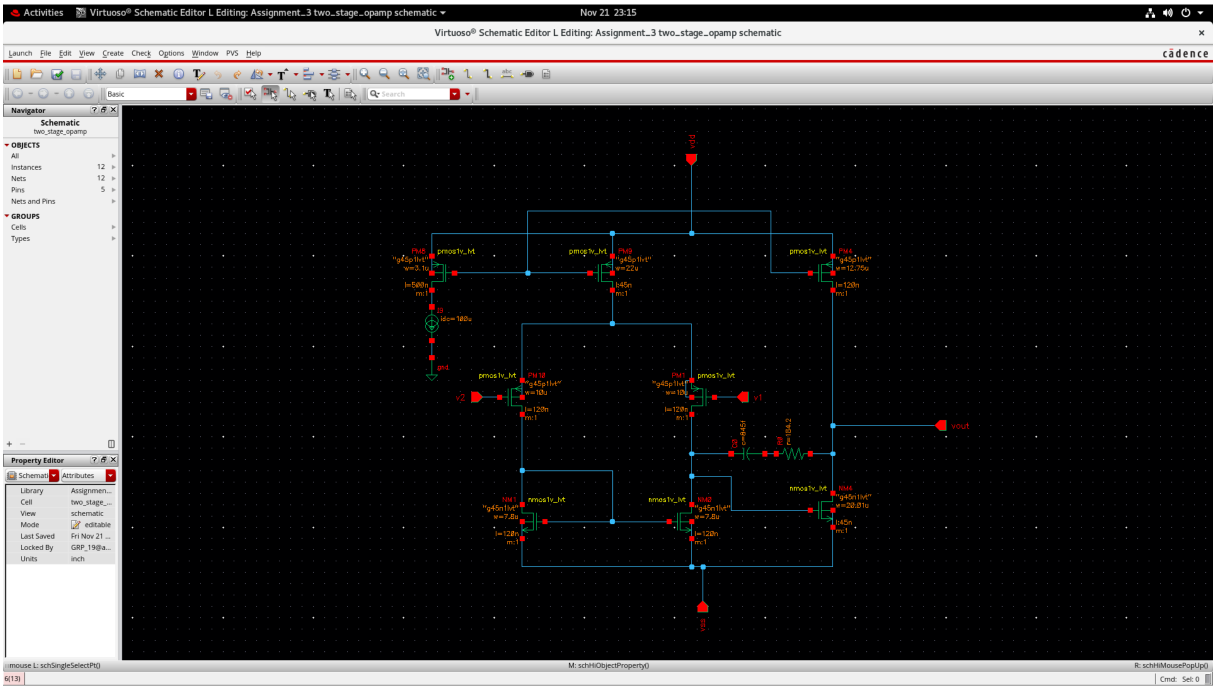


FIGURE 2: Two-stage Opamp

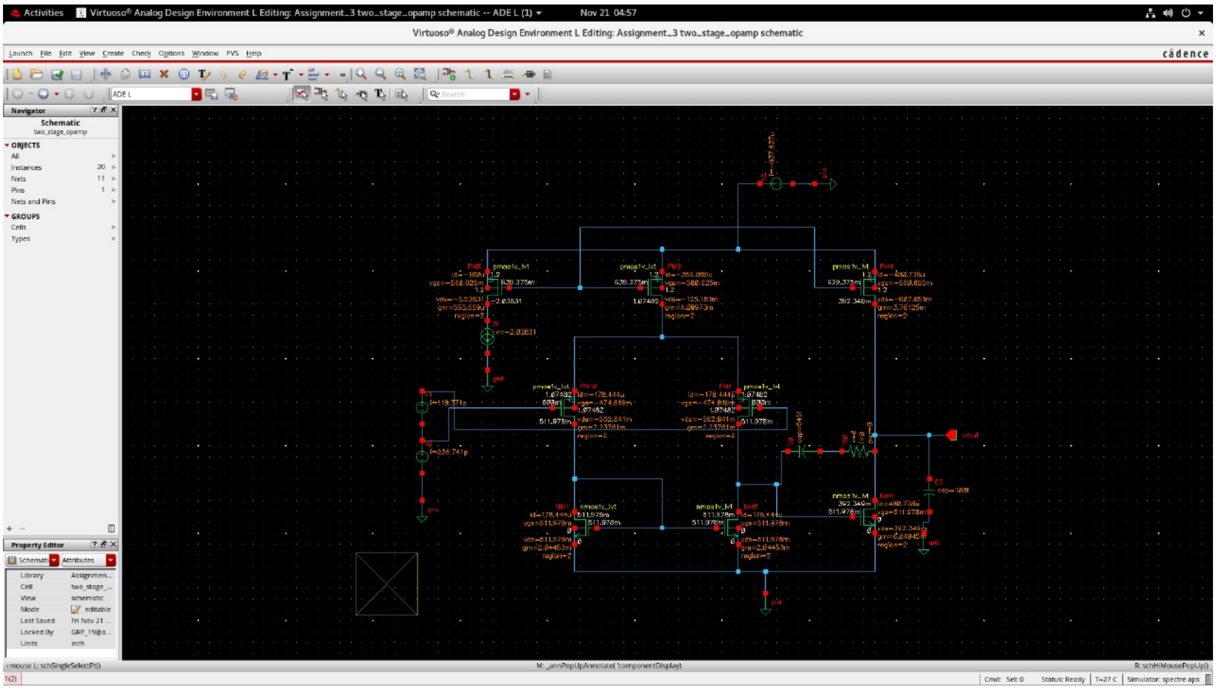


FIGURE 3: DC operating points

0.2 DC Testbench results

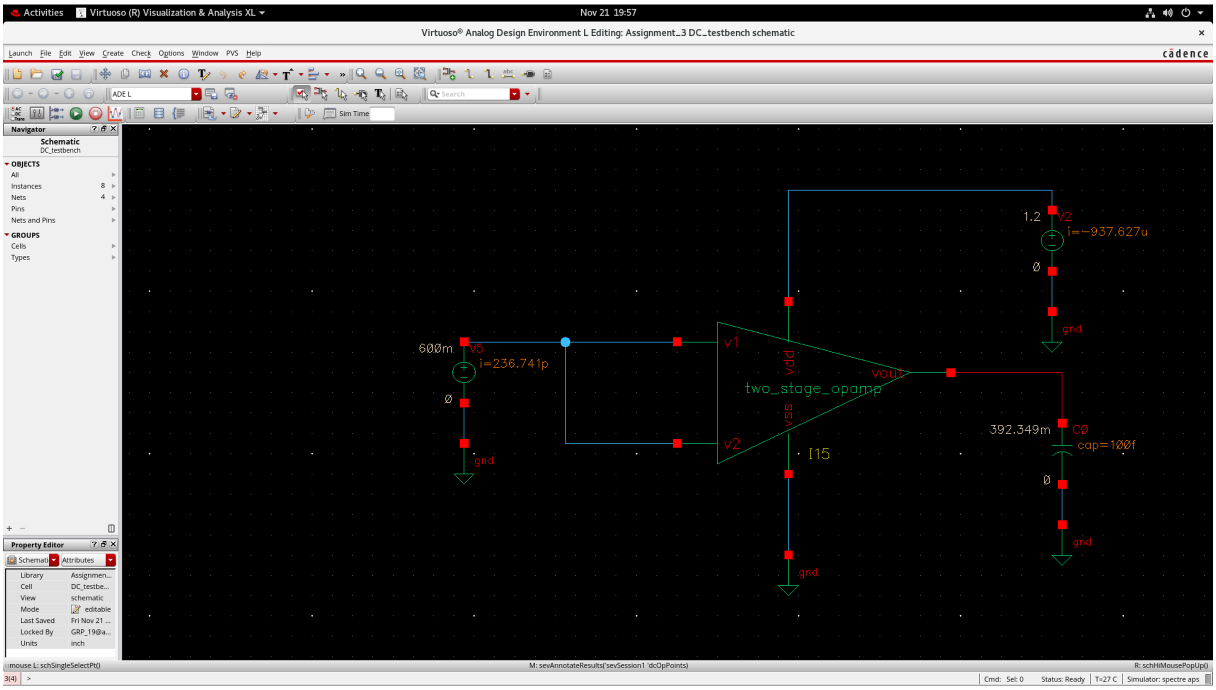


FIGURE 4: Opamp with Vin = Vcm

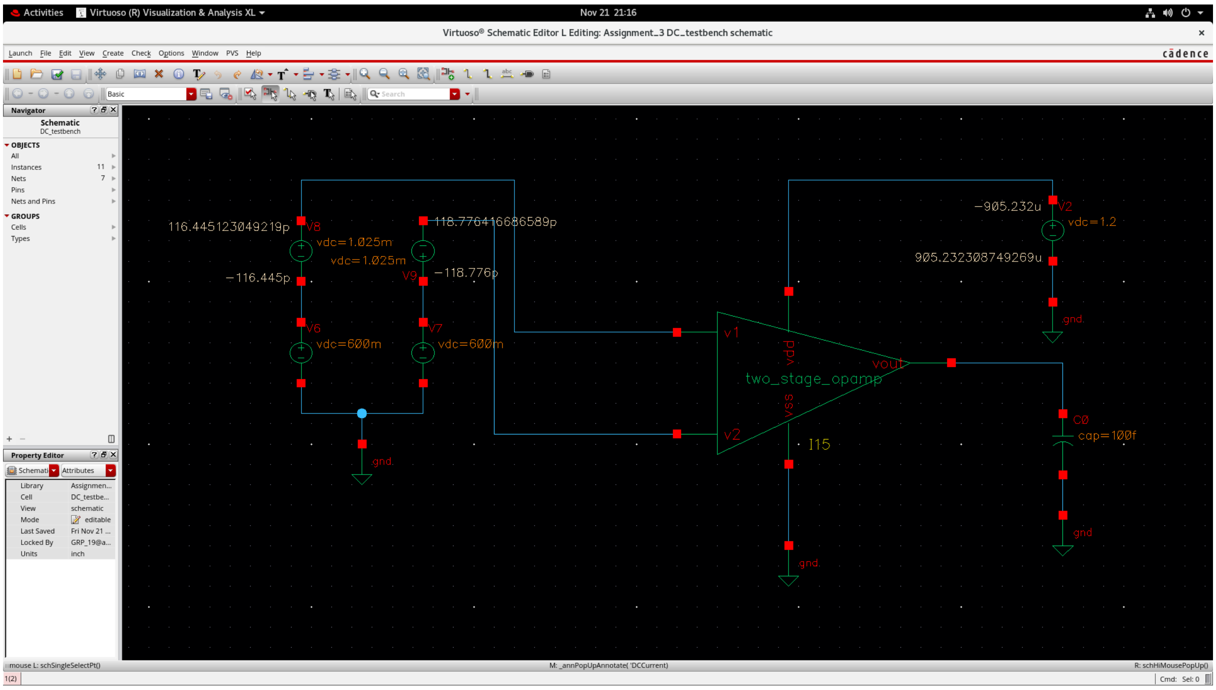


FIGURE 5: Opamp with Vin = Vid

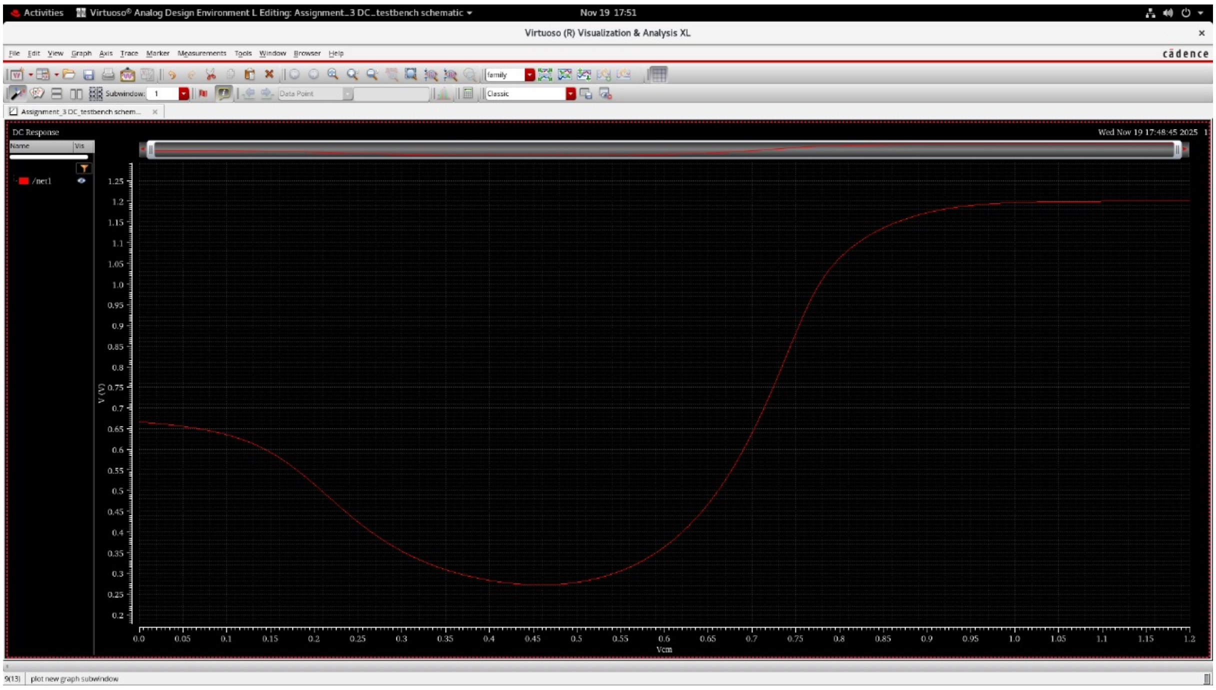


FIGURE 6: CMR Curve

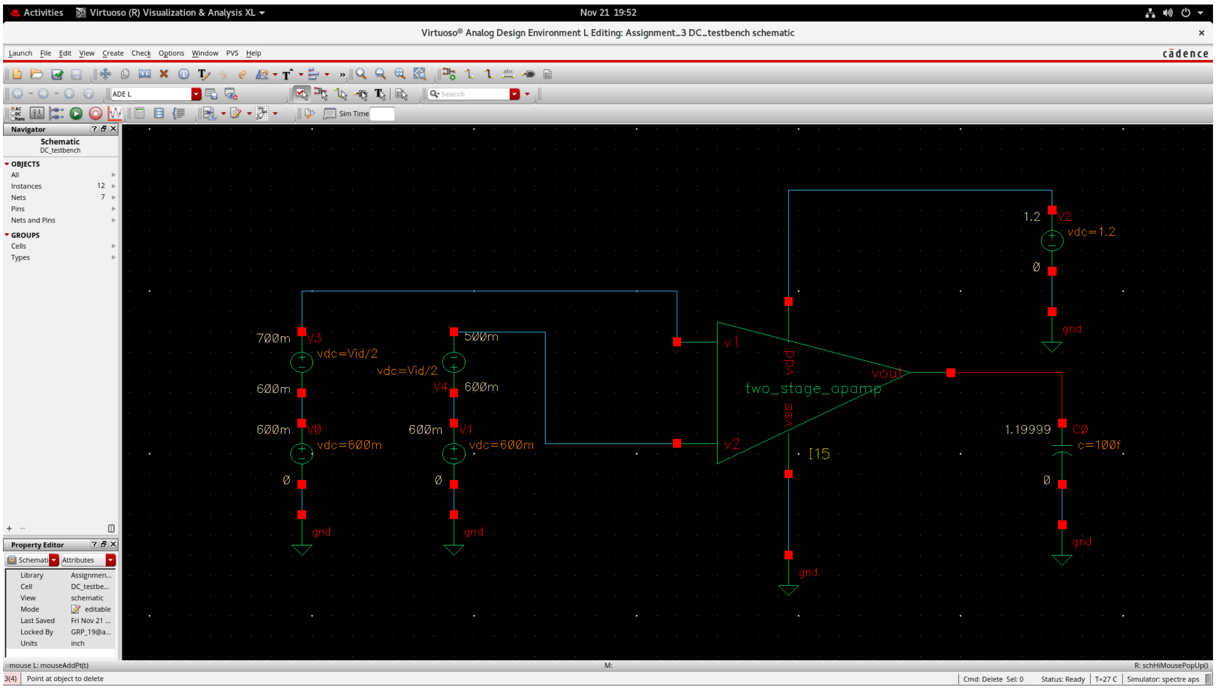


FIGURE 7: VTC Curve with derivative

- Voffset = Vid at which Vout = Vdd/2 = 600m
- Voffset = **2.05mV** ...from VTC
- V1 = Vcm + Voffset/2
- V1 = Vcm - Voffset/2
- DC differential mode voltage gain (Ao) = 600m/2.05m = **292.68**
- DC common mode voltage gain (Acmo) = 392m/600m = **0.653**
- CMRR = Ao/Acmo = 448.21 or **53.03 dB**
- Ibias,p = **116.46 pA**
- Ibias,n = **118.78 pA**
- Ibias = **117.62 pA**
- V- = **9.22 mV** ...from VTC
- V+ = **1.2 V** ...from VTC
- Power dissipation = 1.2V x 937.63uA = **1125.15 uW**

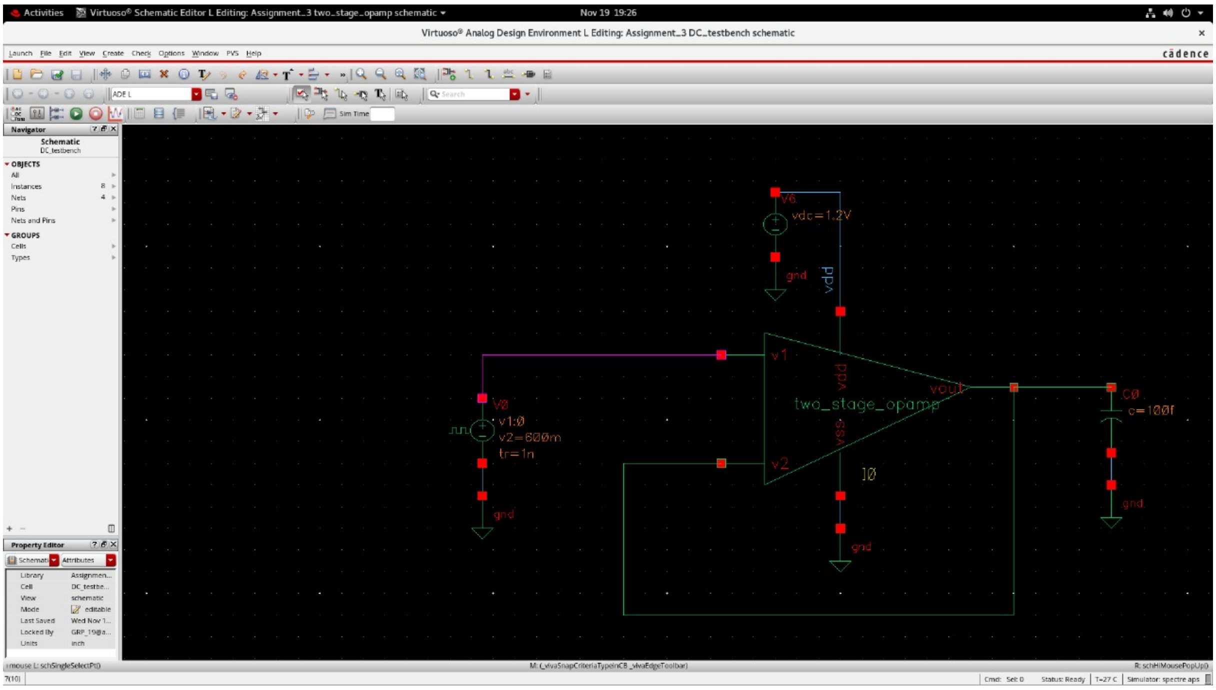
0.3 AC Testbench results

FIGURE 8: AC Response for uncompensated opamp

FIGURE 9: AC response of compensated opamp

- DC Voltage gain (Ao) = **39.17dB**
- -3dB Bandwidth (f-3db) = **5MHz**
- Gain Bandwidth product (GBW) = **446.77MHz**
- Phasef0db = **-95.58 degress**
- Phase Margin = 180 - 95.58 = **84.42 degress**

0.4 Transient Testbench analysis



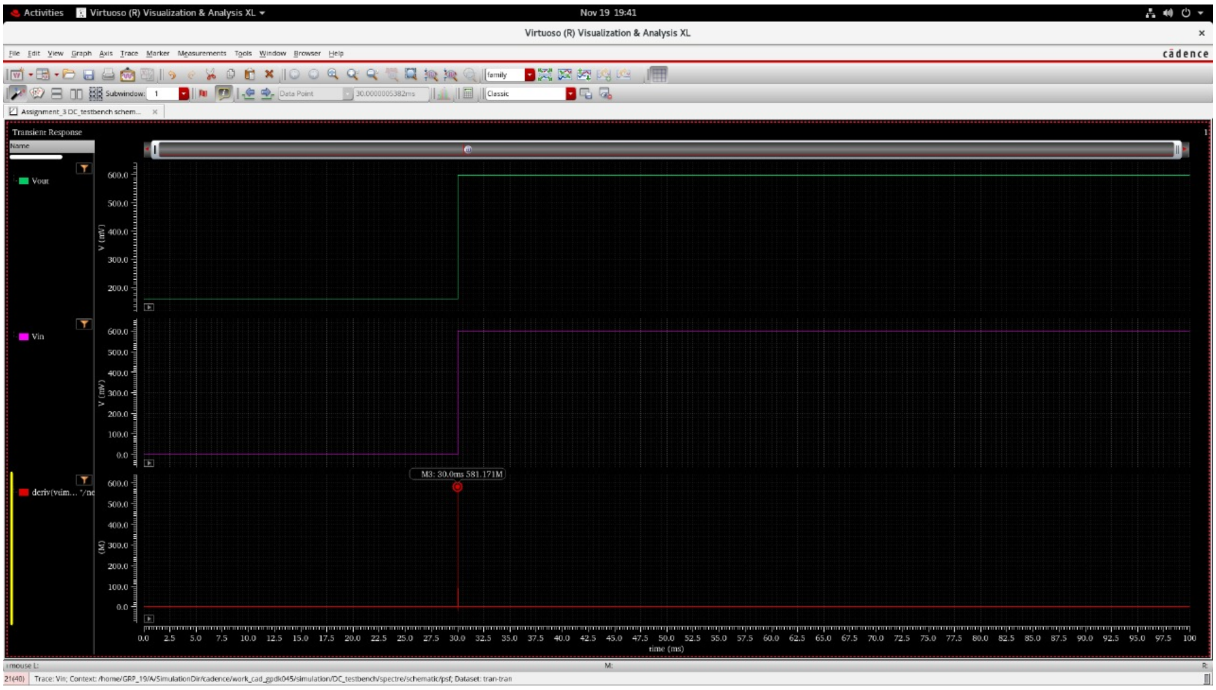


FIGURE 10: Positive step response of compensated opamp

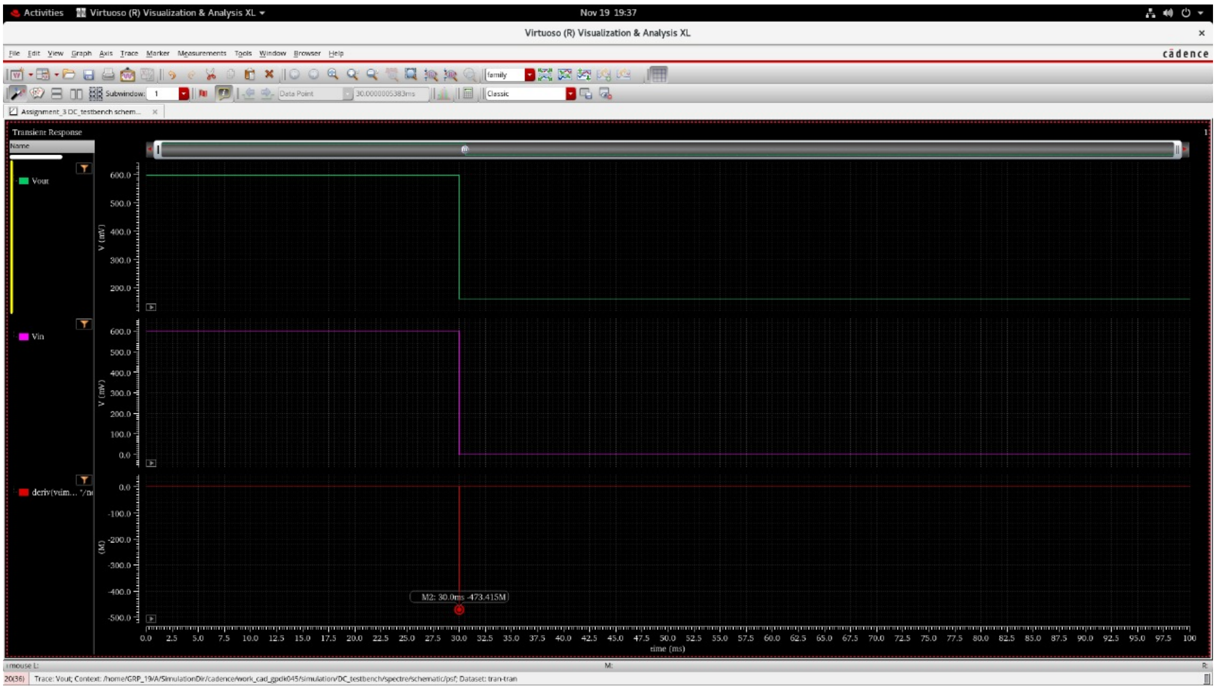


FIGURE 11: Negative step response of compensated opamp

- **SR+ = 581.171 V/us**
- **SR- = 473.415 V/us**

TABLE 2: Performance parameters of designed two stage op-amp @ [$V_{DD} = 1.2\ V$, $C_L = 100\ fF$, $T = 27°C$, $V_{ic} = 0.6\ V$].

S.N.	Parameter	Symbol	Value
1.	Open-loop, differential-mode, DC voltage gain	A_0	$39.17dB$
2.	Open-loop, –3 dB bandwidth (with frequency compensation)	f_{-3dB}	$5\ MHz$
3.	Unity-gain frequency or magnitude crossover frequency	f_T or f_{0dB}	$446.77\ MH$
4.	Phase margin	PM	$84.42°$
5.	Low-frequency common-mode rejection ratio	$CMRR$	$53.03\ dB$
6.	Power dissipation	P_{diss}	$1125.15\ \mu W$
7.	Input-referred offset voltage (systematic)	V_{offset}	$2.05\ mV$
8.	Bias current	I_{bias}	$117.62\ pA$
9.	Slew rate @ 600 mV step	SR^+ SR^-	$581.171\ V/$ $473.415\ V/$

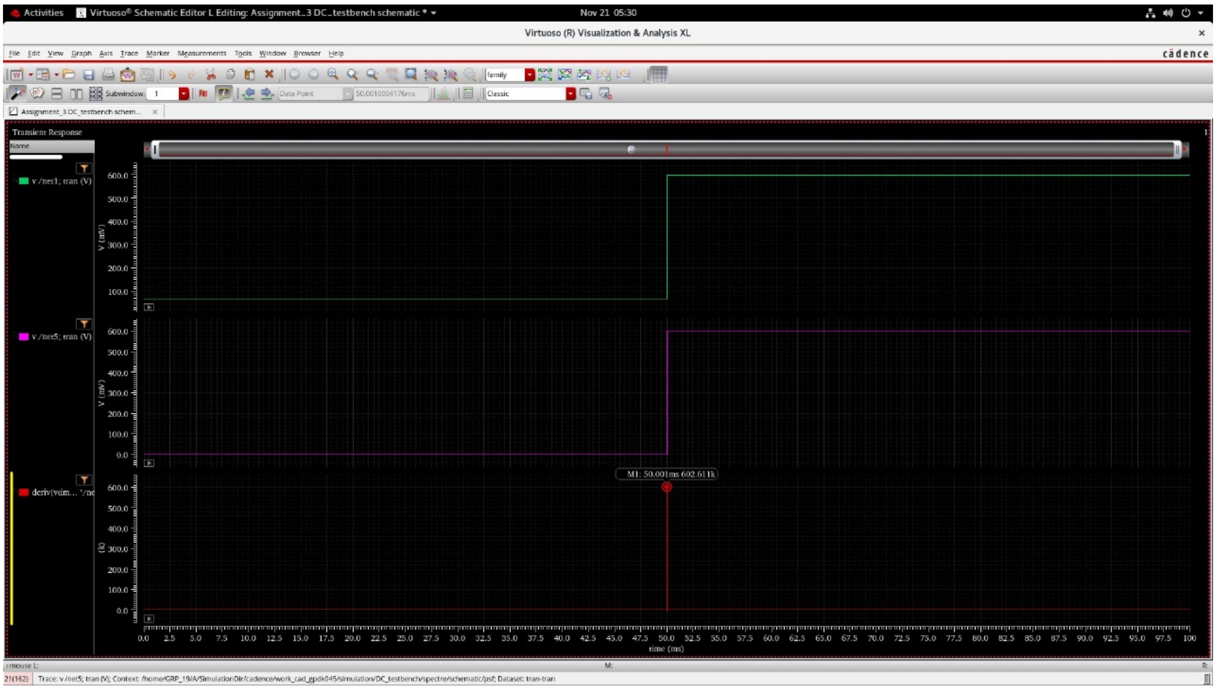


FIGURE 12: Step response of uncompensated opamp

0.5 Include the individual responses in the report to the following:

1. Derive the expression for the overall frequency dependent voltage gain from the differential input to the output voltage. Also, write the expression for the gain-bandwidth product

2. The given topology does not include the output stage. Why is it not essential to employ an output buffer in the internal amplifiers?

3. In negative feedback amplifier, explain, in terms of the circuit parameters (not using the feedback theory), the reason for the bandwidth expansion by the factor of one plus loop gain at the expense of the gain reduction by the same factor.