LAB 4 Report

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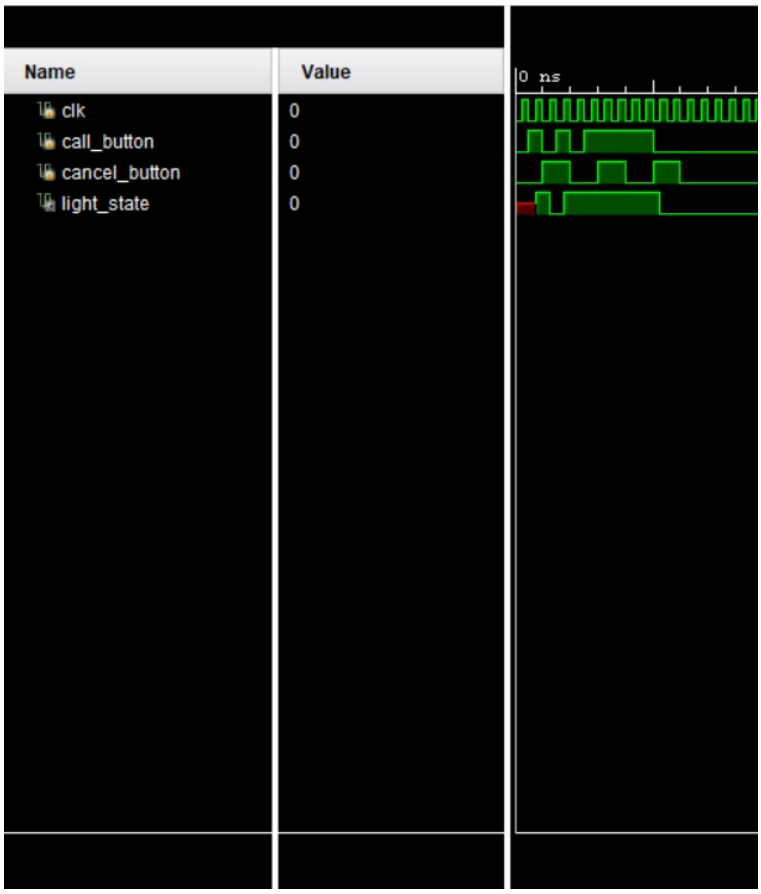
Section: 15295 (Lab Wednesday 12-1)

Checklist:

Part 1 -

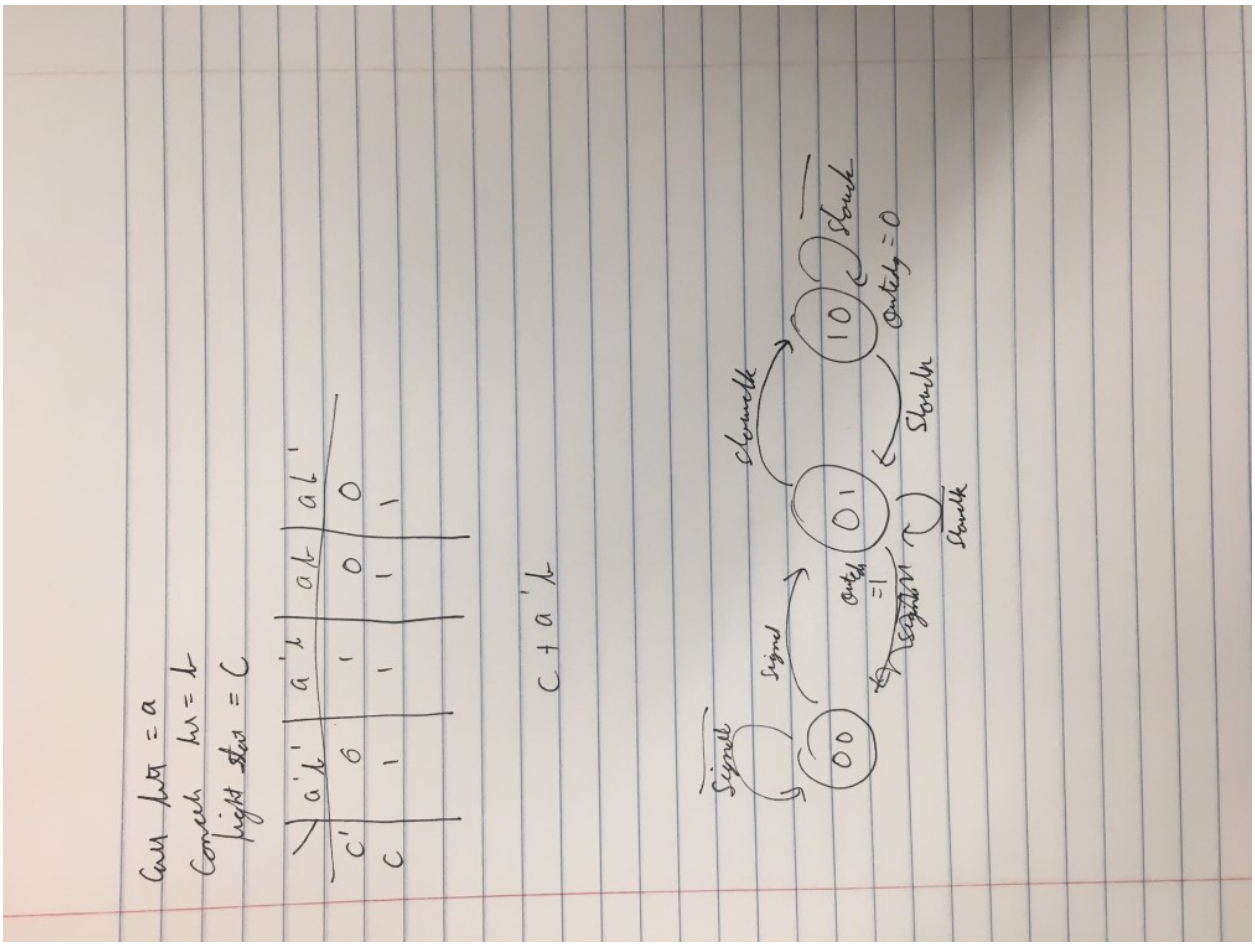
i. Simulation waveform of the Flight Attendant Call System for behavioral as well as dataflow modelling



ii. K-map for minimizing the expression for next_state for dataflow modelling

below

iii.



iv. Boolean expression for next_state for dataflow modelling

above

v. Completed design file (.v) for dataflow modelling

`timescale 1ns / 1ps

//

```
// Company:
// Engineer:
//
// Create Date: 03/06/2018 07:08:25 PM
// Design Name:
// Module Name: flight_attendant_call_system_dataflow
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module flight_attendant_call_system_dataflow(
    input wire clk,
```

```
    input wire call_button,
    input wire cancel_button,
    output reg light_state
    );


    wire next_state;

assign next_state= call_button|(~cancel_button&light_state);


 always@(posedge clk) begin
       light_state<=next_state;
 end




endmodule
```

Part 2 -

vi. State Diagram of the Rising Edge Detector

above

vii. Completed design files (.v) including the top module and clock divider

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 03/07/2018 12:04:57 AM
// Design Name:
// Module Name: rising_edge_detector
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
```

```
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module rising_edge_detector(
    input clk,
    input reset,
    input signal,
    output reg outedge
    );

    wire slow_clk;

    reg[1:0] state;
    reg[1:0] next_state;

    clkdiv c1(clk, reset,slow_clk);

    always @(state) begin

    case(state)
```

```
2'b00 : begin
   outedge= 1'b0;
   if(~signal)
      next_state= 2'b00;
   else
      next_state= 2'b01;

   end

2'b01 : begin

outedge= 1'b1;
next_state= 2'b10;

end

2'b10: begin

outedge= 1'b0;
next_state= 2'b01;
```

```
    end

    default: begin

        next_state=2'b00;
        outedge= 1'b0;
        end

endcase
end

always @(posedge clk) begin
    if(reset)begin
        state <= 2'b00;
        next_state <= 2'b00;
        end
    else
        state <= next_state;

        end
```

```
endmodule



`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 03/07/2018 12:12:33 AM
// Design Name:
// Module Name: clkdiv
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
```

```
//
//////////////////////////////////////////////////////////////////////////////////


module clkdiv(
   input clk,
   input reset,
   output clk_out
   );

   reg [26:0] COUNT;

   assign clk_out= COUNT[16];

   always @(posedge clk)
   begin
  // if (reset)
   //    COUNT=0;
   //else
      COUNT=COUNT+1;
      end
```

```
endmodule
```

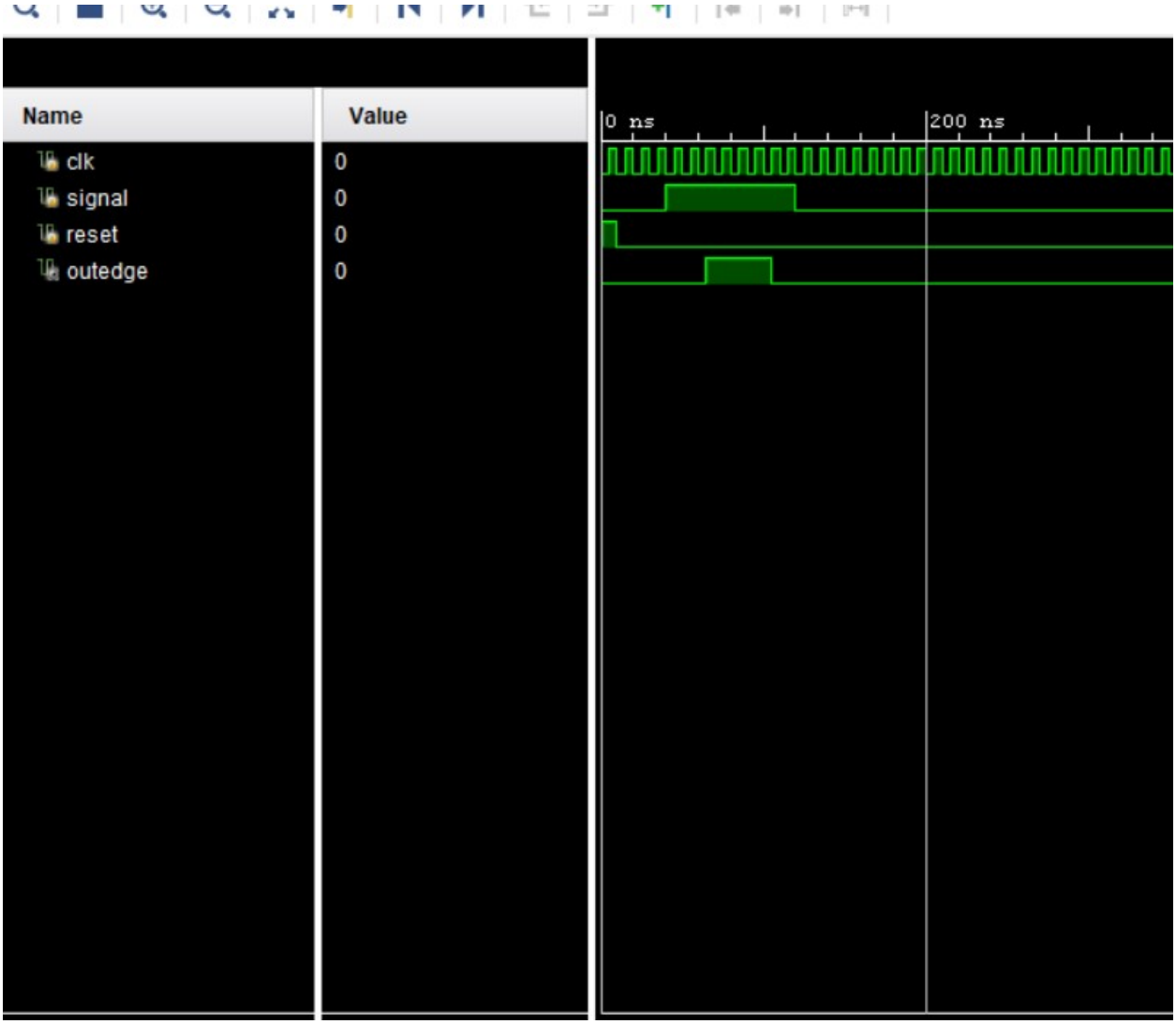
viii. Test-bench of the system

```
`timescale 1ns / 1ps

module tb_rising_edge_detector;

reg clk;
reg signal;
reg reset;

wire outedge;

rising_edge_detector u1(
   .clk(clk),
   .signal(signal),
   .reset(reset),
   .outedge(outedge)
);
```

```
clkdiv u2(
    .clk(clk)
);

initial
begin

clk = 0;
signal = 0;
reset = 1;

#10

signal = 0;
reset = 0;

#30

signal = 1;
reset = 0;
```

```
#40

signal = 1;
reset = 0;
#40

signal = 0;
reset = 0;

end

always
#5 clk = ~clk;

endmodule
```

ix. Simulation waveform



x. Constraints File (Just the uncommented portion)

```
## This file is a general .xdc for the Basys3 rev B board

## To use it in a project:

## - uncomment the lines corresponding to used pins
```

- rename the used ports (in each line, after get_ports) according to the top level signal names in the project

Clock signal

set_property PACKAGE_PIN W5 [get_ports clk]

set_property IOSTANDARD LVCMOS33 [get_ports clk]

create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]

Switches

set_property PACKAGE_PIN V17 [get_ports {signal}]

set_property IOSTANDARD LVCMOS33 [get_ports {signal}]

#set_property PACKAGE_PIN V16 [get_ports {sw[1]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {sw[1]}]

#set_property PACKAGE_PIN W16 [get_ports {sw[2]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {sw[2]}]

#set_property PACKAGE_PIN W17 [get_ports {sw[3]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {sw[3]}]

#set_property PACKAGE_PIN W15 [get_ports {sw[4]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {sw[4]}]

#set_property PACKAGE_PIN V15 [get_ports {sw[5]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {sw[5]}]

```
#set_property PACKAGE_PIN W14 [get_ports {sw[6]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {sw[6]}]
#set_property PACKAGE_PIN W13 [get_ports {sw[7]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {sw[7]}]
#set_property PACKAGE_PIN V2 [get_ports {sw[8]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {sw[8]}]
#set_property PACKAGE_PIN T3 [get_ports {sw[9]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {sw[9]}]
#set_property PACKAGE_PIN T2 [get_ports {sw[10]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {sw[10]}]
#set_property PACKAGE_PIN R3 [get_ports {sw[11]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {sw[11]}]
#set_property PACKAGE_PIN W2 [get_ports {sw[12]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {sw[12]}]
#set_property PACKAGE_PIN U1 [get_ports {sw[13]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {sw[13]}]
#set_property PACKAGE_PIN T1 [get_ports {sw[14]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {sw[14]}]
#set_property PACKAGE_PIN R2 [get_ports {sw[15]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {sw[15]}]
```

```
## LEDs
set_property PACKAGE_PIN U16 [get_ports {outedge}]
	set_property IOSTANDARD LVCMOS33 [get_ports {outedge}]
#set_property PACKAGE_PIN E19 [get_ports {led[1]}]
	#set_property IOSTANDARD LVCMOS33 [get_ports {led[1]}]
#set_property PACKAGE_PIN U19 [get_ports {led[2]}]
	#set_property IOSTANDARD LVCMOS33 [get_ports {led[2]}]
#set_property PACKAGE_PIN V19 [get_ports {led[3]}]
	#set_property IOSTANDARD LVCMOS33 [get_ports {led[3]}]
#set_property PACKAGE_PIN W18 [get_ports {led[4]}]
	#set_property IOSTANDARD LVCMOS33 [get_ports {led[4]}]
#set_property PACKAGE_PIN U15 [get_ports {led[5]}]
	#set_property IOSTANDARD LVCMOS33 [get_ports {led[5]}]
#set_property PACKAGE_PIN U14 [get_ports {led[6]}]
	#set_property IOSTANDARD LVCMOS33 [get_ports {led[6]}]
#set_property PACKAGE_PIN V14 [get_ports {led[7]}]
	#set_property IOSTANDARD LVCMOS33 [get_ports {led[7]}]
#set_property PACKAGE_PIN V13 [get_ports {led[8]}]
	#set_property IOSTANDARD LVCMOS33 [get_ports {led[8]}]
#set_property PACKAGE_PIN V3 [get_ports {led[9]}]
	#set_property IOSTANDARD LVCMOS33 [get_ports {led[9]}]
#set_property PACKAGE_PIN W3 [get_ports {led[10]}]
```

#set_property IOSTANDARD LVCMOS33 [get_ports {led[10]}]

#set_property PACKAGE_PIN U3 [get_ports {led[11]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {led[11]}]

#set_property PACKAGE_PIN P3 [get_ports {led[12]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {led[12]}]

#set_property PACKAGE_PIN N3 [get_ports {led[13]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {led[13]}]

#set_property PACKAGE_PIN P1 [get_ports {led[14]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {led[14]}]

#set_property PACKAGE_PIN L1 [get_ports {led[15]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {led[15]}]

##7 segment display

#set_property PACKAGE_PIN W7 [get_ports {seg[0]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {seg[0]}]

#set_property PACKAGE_PIN W6 [get_ports {seg[1]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {seg[1]}]

#set_property PACKAGE_PIN U8 [get_ports {seg[2]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {seg[2]}]

#set_property PACKAGE_PIN V8 [get_ports {seg[3]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {seg[3]}]

```
#set_property PACKAGE_PIN U5 [get_ports {seg[4]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {seg[4]}]
#set_property PACKAGE_PIN V5 [get_ports {seg[5]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {seg[5]}]
#set_property PACKAGE_PIN U7 [get_ports {seg[6]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {seg[6]}]

#set_property PACKAGE_PIN V7 [get_ports dp]

        #set_property IOSTANDARD LVCMOS33 [get_ports dp]

#set_property PACKAGE_PIN U2 [get_ports {an[0]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {an[0]}]
#set_property PACKAGE_PIN U4 [get_ports {an[1]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {an[1]}]
#set_property PACKAGE_PIN V4 [get_ports {an[2]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {an[2]}]
#set_property PACKAGE_PIN W4 [get_ports {an[3]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {an[3]}]


##Buttons
```

```
set_property PACKAGE_PIN U18 [get_ports reset]
        set_property IOSTANDARD LVCMOS33 [get_ports reset]
#set_property PACKAGE_PIN T18 [get_ports btnU]
        #set_property IOSTANDARD LVCMOS33 [get_ports btnU]
#set_property PACKAGE_PIN W19 [get_ports btnL]

        #set_property IOSTANDARD LVCMOS33 [get_ports btnL]
#set_property PACKAGE_PIN T17 [get_ports btnR]
        #set_property IOSTANDARD LVCMOS33 [get_ports btnR]
#set_property PACKAGE_PIN U17 [get_ports btnD]

        #set_property IOSTANDARD LVCMOS33 [get_ports btnD]



##Pmod Header JA
##Sch name = JA1
#set_property PACKAGE_PIN J1 [get_ports {JA[0]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JA[0]}]
##Sch name = JA2
#set_property PACKAGE_PIN L2 [get_ports {JA[1]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JA[1]}]
```

```
##Sch name = JA3
#set_property PACKAGE_PIN J2 [get_ports {JA[2]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JA[2]}]
##Sch name = JA4
#set_property PACKAGE_PIN G2 [get_ports {JA[3]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JA[3]}]
##Sch name = JA7
#set_property PACKAGE_PIN H1 [get_ports {JA[4]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JA[4]}]
##Sch name = JA8
#set_property PACKAGE_PIN K2 [get_ports {JA[5]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JA[5]}]
##Sch name = JA9
#set_property PACKAGE_PIN H2 [get_ports {JA[6]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JA[6]}]
##Sch name = JA10
#set_property PACKAGE_PIN G3 [get_ports {JA[7]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JA[7]}]




##Pmod Header JB
```

```
##Sch name = JB1
#set_property PACKAGE_PIN A14 [get_ports {JB[0]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JB[0]}]
##Sch name = JB2
#set_property PACKAGE_PIN A16 [get_ports {JB[1]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JB[1]}]
##Sch name = JB3
#set_property PACKAGE_PIN B15 [get_ports {JB[2]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JB[2]}]
##Sch name = JB4
#set_property PACKAGE_PIN B16 [get_ports {JB[3]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JB[3]}]
##Sch name = JB7
#set_property PACKAGE_PIN A15 [get_ports {JB[4]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JB[4]}]
##Sch name = JB8
#set_property PACKAGE_PIN A17 [get_ports {JB[5]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JB[5]}]
##Sch name = JB9
#set_property PACKAGE_PIN C15 [get_ports {JB[6]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JB[6]}]
##Sch name = JB10
```

```
#set_property PACKAGE_PIN C16 [get_ports {JB[7]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JB[7]}]



##Pmod Header JC
##Sch name = JC1
#set_property PACKAGE_PIN K17 [get_ports {JC[0]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JC[0]}]
##Sch name = JC2
#set_property PACKAGE_PIN M18 [get_ports {JC[1]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JC[1]}]
##Sch name = JC3
#set_property PACKAGE_PIN N17 [get_ports {JC[2]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JC[2]}]
##Sch name = JC4
#set_property PACKAGE_PIN P18 [get_ports {JC[3]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JC[3]}]
##Sch name = JC7
#set_property PACKAGE_PIN L17 [get_ports {JC[4]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JC[4]}]
##Sch name = JC8
```

```
#set_property PACKAGE_PIN M19 [get_ports {JC[5]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JC[5]}]
##Sch name = JC9
#set_property PACKAGE_PIN P17 [get_ports {JC[6]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JC[6]}]
##Sch name = JC10
#set_property PACKAGE_PIN R18 [get_ports {JC[7]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JC[7]}]



##Pmod Header JXADC
##Sch name = XA1_P
#set_property PACKAGE_PIN J3 [get_ports {JXADC[0]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JXADC[0]}]
##Sch name = XA2_P
#set_property PACKAGE_PIN L3 [get_ports {JXADC[1]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JXADC[1]}]
##Sch name = XA3_P
#set_property PACKAGE_PIN M2 [get_ports {JXADC[2]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JXADC[2]}]
##Sch name = XA4_P
#set_property PACKAGE_PIN N2 [get_ports {JXADC[3]}]
```

```
        #set_property IOSTANDARD LVCMOS33 [get_ports {JXADC[3]}]
##Sch name = XA1_N
#set_property PACKAGE_PIN K3 [get_ports {JXADC[4]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JXADC[4]}]
##Sch name = XA2_N
#set_property PACKAGE_PIN M3 [get_ports {JXADC[5]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JXADC[5]}]
##Sch name = XA3_N
#set_property PACKAGE_PIN M1 [get_ports {JXADC[6]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JXADC[6]}]
##Sch name = XA4_N
#set_property PACKAGE_PIN N1 [get_ports {JXADC[7]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JXADC[7]}]




##VGA Connector
#set_property PACKAGE_PIN G19 [get_ports {vgaRed[0]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {vgaRed[0]}]
#set_property PACKAGE_PIN H19 [get_ports {vgaRed[1]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {vgaRed[1]}]
#set_property PACKAGE_PIN J19 [get_ports {vgaRed[2]}]
```

#set_property IOSTANDARD LVCMOS33 [get_ports {vgaRed[2]}]

#set_property PACKAGE_PIN N19 [get_ports {vgaRed[3]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {vgaRed[3]}]

#set_property PACKAGE_PIN N18 [get_ports {vgaBlue[0]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {vgaBlue[0]}]

#set_property PACKAGE_PIN L18 [get_ports {vgaBlue[1]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {vgaBlue[1]}]

#set_property PACKAGE_PIN K18 [get_ports {vgaBlue[2]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {vgaBlue[2]}]

#set_property PACKAGE_PIN J18 [get_ports {vgaBlue[3]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {vgaBlue[3]}]

#set_property PACKAGE_PIN J17 [get_ports {vgaGreen[0]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {vgaGreen[0]}]

#set_property PACKAGE_PIN H17 [get_ports {vgaGreen[1]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {vgaGreen[1]}]

#set_property PACKAGE_PIN G17 [get_ports {vgaGreen[2]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {vgaGreen[2]}]

#set_property PACKAGE_PIN D17 [get_ports {vgaGreen[3]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {vgaGreen[3]}]

#set_property PACKAGE_PIN P19 [get_ports Hsync]

#set_property IOSTANDARD LVCMOS33 [get_ports Hsync]

```
#set_property PACKAGE_PIN R19 [get_ports Vsync]

        #set_property IOSTANDARD LVCMOS33 [get_ports Vsync]


##USB-RS232 Interface
#set_property PACKAGE_PIN B18 [get_ports RsRx]
        #set_property IOSTANDARD LVCMOS33 [get_ports RsRx]
#set_property PACKAGE_PIN A18 [get_ports RsTx]
        #set_property IOSTANDARD LVCMOS33 [get_ports RsTx]


##USB HID (PS/2)
#set_property PACKAGE_PIN C17 [get_ports PS2Clk]

        #set_property IOSTANDARD LVCMOS33 [get_ports PS2Clk]
        #set_property PULLUP true [get_ports PS2Clk]
#set_property PACKAGE_PIN B17 [get_ports PS2Data]
        #set_property IOSTANDARD LVCMOS33 [get_ports PS2Data]
        #set_property PULLUP true [get_ports PS2Data]
```

##Quad SPI Flash

##Note that CCLK_0 cannot be placed in 7 series devices. You can access it using the

##STARTUPE2 primitive.

#set_property PACKAGE_PIN D18 [get_ports {QspiDB[0]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {QspiDB[0]}]

#set_property PACKAGE_PIN D19 [get_ports {QspiDB[1]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {QspiDB[1]}]

#set_property PACKAGE_PIN G18 [get_ports {QspiDB[2]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {QspiDB[2]}]

#set_property PACKAGE_PIN F18 [get_ports {QspiDB[3]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {QspiDB[3]}]

#set_property PACKAGE_PIN K19 [get_ports QspiCSn]

#set_property IOSTANDARD LVCMOS33 [get_ports QspiCSn]

Part 3 -

xi. Completed design files (.v) of all the modules in the system

`timescale 1ns / 1ps

```
module clkdiv(
    input clk,
    input reset,
    output slow_clk
    );

    reg [25:0] COUNT;

    assign slow_clk = COUNT[25];
    always @(posedge clk) begin
        if(reset)
            COUNT = 0;
        else
            COUNT = COUNT + 1;
        end
endmodule


`timescale 1ns / 1ps
```

```
module hexto7segment(
   input [3:0] x,
   output reg [6:0] r
   );
   always @(*)
      case(x)
         4'b0000 :   r = 7'b0000001;
         4'b0001 :   r = 7'b1001111;
         4'b0010 :   r = 7'b0010010;
         4'b0011 :   r = 7'b0000110;
         4'b0100 :   r = 7'b1001100;
         4'b0101 :   r = 7'b0100100;
         4'b0110 :   r = 7'b0100000;
         4'b0111 :   r = 7'b0001111;
         4'b1000 :   r = 7'b0000000;
         4'b1001 :   r = 7'b0001100;
         4'b1010 :   r = 7'b1111111;
         4'b1011 :   r = 7'b1111111;
         4'b1100 :   r = 7'b1111111;
         4'b1101 :   r = 7'b1111111;
```

```
            4'b1110 :   r = 7'b1111111;
            4'b1111 :   r = 7'b1111111;
        endcase
endmodule
`timescale 1ns / 1ps

module tb_time_multiplexing_main;

    reg clk;
    reg reset;
    reg [15:0]sw;

    wire [3:0] an;
    wire [6:0] sseg;

time_multiplexing_main u1(
    .clk(clk),
    .reset(reset),
    .sw(sw),
    .an(an),
    .sseg(sseg)
);
```

```
initial begin



sw = 16'h0000;

clk = 0;

reset = 0;


#30

reset = 0;

sw = 16'h0008;


#30;

reset = 0;

sw = 16'h4321;


#30;

reset = 0;

sw = 16'h0002;


#30;

reset = 0;
```

```
sw = 16'h0302;
end


always
#5 clk = ~clk;

endmodule

`timescale 1ns / 1ps


module time_multiplexing_main(
    input clk,
    input reset,
    input [15:0] sw,
    output [3:0] an,
    output [6:0] sseg);

    wire [6:0] in0, in1, in2, in3 ;

    wire slow_clk;
```

```
    hexto7segment c1 (.x(sw[3:0]), .r(in0));
    hexto7segment c2 (.x(sw[7:4]), .r(in1));
    hexto7segment c3 (.x(sw[11:8]), .r(in2));
    hexto7segment c4 (.x(sw[15:12]), .r(in3));

    clkdiv c5 (.clk(clk), .reset(reset), .slow_clk(slow_clk));

    time_mux_state_machine c6(
       .clk (slow_clk),
       .reset (reset),
       .in0 (in0),
       .in1 (in1),
       .in2 (in2),
       .in3 (in3),
       .an (an),
       .sseg (sseg));

Endmodule
```

```
`timescale 1ns / 1ps


module time_mux_state_machine(
    input clk,
    input reset,
    input [6:0] in0,
    input [6:0] in1,
    input [6:0] in2,
    input [6:0] in3,
    output reg [3:0] an,
    output reg [6:0] sseg
    );


    reg [1:0] state;
    reg [1:0] next_state;


    always @(*) begin
        case(state)
            2'b00: next_state = 2'b01;
            2'b01: next_state = 2'b10;
            2'b10: next_state = 2'b11;
            2'b11: next_state = 2'b00;
```

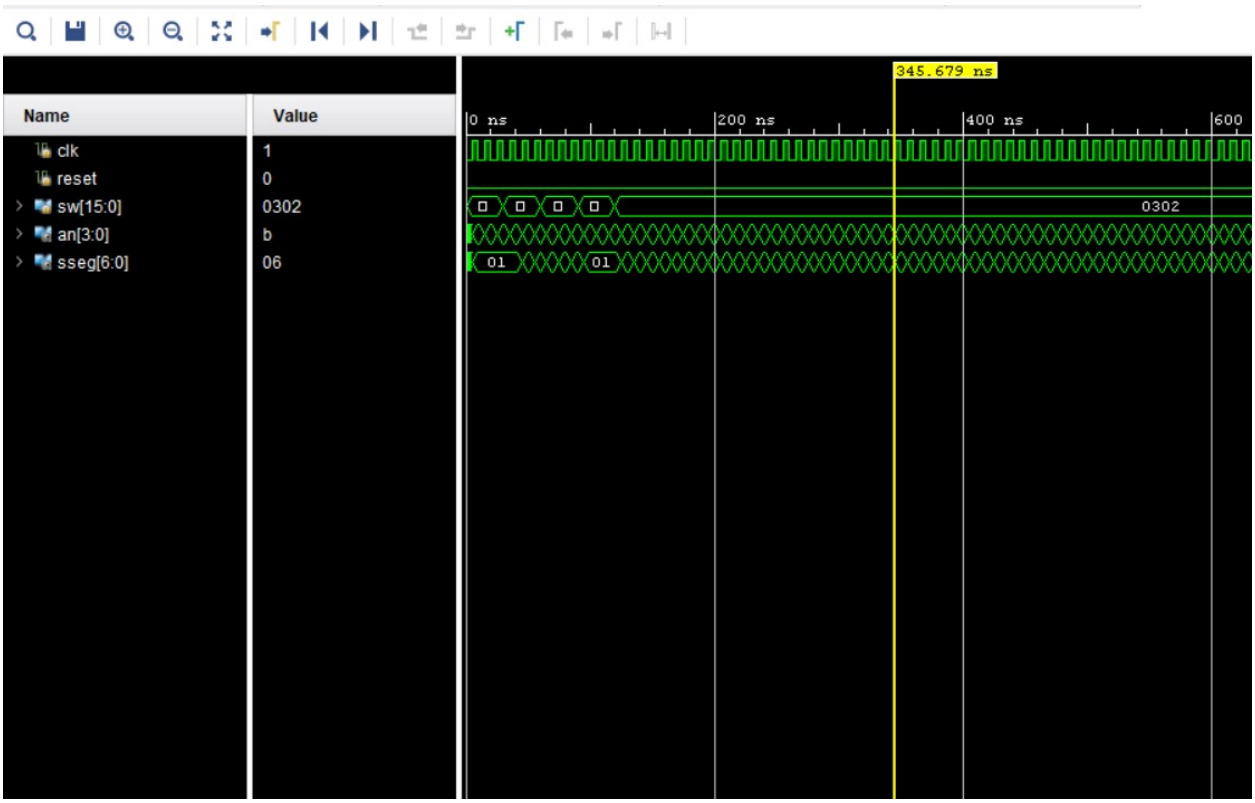
```
    endcase
end

always @(*) begin
    case(state)
        2'b00: sseg = in0;
        2'b01: sseg = in1;
        2'b10: sseg = in2;
        2'b11: sseg = in3;
    endcase

    case(state)
        2'b00: an = 4'b1110;
        2'b01: an = 4'b1101;
        2'b10: an = 4'b1011;
        2'b11: an = 4'b0111;
    endcase
end

always @(posedge clk or posedge reset) begin
    if(reset)
        state <= 2'b00;
```

```
        else
            state <= next_state;
    end

endmodule
```

xii. Test-bench of the system

Above

xiii. Simulation waveform



xiv. Constraints File (Just the uncommented portion)

This file is a general .xdc for the Basys3 rev B board

To use it in a project:

- uncomment the lines corresponding to used pins

- rename the used ports (in each line, after get_ports) according to the top level signal names in the project

Clock signal

set_property PACKAGE_PIN W5 [get_ports {clk}]

```
        set_property IOSTANDARD LVCMOS33 [get_ports {clk}]

        create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports {clk}]


## Switches
set_property PACKAGE_PIN V17 [get_ports {sw[0]}]

        set_property IOSTANDARD LVCMOS33 [get_ports {sw[0]}]

set_property PACKAGE_PIN V16 [get_ports {sw[1]}]

        set_property IOSTANDARD LVCMOS33 [get_ports {sw[1]}]

set_property PACKAGE_PIN W16 [get_ports {sw[2]}]

        set_property IOSTANDARD LVCMOS33 [get_ports {sw[2]}]

set_property PACKAGE_PIN W17 [get_ports {sw[3]}]

        set_property IOSTANDARD LVCMOS33 [get_ports {sw[3]}]

set_property PACKAGE_PIN W15 [get_ports {sw[4]}]

        set_property IOSTANDARD LVCMOS33 [get_ports {sw[4]}]

set_property PACKAGE_PIN V15 [get_ports {sw[5]}]

        set_property IOSTANDARD LVCMOS33 [get_ports {sw[5]}]

set_property PACKAGE_PIN W14 [get_ports {sw[6]}]

        set_property IOSTANDARD LVCMOS33 [get_ports {sw[6]}]

set_property PACKAGE_PIN W13 [get_ports {sw[7]}]

        set_property IOSTANDARD LVCMOS33 [get_ports {sw[7]}]

set_property PACKAGE_PIN V2 [get_ports {sw[8]}]
```

```
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[8]}]
set_property PACKAGE_PIN T3 [get_ports {sw[9]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[9]}]
set_property PACKAGE_PIN T2 [get_ports {sw[10]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[10]}]
set_property PACKAGE_PIN R3 [get_ports {sw[11]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[11]}]
set_property PACKAGE_PIN W2 [get_ports {sw[12]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[12]}]
set_property PACKAGE_PIN U1 [get_ports {sw[13]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[13]}]
set_property PACKAGE_PIN T1 [get_ports {sw[14]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[14]}]
set_property PACKAGE_PIN R2 [get_ports {sw[15]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[15]}]



## LEDs
#set_property PACKAGE_PIN U16 [get_ports {led[0]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {led[0]}]
#set_property PACKAGE_PIN E19 [get_ports {led[1]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {led[1]}]
```

```
#set_property PACKAGE_PIN U19 [get_ports {led[2]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {led[2]}]
#set_property PACKAGE_PIN V19 [get_ports {led[3]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {led[3]}]
#set_property PACKAGE_PIN W18 [get_ports {led[4]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {led[4]}]
#set_property PACKAGE_PIN U15 [get_ports {led[5]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {led[5]}]
#set_property PACKAGE_PIN U14 [get_ports {led[6]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {led[6]}]
#set_property PACKAGE_PIN V14 [get_ports {led[7]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {led[7]}]
#set_property PACKAGE_PIN V13 [get_ports {led[8]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {led[8]}]
#set_property PACKAGE_PIN V3 [get_ports {led[9]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {led[9]}]
#set_property PACKAGE_PIN W3 [get_ports {led[10]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {led[10]}]
#set_property PACKAGE_PIN U3 [get_ports {led[11]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {led[11]}]
#set_property PACKAGE_PIN P3 [get_ports {led[12]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {led[12]}]
```

```
#set_property PACKAGE_PIN N3 [get_ports {led[13]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {led[13]}]
#set_property PACKAGE_PIN P1 [get_ports {led[14]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {led[14]}]
#set_property PACKAGE_PIN L1 [get_ports {led[15]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {led[15]}]



##7 segment display
set_property PACKAGE_PIN W7 [get_ports {sseg[6]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sseg[6]}]
set_property PACKAGE_PIN W6 [get_ports {sseg[5]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sseg[5]}]
set_property PACKAGE_PIN U8 [get_ports {sseg[4]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sseg[4]}]
set_property PACKAGE_PIN V8 [get_ports {sseg[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sseg[3]}]
set_property PACKAGE_PIN U5 [get_ports {sseg[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sseg[2]}]
set_property PACKAGE_PIN V5 [get_ports {sseg[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sseg[1]}]
set_property PACKAGE_PIN U7 [get_ports {sseg[0]}]
```

```
        set_property IOSTANDARD LVCMOS33 [get_ports {sseg[0]}]


#set_property PACKAGE_PIN V7 [get_ports dp]

        #set_property IOSTANDARD LVCMOS33 [get_ports dp]


set_property PACKAGE_PIN U2 [get_ports {an[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {an[0]}]
set_property PACKAGE_PIN U4 [get_ports {an[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {an[1]}]
set_property PACKAGE_PIN V4 [get_ports {an[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {an[2]}]
set_property PACKAGE_PIN W4 [get_ports {an[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {an[3]}]



##Buttons
set_property PACKAGE_PIN U18 [get_ports reset]
        set_property IOSTANDARD LVCMOS33 [get_ports reset]
#set_property PACKAGE_PIN T18 [get_ports btnU]
        #set_property IOSTANDARD LVCMOS33 [get_ports btnU]
```

```
#set_property PACKAGE_PIN W19 [get_ports btnL]

        #set_property IOSTANDARD LVCMOS33 [get_ports btnL]
#set_property PACKAGE_PIN T17 [get_ports btnR]
        #set_property IOSTANDARD LVCMOS33 [get_ports btnR]
#set_property PACKAGE_PIN U17 [get_ports btnD]

        #set_property IOSTANDARD LVCMOS33 [get_ports btnD]




##Pmod Header JA
##Sch name = JA1
#set_property PACKAGE_PIN J1 [get_ports {JA[0]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JA[0]}]
##Sch name = JA2
#set_property PACKAGE_PIN L2 [get_ports {JA[1]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JA[1]}]
##Sch name = JA3
#set_property PACKAGE_PIN J2 [get_ports {JA[2]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JA[2]}]
##Sch name = JA4
```

```
#set_property PACKAGE_PIN G2 [get_ports {JA[3]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JA[3]}]
##Sch name = JA7
#set_property PACKAGE_PIN H1 [get_ports {JA[4]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JA[4]}]
##Sch name = JA8
#set_property PACKAGE_PIN K2 [get_ports {JA[5]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JA[5]}]
##Sch name = JA9
#set_property PACKAGE_PIN H2 [get_ports {JA[6]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JA[6]}]
##Sch name = JA10
#set_property PACKAGE_PIN G3 [get_ports {JA[7]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JA[7]}]



##Pmod Header JB
##Sch name = JB1
#set_property PACKAGE_PIN A14 [get_ports {JB[0]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JB[0]}]
##Sch name = JB2
```

```
#set_property PACKAGE_PIN A16 [get_ports {JB[1]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JB[1]}]
##Sch name = JB3
#set_property PACKAGE_PIN B15 [get_ports {JB[2]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JB[2]}]
##Sch name = JB4
#set_property PACKAGE_PIN B16 [get_ports {JB[3]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JB[3]}]
##Sch name = JB7
#set_property PACKAGE_PIN A15 [get_ports {JB[4]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JB[4]}]
##Sch name = JB8
#set_property PACKAGE_PIN A17 [get_ports {JB[5]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JB[5]}]
##Sch name = JB9
#set_property PACKAGE_PIN C15 [get_ports {JB[6]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JB[6]}]
##Sch name = JB10
#set_property PACKAGE_PIN C16 [get_ports {JB[7]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JB[7]}]
```

```
##Pmod Header JC
##Sch name = JC1
#set_property PACKAGE_PIN K17 [get_ports {JC[0]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JC[0]}]
##Sch name = JC2
#set_property PACKAGE_PIN M18 [get_ports {JC[1]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JC[1]}]
##Sch name = JC3
#set_property PACKAGE_PIN N17 [get_ports {JC[2]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JC[2]}]
##Sch name = JC4
#set_property PACKAGE_PIN P18 [get_ports {JC[3]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JC[3]}]
##Sch name = JC7
#set_property PACKAGE_PIN L17 [get_ports {JC[4]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JC[4]}]
##Sch name = JC8
#set_property PACKAGE_PIN M19 [get_ports {JC[5]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JC[5]}]
##Sch name = JC9
#set_property PACKAGE_PIN P17 [get_ports {JC[6]}]
```

```
        #set_property IOSTANDARD LVCMOS33 [get_ports {JC[6]}]
##Sch name = JC10
#set_property PACKAGE_PIN R18 [get_ports {JC[7]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JC[7]}]



##Pmod Header JXADC
##Sch name = XA1_P
#set_property PACKAGE_PIN J3 [get_ports {JXADC[0]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JXADC[0]}]
##Sch name = XA2_P
#set_property PACKAGE_PIN L3 [get_ports {JXADC[1]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JXADC[1]}]
##Sch name = XA3_P
#set_property PACKAGE_PIN M2 [get_ports {JXADC[2]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JXADC[2]}]
##Sch name = XA4_P
#set_property PACKAGE_PIN N2 [get_ports {JXADC[3]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JXADC[3]}]
##Sch name = XA1_N
#set_property PACKAGE_PIN K3 [get_ports {JXADC[4]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JXADC[4]}]
```

```
##Sch name = XA2_N
#set_property PACKAGE_PIN M3 [get_ports {JXADC[5]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JXADC[5]}]
##Sch name = XA3_N
#set_property PACKAGE_PIN M1 [get_ports {JXADC[6]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JXADC[6]}]
##Sch name = XA4_N
#set_property PACKAGE_PIN N1 [get_ports {JXADC[7]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {JXADC[7]}]




##VGA Connector
#set_property PACKAGE_PIN G19 [get_ports {vgaRed[0]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {vgaRed[0]}]
#set_property PACKAGE_PIN H19 [get_ports {vgaRed[1]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {vgaRed[1]}]
#set_property PACKAGE_PIN J19 [get_ports {vgaRed[2]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {vgaRed[2]}]
#set_property PACKAGE_PIN N19 [get_ports {vgaRed[3]}]
        #set_property IOSTANDARD LVCMOS33 [get_ports {vgaRed[3]}]
#set_property PACKAGE_PIN N18 [get_ports {vgaBlue[0]}]
```

#set_property IOSTANDARD LVCMOS33 [get_ports {vgaBlue[0]}]

#set_property PACKAGE_PIN L18 [get_ports {vgaBlue[1]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {vgaBlue[1]}]

#set_property PACKAGE_PIN K18 [get_ports {vgaBlue[2]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {vgaBlue[2]}]

#set_property PACKAGE_PIN J18 [get_ports {vgaBlue[3]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {vgaBlue[3]}]

#set_property PACKAGE_PIN J17 [get_ports {vgaGreen[0]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {vgaGreen[0]}]

#set_property PACKAGE_PIN H17 [get_ports {vgaGreen[1]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {vgaGreen[1]}]

#set_property PACKAGE_PIN G17 [get_ports {vgaGreen[2]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {vgaGreen[2]}]

#set_property PACKAGE_PIN D17 [get_ports {vgaGreen[3]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {vgaGreen[3]}]

#set_property PACKAGE_PIN P19 [get_ports Hsync]

#set_property IOSTANDARD LVCMOS33 [get_ports Hsync]

#set_property PACKAGE_PIN R19 [get_ports Vsync]

#set_property IOSTANDARD LVCMOS33 [get_ports Vsync]

##USB-RS232 Interface

#set_property PACKAGE_PIN B18 [get_ports RsRx]

#set_property IOSTANDARD LVCMOS33 [get_ports RsRx]

#set_property PACKAGE_PIN A18 [get_ports RsTx]

#set_property IOSTANDARD LVCMOS33 [get_ports RsTx]

##USB HID (PS/2)

#set_property PACKAGE_PIN C17 [get_ports PS2Clk]

#set_property IOSTANDARD LVCMOS33 [get_ports PS2Clk]

#set_property PULLUP true [get_ports PS2Clk]

#set_property PACKAGE_PIN B17 [get_ports PS2Data]

#set_property IOSTANDARD LVCMOS33 [get_ports PS2Data]

#set_property PULLUP true [get_ports PS2Data]

##Quad SPI Flash

##Note that CCLK_0 cannot be placed in 7 series devices. You can access it using the

##STARTUPE2 primitive.

```
#set_property PACKAGE_PIN D18 [get_ports {QspiDB[0]}]
    #set_property IOSTANDARD LVCMOS33 [get_ports {QspiDB[0]}]
#set_property PACKAGE_PIN D19 [get_ports {QspiDB[1]}]
    #set_property IOSTANDARD LVCMOS33 [get_ports {QspiDB[1]}]
#set_property PACKAGE_PIN G18 [get_ports {QspiDB[2]}]
    #set_property IOSTANDARD LVCMOS33 [get_ports {QspiDB[2]}]
#set_property PACKAGE_PIN F18 [get_ports {QspiDB[3]}]
    #set_property IOSTANDARD LVCMOS33 [get_ports {QspiDB[3]}]
#set_property PACKAGE_PIN K19 [get_ports QspiCSn]
    #set_property IOSTANDARD LVCMOS33 [get_ports QspiCSn]
```

Note → *The Verilog codes and the uncommented portions of the constraint files should be copied in your lab report and the* ***actual Verilog (.v), Constraint (.xdc) files and Bitstream (.bit) files*** *need to be zipped and submitted as well on Canvas. You are not allowed to change your codes after final submission as the TAs may download the submitted codes or bitstream files from Canvas during checkouts. For the truth Table, K-maps minimizations and algebraic expressions, you are free to draw them on paper and then put the pictures in your lab report, but please make sure it is legible for the TAs to grade it properly.*