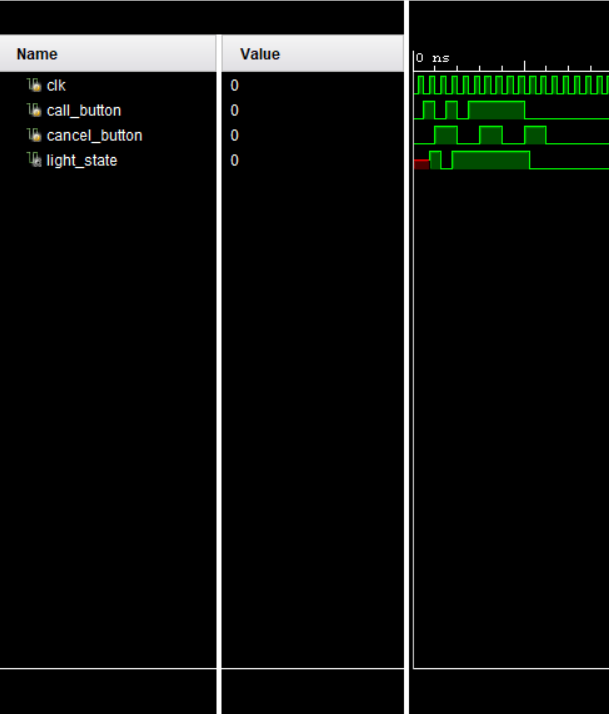
**LAB 4 Report**

**Name: Dhruv Sandesara**

**UT EID: djs3967**

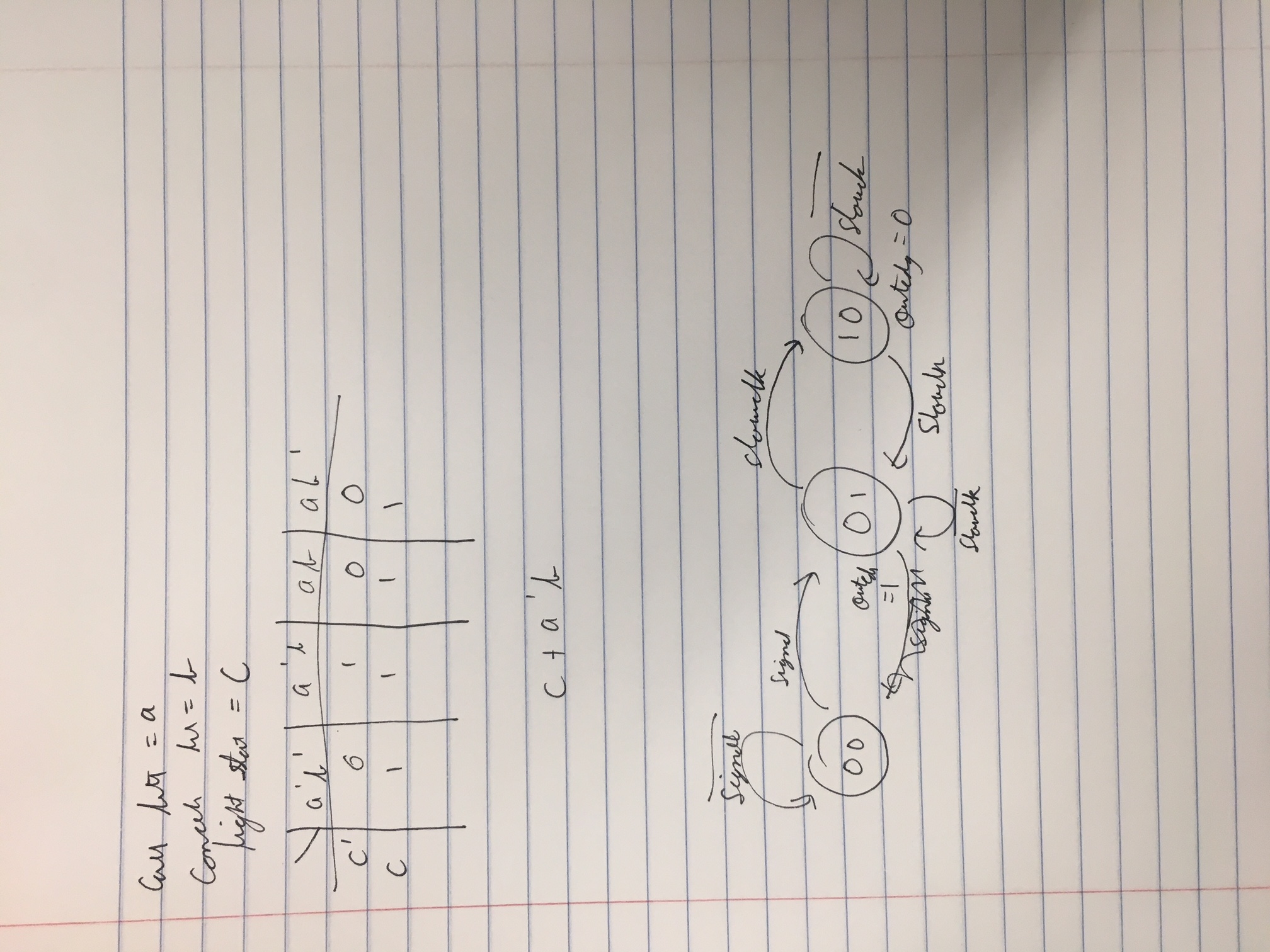
**Section: 15295 (Lab Wednesday 12-1)**

**Checklist:**

**Part 1 -**

1. Simulation waveform of the Flight Attendant Call System for behavioral as well as dataflow modelling
2. K-map for minimizing the expression for next\_state for dataflow modelling

below

1. 
2. Boolean expression for next\_state for dataflow modelling

above

1. Completed design file (.v) for dataflow modelling

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 03/06/2018 07:08:25 PM

// Design Name:

// Module Name: flight\_attendant\_call\_system\_dataflow

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module flight\_attendant\_call\_system\_dataflow(

input wire clk,

input wire call\_button,

input wire cancel\_button,

output reg light\_state

);

wire next\_state;

assign next\_state= call\_button|(~cancel\_button&light\_state);

always@(posedge clk) begin

light\_state<=next\_state;

end

endmodule

**Part 2 -**

1. State Diagram of the Rising Edge Detector

above

1. Completed design files (.v) including the top module and clock divider

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 03/07/2018 12:04:57 AM

// Design Name:

// Module Name: rising\_edge\_detector

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module rising\_edge\_detector(

input clk,

input reset,

input signal,

output reg outedge

);

wire slow\_clk;

reg[1:0] state;

reg[1:0] next\_state;

clkdiv c1(clk, reset,slow\_clk);

always @(state) begin

case(state)

2'b00 : begin

outedge= 1'b0;

if(~signal)

next\_state= 2'b00;

else

next\_state= 2'b01;

end

2'b01 : begin

outedge= 1'b1;

next\_state= 2'b10;

end

2'b10: begin

outedge= 1'b0;

next\_state= 2'b01;

end

default: begin

next\_state=2'b00;

outedge= 1'b0;

end

endcase

end

always @(posedge clk) begin

if(reset)begin

state <= 2'b00;

next\_state <= 2'b00;

end

else

state <= next\_state;

end

endmodule

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 03/07/2018 12:12:33 AM

// Design Name:

// Module Name: clkdiv

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module clkdiv(

input clk,

input reset,

output clk\_out

);

reg [26:0] COUNT;

assign clk\_out= COUNT[16];

always @(posedge clk)

begin

// if (reset)

// COUNT=0;

//else

COUNT=COUNT+1;

end

endmodule

1. Test-bench of the system

`timescale 1ns / 1ps

module tb\_rising\_edge\_detector;

reg clk;

reg signal;

reg reset;

wire outedge;

rising\_edge\_detector u1(

.clk(clk),

.signal(signal),

.reset(reset),

.outedge(outedge)

);

clkdiv u2(

.clk(clk)

);

initial

begin

clk = 0;

signal = 0;

reset = 1;

#10

signal = 0;

reset = 0;

#30

signal = 1;

reset = 0;

#40

signal = 1;

reset = 0;

#40

signal = 0;

reset = 0;

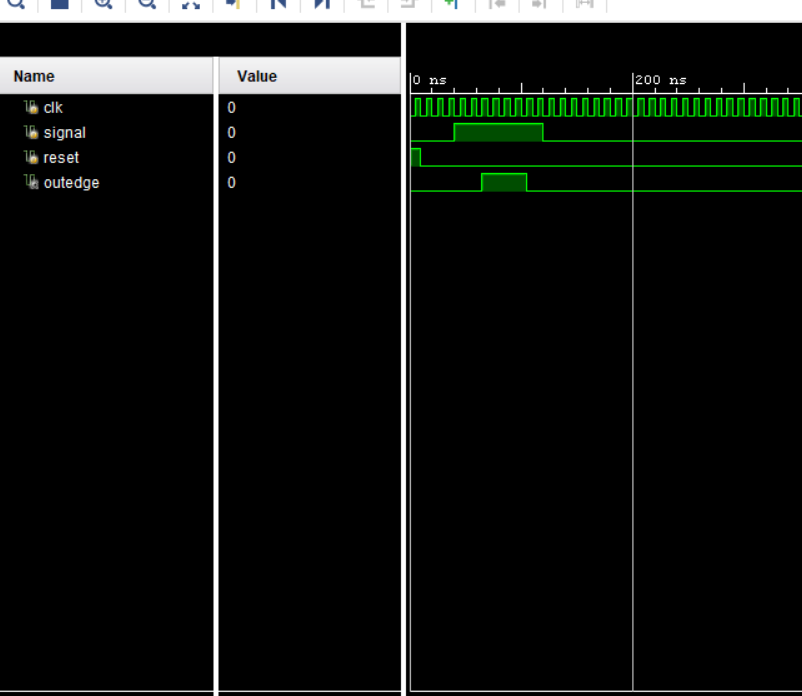
end

always

#5 clk = ~clk;

endmodule

1. Simulation waveform



1. Constraints File (Just the uncommented portion)

## This file is a general .xdc for the Basys3 rev B board

## To use it in a project:

## - uncomment the lines corresponding to used pins

## - rename the used ports (in each line, after get\_ports) according to the top level signal names in the project

## Clock signal

set\_property PACKAGE\_PIN W5 [get\_ports clk]

set\_property IOSTANDARD LVCMOS33 [get\_ports clk]

create\_clock -add -name sys\_clk\_pin -period 10.00 -waveform {0 5} [get\_ports clk]

## Switches

set\_property PACKAGE\_PIN V17 [get\_ports {signal}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {signal}]

#set\_property PACKAGE\_PIN V16 [get\_ports {sw[1]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[1]}]

#set\_property PACKAGE\_PIN W16 [get\_ports {sw[2]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[2]}]

#set\_property PACKAGE\_PIN W17 [get\_ports {sw[3]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[3]}]

#set\_property PACKAGE\_PIN W15 [get\_ports {sw[4]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[4]}]

#set\_property PACKAGE\_PIN V15 [get\_ports {sw[5]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[5]}]

#set\_property PACKAGE\_PIN W14 [get\_ports {sw[6]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[6]}]

#set\_property PACKAGE\_PIN W13 [get\_ports {sw[7]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[7]}]

#set\_property PACKAGE\_PIN V2 [get\_ports {sw[8]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[8]}]

#set\_property PACKAGE\_PIN T3 [get\_ports {sw[9]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[9]}]

#set\_property PACKAGE\_PIN T2 [get\_ports {sw[10]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[10]}]

#set\_property PACKAGE\_PIN R3 [get\_ports {sw[11]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[11]}]

#set\_property PACKAGE\_PIN W2 [get\_ports {sw[12]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[12]}]

#set\_property PACKAGE\_PIN U1 [get\_ports {sw[13]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[13]}]

#set\_property PACKAGE\_PIN T1 [get\_ports {sw[14]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[14]}]

#set\_property PACKAGE\_PIN R2 [get\_ports {sw[15]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[15]}]

## LEDs

set\_property PACKAGE\_PIN U16 [get\_ports {outedge}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {outedge}]

#set\_property PACKAGE\_PIN E19 [get\_ports {led[1]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[1]}]

#set\_property PACKAGE\_PIN U19 [get\_ports {led[2]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[2]}]

#set\_property PACKAGE\_PIN V19 [get\_ports {led[3]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[3]}]

#set\_property PACKAGE\_PIN W18 [get\_ports {led[4]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[4]}]

#set\_property PACKAGE\_PIN U15 [get\_ports {led[5]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[5]}]

#set\_property PACKAGE\_PIN U14 [get\_ports {led[6]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[6]}]

#set\_property PACKAGE\_PIN V14 [get\_ports {led[7]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[7]}]

#set\_property PACKAGE\_PIN V13 [get\_ports {led[8]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[8]}]

#set\_property PACKAGE\_PIN V3 [get\_ports {led[9]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[9]}]

#set\_property PACKAGE\_PIN W3 [get\_ports {led[10]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[10]}]

#set\_property PACKAGE\_PIN U3 [get\_ports {led[11]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[11]}]

#set\_property PACKAGE\_PIN P3 [get\_ports {led[12]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[12]}]

#set\_property PACKAGE\_PIN N3 [get\_ports {led[13]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[13]}]

#set\_property PACKAGE\_PIN P1 [get\_ports {led[14]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[14]}]

#set\_property PACKAGE\_PIN L1 [get\_ports {led[15]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[15]}]

##7 segment display

#set\_property PACKAGE\_PIN W7 [get\_ports {seg[0]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {seg[0]}]

#set\_property PACKAGE\_PIN W6 [get\_ports {seg[1]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {seg[1]}]

#set\_property PACKAGE\_PIN U8 [get\_ports {seg[2]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {seg[2]}]

#set\_property PACKAGE\_PIN V8 [get\_ports {seg[3]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {seg[3]}]

#set\_property PACKAGE\_PIN U5 [get\_ports {seg[4]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {seg[4]}]

#set\_property PACKAGE\_PIN V5 [get\_ports {seg[5]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {seg[5]}]

#set\_property PACKAGE\_PIN U7 [get\_ports {seg[6]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {seg[6]}]

#set\_property PACKAGE\_PIN V7 [get\_ports dp]

#set\_property IOSTANDARD LVCMOS33 [get\_ports dp]

#set\_property PACKAGE\_PIN U2 [get\_ports {an[0]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {an[0]}]

#set\_property PACKAGE\_PIN U4 [get\_ports {an[1]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {an[1]}]

#set\_property PACKAGE\_PIN V4 [get\_ports {an[2]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {an[2]}]

#set\_property PACKAGE\_PIN W4 [get\_ports {an[3]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {an[3]}]

##Buttons

set\_property PACKAGE\_PIN U18 [get\_ports reset]

set\_property IOSTANDARD LVCMOS33 [get\_ports reset]

#set\_property PACKAGE\_PIN T18 [get\_ports btnU]

#set\_property IOSTANDARD LVCMOS33 [get\_ports btnU]

#set\_property PACKAGE\_PIN W19 [get\_ports btnL]

#set\_property IOSTANDARD LVCMOS33 [get\_ports btnL]

#set\_property PACKAGE\_PIN T17 [get\_ports btnR]

#set\_property IOSTANDARD LVCMOS33 [get\_ports btnR]

#set\_property PACKAGE\_PIN U17 [get\_ports btnD]

#set\_property IOSTANDARD LVCMOS33 [get\_ports btnD]

##Pmod Header JA

##Sch name = JA1

#set\_property PACKAGE\_PIN J1 [get\_ports {JA[0]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JA[0]}]

##Sch name = JA2

#set\_property PACKAGE\_PIN L2 [get\_ports {JA[1]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JA[1]}]

##Sch name = JA3

#set\_property PACKAGE\_PIN J2 [get\_ports {JA[2]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JA[2]}]

##Sch name = JA4

#set\_property PACKAGE\_PIN G2 [get\_ports {JA[3]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JA[3]}]

##Sch name = JA7

#set\_property PACKAGE\_PIN H1 [get\_ports {JA[4]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JA[4]}]

##Sch name = JA8

#set\_property PACKAGE\_PIN K2 [get\_ports {JA[5]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JA[5]}]

##Sch name = JA9

#set\_property PACKAGE\_PIN H2 [get\_ports {JA[6]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JA[6]}]

##Sch name = JA10

#set\_property PACKAGE\_PIN G3 [get\_ports {JA[7]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JA[7]}]

##Pmod Header JB

##Sch name = JB1

#set\_property PACKAGE\_PIN A14 [get\_ports {JB[0]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JB[0]}]

##Sch name = JB2

#set\_property PACKAGE\_PIN A16 [get\_ports {JB[1]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JB[1]}]

##Sch name = JB3

#set\_property PACKAGE\_PIN B15 [get\_ports {JB[2]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JB[2]}]

##Sch name = JB4

#set\_property PACKAGE\_PIN B16 [get\_ports {JB[3]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JB[3]}]

##Sch name = JB7

#set\_property PACKAGE\_PIN A15 [get\_ports {JB[4]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JB[4]}]

##Sch name = JB8

#set\_property PACKAGE\_PIN A17 [get\_ports {JB[5]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JB[5]}]

##Sch name = JB9

#set\_property PACKAGE\_PIN C15 [get\_ports {JB[6]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JB[6]}]

##Sch name = JB10

#set\_property PACKAGE\_PIN C16 [get\_ports {JB[7]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JB[7]}]

##Pmod Header JC

##Sch name = JC1

#set\_property PACKAGE\_PIN K17 [get\_ports {JC[0]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JC[0]}]

##Sch name = JC2

#set\_property PACKAGE\_PIN M18 [get\_ports {JC[1]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JC[1]}]

##Sch name = JC3

#set\_property PACKAGE\_PIN N17 [get\_ports {JC[2]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JC[2]}]

##Sch name = JC4

#set\_property PACKAGE\_PIN P18 [get\_ports {JC[3]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JC[3]}]

##Sch name = JC7

#set\_property PACKAGE\_PIN L17 [get\_ports {JC[4]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JC[4]}]

##Sch name = JC8

#set\_property PACKAGE\_PIN M19 [get\_ports {JC[5]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JC[5]}]

##Sch name = JC9

#set\_property PACKAGE\_PIN P17 [get\_ports {JC[6]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JC[6]}]

##Sch name = JC10

#set\_property PACKAGE\_PIN R18 [get\_ports {JC[7]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JC[7]}]

##Pmod Header JXADC

##Sch name = XA1\_P

#set\_property PACKAGE\_PIN J3 [get\_ports {JXADC[0]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JXADC[0]}]

##Sch name = XA2\_P

#set\_property PACKAGE\_PIN L3 [get\_ports {JXADC[1]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JXADC[1]}]

##Sch name = XA3\_P

#set\_property PACKAGE\_PIN M2 [get\_ports {JXADC[2]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JXADC[2]}]

##Sch name = XA4\_P

#set\_property PACKAGE\_PIN N2 [get\_ports {JXADC[3]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JXADC[3]}]

##Sch name = XA1\_N

#set\_property PACKAGE\_PIN K3 [get\_ports {JXADC[4]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JXADC[4]}]

##Sch name = XA2\_N

#set\_property PACKAGE\_PIN M3 [get\_ports {JXADC[5]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JXADC[5]}]

##Sch name = XA3\_N

#set\_property PACKAGE\_PIN M1 [get\_ports {JXADC[6]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JXADC[6]}]

##Sch name = XA4\_N

#set\_property PACKAGE\_PIN N1 [get\_ports {JXADC[7]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JXADC[7]}]

##VGA Connector

#set\_property PACKAGE\_PIN G19 [get\_ports {vgaRed[0]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaRed[0]}]

#set\_property PACKAGE\_PIN H19 [get\_ports {vgaRed[1]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaRed[1]}]

#set\_property PACKAGE\_PIN J19 [get\_ports {vgaRed[2]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaRed[2]}]

#set\_property PACKAGE\_PIN N19 [get\_ports {vgaRed[3]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaRed[3]}]

#set\_property PACKAGE\_PIN N18 [get\_ports {vgaBlue[0]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaBlue[0]}]

#set\_property PACKAGE\_PIN L18 [get\_ports {vgaBlue[1]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaBlue[1]}]

#set\_property PACKAGE\_PIN K18 [get\_ports {vgaBlue[2]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaBlue[2]}]

#set\_property PACKAGE\_PIN J18 [get\_ports {vgaBlue[3]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaBlue[3]}]

#set\_property PACKAGE\_PIN J17 [get\_ports {vgaGreen[0]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaGreen[0]}]

#set\_property PACKAGE\_PIN H17 [get\_ports {vgaGreen[1]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaGreen[1]}]

#set\_property PACKAGE\_PIN G17 [get\_ports {vgaGreen[2]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaGreen[2]}]

#set\_property PACKAGE\_PIN D17 [get\_ports {vgaGreen[3]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaGreen[3]}]

#set\_property PACKAGE\_PIN P19 [get\_ports Hsync]

#set\_property IOSTANDARD LVCMOS33 [get\_ports Hsync]

#set\_property PACKAGE\_PIN R19 [get\_ports Vsync]

#set\_property IOSTANDARD LVCMOS33 [get\_ports Vsync]

##USB-RS232 Interface

#set\_property PACKAGE\_PIN B18 [get\_ports RsRx]

#set\_property IOSTANDARD LVCMOS33 [get\_ports RsRx]

#set\_property PACKAGE\_PIN A18 [get\_ports RsTx]

#set\_property IOSTANDARD LVCMOS33 [get\_ports RsTx]

##USB HID (PS/2)

#set\_property PACKAGE\_PIN C17 [get\_ports PS2Clk]

#set\_property IOSTANDARD LVCMOS33 [get\_ports PS2Clk]

#set\_property PULLUP true [get\_ports PS2Clk]

#set\_property PACKAGE\_PIN B17 [get\_ports PS2Data]

#set\_property IOSTANDARD LVCMOS33 [get\_ports PS2Data]

#set\_property PULLUP true [get\_ports PS2Data]

##Quad SPI Flash

##Note that CCLK\_0 cannot be placed in 7 series devices. You can access it using the

##STARTUPE2 primitive.

#set\_property PACKAGE\_PIN D18 [get\_ports {QspiDB[0]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {QspiDB[0]}]

#set\_property PACKAGE\_PIN D19 [get\_ports {QspiDB[1]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {QspiDB[1]}]

#set\_property PACKAGE\_PIN G18 [get\_ports {QspiDB[2]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {QspiDB[2]}]

#set\_property PACKAGE\_PIN F18 [get\_ports {QspiDB[3]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {QspiDB[3]}]

#set\_property PACKAGE\_PIN K19 [get\_ports QspiCSn]

#set\_property IOSTANDARD LVCMOS33 [get\_ports QspiCSn]

**Part 3 -**

1. Completed design files (.v) of all the modules in the system

`timescale 1ns / 1ps

module clkdiv(

input clk,

input reset,

output slow\_clk

);

reg [25:0] COUNT;

assign slow\_clk = COUNT[25];

always @(posedge clk) begin

if(reset)

COUNT = 0;

else

COUNT = COUNT + 1;

end

endmodule

`timescale 1ns / 1ps

module hexto7segment(

input [3:0] x,

output reg [6:0] r

);

always @(\*)

case(x)

4'b0000 : r = 7'b0000001;

4'b0001 : r = 7'b1001111;

4'b0010 : r = 7'b0010010;

4'b0011 : r = 7'b0000110;

4'b0100 : r = 7'b1001100;

4'b0101 : r = 7'b0100100;

4'b0110 : r = 7'b0100000;

4'b0111 : r = 7'b0001111;

4'b1000 : r = 7'b0000000;

4'b1001 : r = 7'b0001100;

4'b1010 : r = 7'b1111111;

4'b1011 : r = 7'b1111111;

4'b1100 : r = 7'b1111111;

4'b1101 : r = 7'b1111111;

4'b1110 : r = 7'b1111111;

4'b1111 : r = 7'b1111111;

endcase

endmodule

`timescale 1ns / 1ps

module tb\_time\_multiplexing\_main;

reg clk;

reg reset;

reg [15:0]sw;

wire [3:0] an;

wire [6:0] sseg;

time\_multiplexing\_main u1(

.clk(clk),

.reset(reset),

.sw(sw),

.an(an),

.sseg(sseg)

);

initial begin

sw = 16'h0000;

clk = 0;

reset = 0;

#30

reset = 0;

sw = 16'h0008;

#30;

reset = 0;

sw = 16'h4321;

#30;

reset = 0;

sw = 16'h0002;

#30;

reset = 0;

sw = 16'h0302;

end

always

#5 clk = ~clk;

endmodule

`timescale 1ns / 1ps

module time\_multiplexing\_main(

input clk,

input reset,

input [15:0] sw,

output [3:0] an,

output [6:0] sseg);

wire [6:0] in0, in1, in2, in3 ;

wire slow\_clk;

hexto7segment c1 (.x(sw[3:0]), .r(in0));

hexto7segment c2 (.x(sw[7:4]), .r(in1));

hexto7segment c3 (.x(sw[11:8]), .r(in2));

hexto7segment c4 (.x(sw[15:12]), .r(in3));

clkdiv c5 (.clk(clk), .reset(reset), .slow\_clk(slow\_clk));

time\_mux\_state\_machine c6(

.clk (slow\_clk),

.reset (reset),

.in0 (in0),

.in1 (in1),

.in2 (in2),

.in3 (in3),

.an (an),

.sseg (sseg));

Endmodule

`timescale 1ns / 1ps

module time\_mux\_state\_machine(

input clk,

input reset,

input [6:0] in0,

input [6:0] in1,

input [6:0] in2,

input [6:0] in3,

output reg [3:0] an,

output reg [6:0] sseg

);

reg [1:0] state;

reg [1:0] next\_state;

always @(\*) begin

case(state)

2'b00: next\_state = 2'b01;

2'b01: next\_state = 2'b10;

2'b10: next\_state = 2'b11;

2'b11: next\_state = 2'b00;

endcase

end

always @(\*) begin

case(state)

2'b00: sseg = in0;

2'b01: sseg = in1;

2'b10: sseg = in2;

2'b11: sseg = in3;

endcase

case(state)

2'b00: an = 4'b1110;

2'b01: an = 4'b1101;

2'b10: an = 4'b1011;

2'b11: an = 4'b0111;

endcase

end

always @(posedge clk or posedge reset) begin

if(reset)

state <= 2'b00;

else

state <= next\_state;

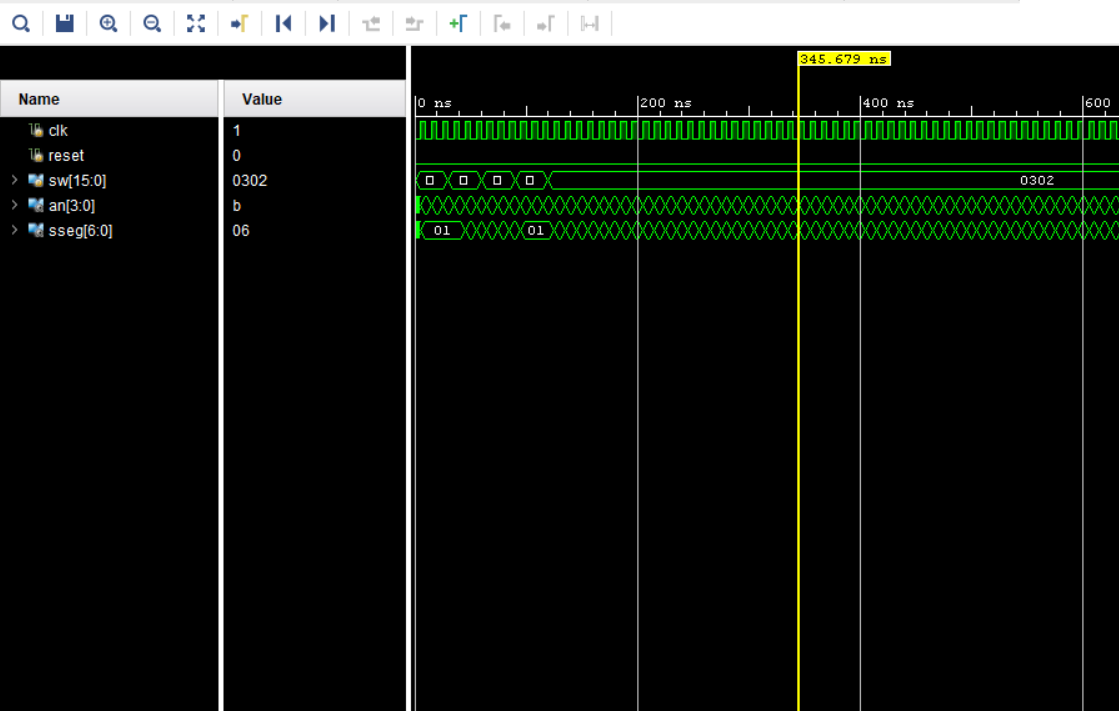
end

endmodule

1. Test-bench of the system

Above

1. Simulation waveform



1. Constraints File (Just the uncommented portion)

## This file is a general .xdc for the Basys3 rev B board

## To use it in a project:

## - uncomment the lines corresponding to used pins

## - rename the used ports (in each line, after get\_ports) according to the top level signal names in the project

## Clock signal

set\_property PACKAGE\_PIN W5 [get\_ports {clk}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {clk}]

create\_clock -add -name sys\_clk\_pin -period 10.00 -waveform {0 5} [get\_ports {clk}]

## Switches

set\_property PACKAGE\_PIN V17 [get\_ports {sw[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[0]}]

set\_property PACKAGE\_PIN V16 [get\_ports {sw[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[1]}]

set\_property PACKAGE\_PIN W16 [get\_ports {sw[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[2]}]

set\_property PACKAGE\_PIN W17 [get\_ports {sw[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[3]}]

set\_property PACKAGE\_PIN W15 [get\_ports {sw[4]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[4]}]

set\_property PACKAGE\_PIN V15 [get\_ports {sw[5]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[5]}]

set\_property PACKAGE\_PIN W14 [get\_ports {sw[6]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[6]}]

set\_property PACKAGE\_PIN W13 [get\_ports {sw[7]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[7]}]

set\_property PACKAGE\_PIN V2 [get\_ports {sw[8]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[8]}]

set\_property PACKAGE\_PIN T3 [get\_ports {sw[9]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[9]}]

set\_property PACKAGE\_PIN T2 [get\_ports {sw[10]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[10]}]

set\_property PACKAGE\_PIN R3 [get\_ports {sw[11]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[11]}]

set\_property PACKAGE\_PIN W2 [get\_ports {sw[12]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[12]}]

set\_property PACKAGE\_PIN U1 [get\_ports {sw[13]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[13]}]

set\_property PACKAGE\_PIN T1 [get\_ports {sw[14]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[14]}]

set\_property PACKAGE\_PIN R2 [get\_ports {sw[15]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[15]}]

## LEDs

#set\_property PACKAGE\_PIN U16 [get\_ports {led[0]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[0]}]

#set\_property PACKAGE\_PIN E19 [get\_ports {led[1]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[1]}]

#set\_property PACKAGE\_PIN U19 [get\_ports {led[2]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[2]}]

#set\_property PACKAGE\_PIN V19 [get\_ports {led[3]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[3]}]

#set\_property PACKAGE\_PIN W18 [get\_ports {led[4]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[4]}]

#set\_property PACKAGE\_PIN U15 [get\_ports {led[5]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[5]}]

#set\_property PACKAGE\_PIN U14 [get\_ports {led[6]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[6]}]

#set\_property PACKAGE\_PIN V14 [get\_ports {led[7]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[7]}]

#set\_property PACKAGE\_PIN V13 [get\_ports {led[8]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[8]}]

#set\_property PACKAGE\_PIN V3 [get\_ports {led[9]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[9]}]

#set\_property PACKAGE\_PIN W3 [get\_ports {led[10]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[10]}]

#set\_property PACKAGE\_PIN U3 [get\_ports {led[11]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[11]}]

#set\_property PACKAGE\_PIN P3 [get\_ports {led[12]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[12]}]

#set\_property PACKAGE\_PIN N3 [get\_ports {led[13]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[13]}]

#set\_property PACKAGE\_PIN P1 [get\_ports {led[14]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[14]}]

#set\_property PACKAGE\_PIN L1 [get\_ports {led[15]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {led[15]}]

##7 segment display

set\_property PACKAGE\_PIN W7 [get\_ports {sseg[6]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sseg[6]}]

set\_property PACKAGE\_PIN W6 [get\_ports {sseg[5]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sseg[5]}]

set\_property PACKAGE\_PIN U8 [get\_ports {sseg[4]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sseg[4]}]

set\_property PACKAGE\_PIN V8 [get\_ports {sseg[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sseg[3]}]

set\_property PACKAGE\_PIN U5 [get\_ports {sseg[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sseg[2]}]

set\_property PACKAGE\_PIN V5 [get\_ports {sseg[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sseg[1]}]

set\_property PACKAGE\_PIN U7 [get\_ports {sseg[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sseg[0]}]

#set\_property PACKAGE\_PIN V7 [get\_ports dp]

#set\_property IOSTANDARD LVCMOS33 [get\_ports dp]

set\_property PACKAGE\_PIN U2 [get\_ports {an[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[0]}]

set\_property PACKAGE\_PIN U4 [get\_ports {an[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[1]}]

set\_property PACKAGE\_PIN V4 [get\_ports {an[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[2]}]

set\_property PACKAGE\_PIN W4 [get\_ports {an[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[3]}]

##Buttons

set\_property PACKAGE\_PIN U18 [get\_ports reset]

set\_property IOSTANDARD LVCMOS33 [get\_ports reset]

#set\_property PACKAGE\_PIN T18 [get\_ports btnU]

#set\_property IOSTANDARD LVCMOS33 [get\_ports btnU]

#set\_property PACKAGE\_PIN W19 [get\_ports btnL]

#set\_property IOSTANDARD LVCMOS33 [get\_ports btnL]

#set\_property PACKAGE\_PIN T17 [get\_ports btnR]

#set\_property IOSTANDARD LVCMOS33 [get\_ports btnR]

#set\_property PACKAGE\_PIN U17 [get\_ports btnD]

#set\_property IOSTANDARD LVCMOS33 [get\_ports btnD]

##Pmod Header JA

##Sch name = JA1

#set\_property PACKAGE\_PIN J1 [get\_ports {JA[0]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JA[0]}]

##Sch name = JA2

#set\_property PACKAGE\_PIN L2 [get\_ports {JA[1]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JA[1]}]

##Sch name = JA3

#set\_property PACKAGE\_PIN J2 [get\_ports {JA[2]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JA[2]}]

##Sch name = JA4

#set\_property PACKAGE\_PIN G2 [get\_ports {JA[3]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JA[3]}]

##Sch name = JA7

#set\_property PACKAGE\_PIN H1 [get\_ports {JA[4]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JA[4]}]

##Sch name = JA8

#set\_property PACKAGE\_PIN K2 [get\_ports {JA[5]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JA[5]}]

##Sch name = JA9

#set\_property PACKAGE\_PIN H2 [get\_ports {JA[6]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JA[6]}]

##Sch name = JA10

#set\_property PACKAGE\_PIN G3 [get\_ports {JA[7]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JA[7]}]

##Pmod Header JB

##Sch name = JB1

#set\_property PACKAGE\_PIN A14 [get\_ports {JB[0]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JB[0]}]

##Sch name = JB2

#set\_property PACKAGE\_PIN A16 [get\_ports {JB[1]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JB[1]}]

##Sch name = JB3

#set\_property PACKAGE\_PIN B15 [get\_ports {JB[2]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JB[2]}]

##Sch name = JB4

#set\_property PACKAGE\_PIN B16 [get\_ports {JB[3]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JB[3]}]

##Sch name = JB7

#set\_property PACKAGE\_PIN A15 [get\_ports {JB[4]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JB[4]}]

##Sch name = JB8

#set\_property PACKAGE\_PIN A17 [get\_ports {JB[5]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JB[5]}]

##Sch name = JB9

#set\_property PACKAGE\_PIN C15 [get\_ports {JB[6]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JB[6]}]

##Sch name = JB10

#set\_property PACKAGE\_PIN C16 [get\_ports {JB[7]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JB[7]}]

##Pmod Header JC

##Sch name = JC1

#set\_property PACKAGE\_PIN K17 [get\_ports {JC[0]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JC[0]}]

##Sch name = JC2

#set\_property PACKAGE\_PIN M18 [get\_ports {JC[1]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JC[1]}]

##Sch name = JC3

#set\_property PACKAGE\_PIN N17 [get\_ports {JC[2]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JC[2]}]

##Sch name = JC4

#set\_property PACKAGE\_PIN P18 [get\_ports {JC[3]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JC[3]}]

##Sch name = JC7

#set\_property PACKAGE\_PIN L17 [get\_ports {JC[4]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JC[4]}]

##Sch name = JC8

#set\_property PACKAGE\_PIN M19 [get\_ports {JC[5]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JC[5]}]

##Sch name = JC9

#set\_property PACKAGE\_PIN P17 [get\_ports {JC[6]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JC[6]}]

##Sch name = JC10

#set\_property PACKAGE\_PIN R18 [get\_ports {JC[7]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JC[7]}]

##Pmod Header JXADC

##Sch name = XA1\_P

#set\_property PACKAGE\_PIN J3 [get\_ports {JXADC[0]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JXADC[0]}]

##Sch name = XA2\_P

#set\_property PACKAGE\_PIN L3 [get\_ports {JXADC[1]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JXADC[1]}]

##Sch name = XA3\_P

#set\_property PACKAGE\_PIN M2 [get\_ports {JXADC[2]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JXADC[2]}]

##Sch name = XA4\_P

#set\_property PACKAGE\_PIN N2 [get\_ports {JXADC[3]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JXADC[3]}]

##Sch name = XA1\_N

#set\_property PACKAGE\_PIN K3 [get\_ports {JXADC[4]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JXADC[4]}]

##Sch name = XA2\_N

#set\_property PACKAGE\_PIN M3 [get\_ports {JXADC[5]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JXADC[5]}]

##Sch name = XA3\_N

#set\_property PACKAGE\_PIN M1 [get\_ports {JXADC[6]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JXADC[6]}]

##Sch name = XA4\_N

#set\_property PACKAGE\_PIN N1 [get\_ports {JXADC[7]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {JXADC[7]}]

##VGA Connector

#set\_property PACKAGE\_PIN G19 [get\_ports {vgaRed[0]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaRed[0]}]

#set\_property PACKAGE\_PIN H19 [get\_ports {vgaRed[1]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaRed[1]}]

#set\_property PACKAGE\_PIN J19 [get\_ports {vgaRed[2]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaRed[2]}]

#set\_property PACKAGE\_PIN N19 [get\_ports {vgaRed[3]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaRed[3]}]

#set\_property PACKAGE\_PIN N18 [get\_ports {vgaBlue[0]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaBlue[0]}]

#set\_property PACKAGE\_PIN L18 [get\_ports {vgaBlue[1]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaBlue[1]}]

#set\_property PACKAGE\_PIN K18 [get\_ports {vgaBlue[2]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaBlue[2]}]

#set\_property PACKAGE\_PIN J18 [get\_ports {vgaBlue[3]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaBlue[3]}]

#set\_property PACKAGE\_PIN J17 [get\_ports {vgaGreen[0]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaGreen[0]}]

#set\_property PACKAGE\_PIN H17 [get\_ports {vgaGreen[1]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaGreen[1]}]

#set\_property PACKAGE\_PIN G17 [get\_ports {vgaGreen[2]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaGreen[2]}]

#set\_property PACKAGE\_PIN D17 [get\_ports {vgaGreen[3]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {vgaGreen[3]}]

#set\_property PACKAGE\_PIN P19 [get\_ports Hsync]

#set\_property IOSTANDARD LVCMOS33 [get\_ports Hsync]

#set\_property PACKAGE\_PIN R19 [get\_ports Vsync]

#set\_property IOSTANDARD LVCMOS33 [get\_ports Vsync]

##USB-RS232 Interface

#set\_property PACKAGE\_PIN B18 [get\_ports RsRx]

#set\_property IOSTANDARD LVCMOS33 [get\_ports RsRx]

#set\_property PACKAGE\_PIN A18 [get\_ports RsTx]

#set\_property IOSTANDARD LVCMOS33 [get\_ports RsTx]

##USB HID (PS/2)

#set\_property PACKAGE\_PIN C17 [get\_ports PS2Clk]

#set\_property IOSTANDARD LVCMOS33 [get\_ports PS2Clk]

#set\_property PULLUP true [get\_ports PS2Clk]

#set\_property PACKAGE\_PIN B17 [get\_ports PS2Data]

#set\_property IOSTANDARD LVCMOS33 [get\_ports PS2Data]

#set\_property PULLUP true [get\_ports PS2Data]

##Quad SPI Flash

##Note that CCLK\_0 cannot be placed in 7 series devices. You can access it using the

##STARTUPE2 primitive.

#set\_property PACKAGE\_PIN D18 [get\_ports {QspiDB[0]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {QspiDB[0]}]

#set\_property PACKAGE\_PIN D19 [get\_ports {QspiDB[1]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {QspiDB[1]}]

#set\_property PACKAGE\_PIN G18 [get\_ports {QspiDB[2]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {QspiDB[2]}]

#set\_property PACKAGE\_PIN F18 [get\_ports {QspiDB[3]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {QspiDB[3]}]

#set\_property PACKAGE\_PIN K19 [get\_ports QspiCSn]

#set\_property IOSTANDARD LVCMOS33 [get\_ports QspiCSn]

***Note*** *🡪 The Verilog codes and the uncommented portions of the constraint files should be copied in your lab report and the* ***actual Verilog (.v), Constraint (.xdc) files and Bitstream (.bit) files*** *need to be zipped and submitted as well on Canvas. You are not allowed to change your codes after final submission as the TAs may download the submitted codes or bitstream files from Canvas during checkouts. For the truth Table, K-maps minimizations and algebraic expressions, you are free to draw them on paper and then put the pictures in your lab report, but please make sure it is legible for the TAs to grade it properly.*