**LAB 3 Report**

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**Section: 15295 (Lab Wednesday 12-1)**

**Checklist:**

**Part 2 -**

1. Constraint File (Just the uncommented portion)

set\_property PACKAGE\_PIN U16 [get\_ports {d0}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d0}]

set\_property PACKAGE\_PIN E19 [get\_ports {d1}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d1}]

set\_property PACKAGE\_PIN U19 [get\_ports {d2}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d2}]

set\_property PACKAGE\_PIN V19 [get\_ports {d3}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d3}]

set\_property PACKAGE\_PIN W18 [get\_ports {d4}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d4}]

set\_property PACKAGE\_PIN U15 [get\_ports {d5}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d5}]

set\_property PACKAGE\_PIN U14 [get\_ports {d6}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d6}]

set\_property PACKAGE\_PIN V14 [get\_ports {d7}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d7}]

set\_property PACKAGE\_PIN V17 [get\_ports {c}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {c}]

set\_property PACKAGE\_PIN V16 [get\_ports {b}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {b}]

set\_property PACKAGE\_PIN W16 [get\_ports {a}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {a}]

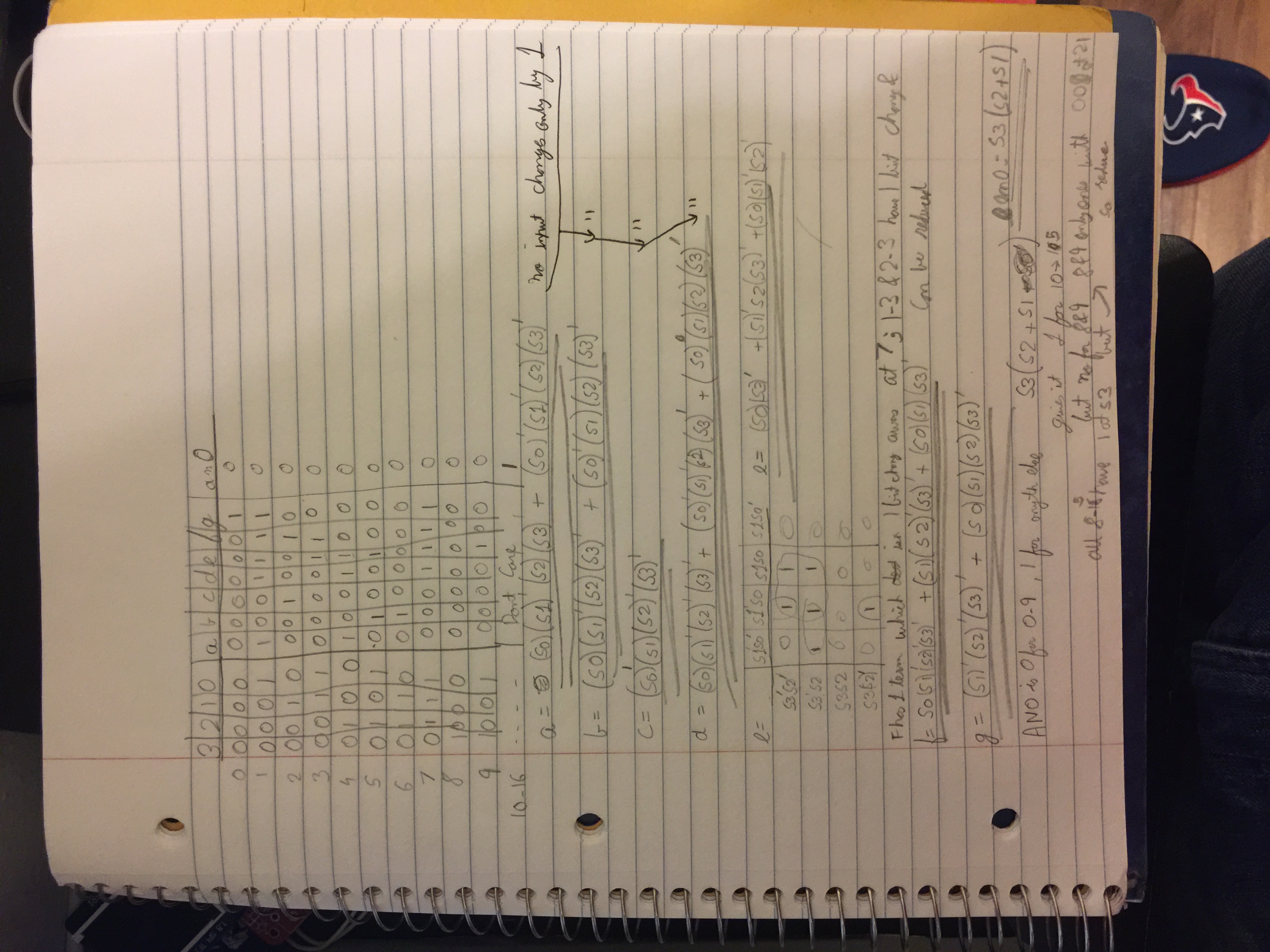
set\_property PACKAGE\_PIN W13 [get\_ports {e}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {e}]

**Part 3 -**

1. Truth Table of the function
2. K-maps showing minimization of the logic functions (outputs)
3. Algebraic expression of the minimized logic functions (outputs)

ALL 3 PARTS COMBINED



1. Verilog codes of module and testbench for structural modelling

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 02/23/2018 02:03:48 PM

// Design Name:

// Module Name: BCD

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module BCD(

input s0,

input s1,

input s2,

input s3,

output a,

output b,

output c,

output d,

output e,

output f,

output g,

output an0,

output an1,

output an2,

output an3 );

wire s0\_not, s1\_not,s2\_not,s3\_not,a0,a1,b0,b1,d0,d1,d2,e0,e1,e2,f0,f1,f2,g00,g01,an00;

not n0(s0\_not,s0);

not n1(s1\_not,s1);

not n2(s2\_not,s2);

not n3(s3\_not,s3);

and g1(a0,s0,s1\_not,s2\_not,s3\_not);

and g2(a1,s0\_not,s1\_not,s2,s3\_not);

or o1(a,a0,a1);

and g3(b0,s0,s1\_not,s2,s3\_not);

and g4(b1,s0\_not,s1,s2,s3\_not);

or o2(b,b0,b1);

and(c,s0\_not,s1,s2\_not,s3\_not);

and g5(d0,s0,s1\_not,s2\_not,s3\_not);

and g6(d1,s0\_not,s1\_not,s2,s3\_not);

and g7(d2,s0,s1,s2,s3\_not);

or o3(d,d0,d1,d2);

and g8(e0,s0,s3\_not);

and g9(e1,s1\_not,s2,s3\_not);

and g10(e2,s0,s1\_not,s2\_not);

or o4(e,e0,e1,e2);

and g11(f0,s0,s1\_not,s2\_not,s3\_not);

and g12(f1,s1,s2\_not,s3\_not);

and g13(f2,s0,s1,s3\_not);

or o5(f,f0,f1,f2);

and g14(g00,s1\_not,s2\_not,s3\_not);

and g15(g01,s0,s1,s2,s3\_not);

or o6(g,g00,g01);

or o7(an00,s2,s1);

and g16(an0,s3,an00);

or g17(an1, 1, 1);

or g18(an2, 1, 1);

or g19(an3, 1, 1);

Endmodule

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 02/23/2018 02:36:04 PM

// Design Name:

// Module Name: tb\_BCD

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module tb\_BCD;

reg s0;

reg s1;

reg s2;

reg s3;

wire a;

wire b;

wire c;

wire d;

wire e;

wire f;

wire g;

wire an0;

BCD uut(

.s0(s0),

.s1(s1),

.s2(s2),

.s3(s3),

.a(a),

.b(b),

.c(c),

.d(d),

.e(e),

.f(f),

.g(g),

.an0(an0),

.an1(an1),

.an2(an2),

.an3(an3),

);

initial begin

s0=0;

s1=0;

s2=0;

s3=0;

#50;

$display("TC00");

if((a!=0)||(b!=0)||(c!=0)||(d!=0)||(e!=0)||(f!=0)||(g!=1)||(an0!=0))$display("Test failed");

s0=1;

s1=0;

s2=0;

s3=0;

#50;

$display("TC01");

if((a!=1)||(b!=0)||(c!=0)||(d!=1)||(e!=1)||(f!=1)||(g!=1)||(an0!=0))$display("Test failed");

s0=0;

s1=1;

s2=0;

s3=0;

#50;

$display("TC02");

if((a!=0)||(b!=0)||(c!=1)||(d!=0)||(e!=0)||(f!=1)||(g!=0)||(an0!=0))$display("Test failed");

s0=1;

s1=1;

s2=0;

s3=0;

#50;

$display("TC03");

if((a!=0)||(b!=0)||(c!=0)||(d!=0)||(e!=1)||(f!=1)||(g!=0)||(an0!=0))$display("Test failed");

s0=0;

s1=0;

s2=1;

s3=0;

#50;

$display("TC04");

if((a!=1)||(b!=0)||(c!=0)||(d!=1)||(e!=1)||(f!=0)||(g!=0)||(an0!=0))$display("Test failed");

s0=1;

s1=0;

s2=1;

s3=0;

#50;

$display("TC05");

if((a!=0)||(b!=1)||(c!=0)||(d!=0)||(e!=1)||(f!=0)||(g!=0)||(an0!=0))$display("Test failed");

s0=0;

s1=1;

s2=1;

s3=0;

#50;

$display("TC05");

if((a!=0)||(b!=1)||(c!=0)||(d!=0)||(e!=0)||(f!=0)||(g!=0)||(an0!=0))$display("Test failed");

s0=1;

s1=1;

s2=1;

s3=0;

#50;

$display("TC07");

if((a!=0)||(b!=0)||(c!=0)||(d!=1)||(e!=1)||(f!=1)||(g!=1)||(an0!=0))$display("Test failed");

s0=0;

s1=0;

s2=0;

s3=1;

#50;

$display("TC08");

if((a!=0)||(b!=0)||(c!=0)||(d!=0)||(e!=0)||(f!=0)||(g!=0)||(an0!=0))$display("Test failed");

s0=1;

s1=0;

s2=0;

s3=1;

#50;

$display("TC09");

if((a!=0)||(b!=0)||(c!=0)||(d!=0)||(e!=1)||(f!=0)||(g!=0)||(an0!=0))$display("Test failed");

s0=0;

s1=1;

s2=0;

s3=1;

#50;

$display("TC10");

if((an0!=1))$display("Test failed");

s0=1;

s1=1;

s2=0;

s3=1;

#50;

$display("TC11");

if((an0!=1))$display("Test failed");

s0=0;

s1=0;

s2=1;

s3=1;

#50;

$display("TC12");

if((an0!=1))$display("Test failed");

s0=1;

s1=0;

s2=1;

s3=1;

#50;

$display("TC13");

if((an0!=1))$display("Test failed");

s0=0;

s1=1;

s2=1;

s3=1;

#50;

$display("TC14");

if((an0!=1))$display("Test failed");

s0=1;

s1=1;

s2=1;

s3=1;

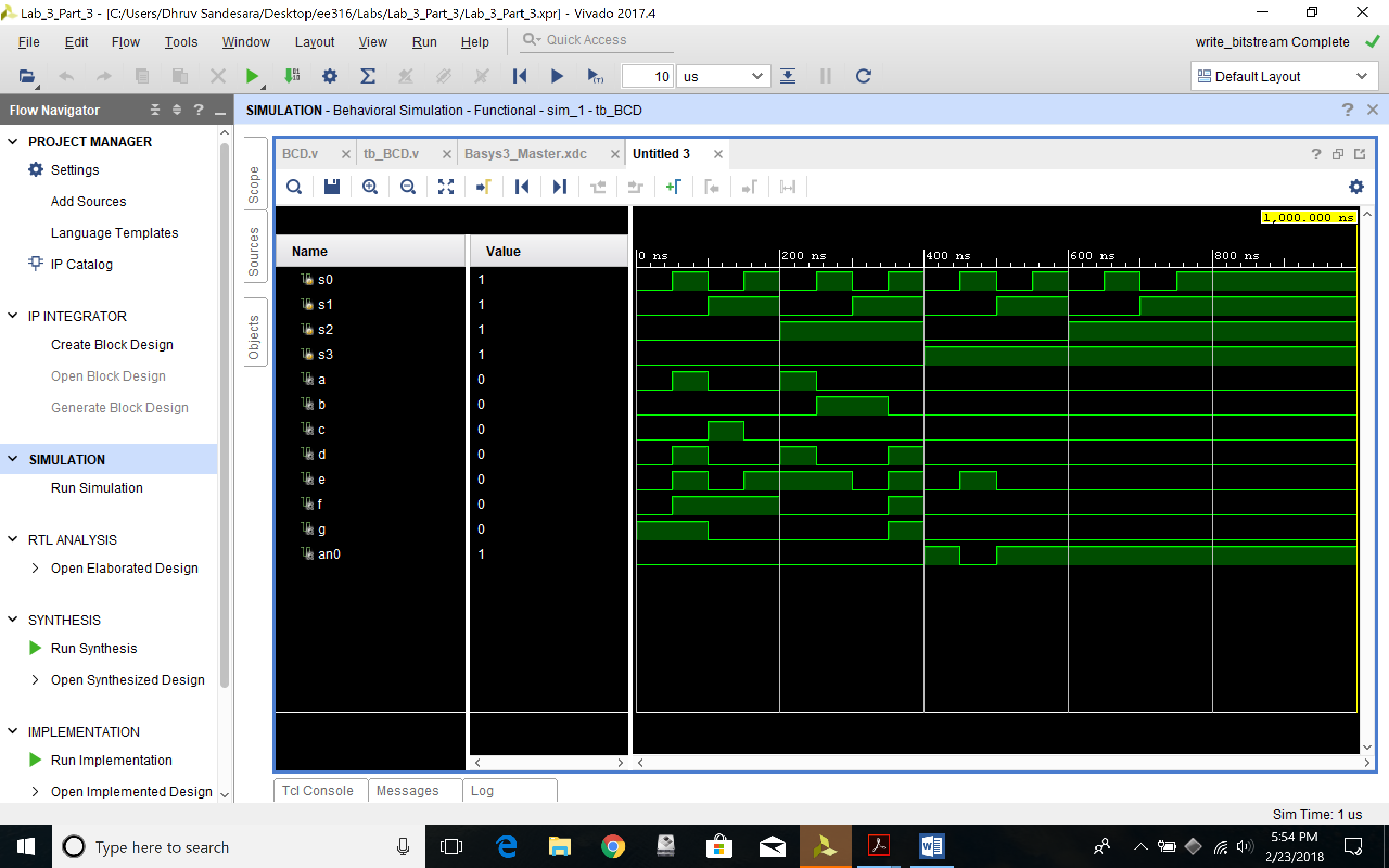
#50;

$display("TC15");

if((an0!=1))$display("Test failed");

end

endmodule

1. Simulation waveform for structural modelling
2. Constraint File (Just the uncommented portion)

set\_property PACKAGE\_PIN V17 [get\_ports {s0}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {s0}]

set\_property PACKAGE\_PIN V16 [get\_ports {s1}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {s1}]

set\_property PACKAGE\_PIN W16 [get\_ports {s2}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {s2}]

set\_property PACKAGE\_PIN W17 [get\_ports {s3}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {s3}]

set\_property PACKAGE\_PIN W7 [get\_ports {a}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {a}]

set\_property PACKAGE\_PIN W6 [get\_ports {b}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {b}]

set\_property PACKAGE\_PIN U8 [get\_ports {c}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {c}]

set\_property PACKAGE\_PIN V8 [get\_ports {d}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d}]

set\_property PACKAGE\_PIN U5 [get\_ports {e}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {e}]

set\_property PACKAGE\_PIN V5 [get\_ports {f}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {f}]

set\_property PACKAGE\_PIN U7 [get\_ports {g}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {g}]

set\_property PACKAGE\_PIN U2 [get\_ports {an0}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an0}]

set\_property PACKAGE\_PIN U4 [get\_ports {an1}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an1}]

set\_property PACKAGE\_PIN V4 [get\_ports {an2}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an2}]

set\_property PACKAGE\_PIN W4 [get\_ports {an3}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an3}]